Characterization and Modeling of Single Charge Trapping in MOS Transistors

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(Invited)

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***Abstract*— Charging and discharging of single defects in MOS transistors seriously affects the performance of integrated devices. To identify the chemical structure of such defects density functional theory calculations can be carried out. For monitoring the impact of the defects on the device behavior the drain-source current through the device is measured and analyzed. The required data is typically recorded by applying voltage sweep measurements, noise/random telegraph noise (RTN) and measure-stress-measure (MSM) experiments. To explain the observed behavior and the impact of single defects on the electrical device characteristics physics-based defect models in combination with device simulators are often employed. After thorough calibration of the models employing detailed experimental data accurate time-to-failure estimations of MOS devices can be made. In this work the most frequently used electrical characterization techniques and advances in physical defect modeling applied to integrated transistors is discussed.**

I. Introduction

The considerable efforts that are put into the enhancement of the performance of integrated MOS transistors has lead to devices with outstanding electrical performance and geometry. Although the finesse of the equipment and processes involved in device fabrication are continuously improved, critical parameters like the threshold voltage, the sub-threshold slope and the on-resistance still remain seriously affected by defects in the atomic structure of the transistor, see Figure 1. Such defects can be charged and uncharged, created or annealed over time and give rise to persistent reliability challenges keeping the research community speculating for their detailed physical origin.

Bias temperature instabilities (BTI), hot-carrier degradation (HCD) and stress induced leakage currents (SILCs) are amongst others the most severe reliability challenges in recent MOS technologies. Both, BTI and HCD are attributed to charging and discharging of oxide defects or defects at the Si/SiO_2 interface, while trap-assisted-tunneling of oxide defects gives rise to SILC especially in devices employing thin oxides [2, 3]. The main difference between BTI and HCD is that in case of BTI the drain bias is kept at zero volt during stress whereas $V_{\mathrm{D}} > V_{\mathrm{G}}/2$ is at least applied for the characterization of HCD in large area devices [4]. At such large drain bias high energetic electrons exists in the channel which can break neutral Si-H bonds leaving an electrically active dangling bond behind [5, 6]. In nanoscale devices, however, the picture of HCD has to be extended to cold carriers, where the dissociation of Si-H bonds involves a series of particles [7–9]. The in case of HCD typically observed increase of the number of interface states reduces the sub-threshold of the devices [9].

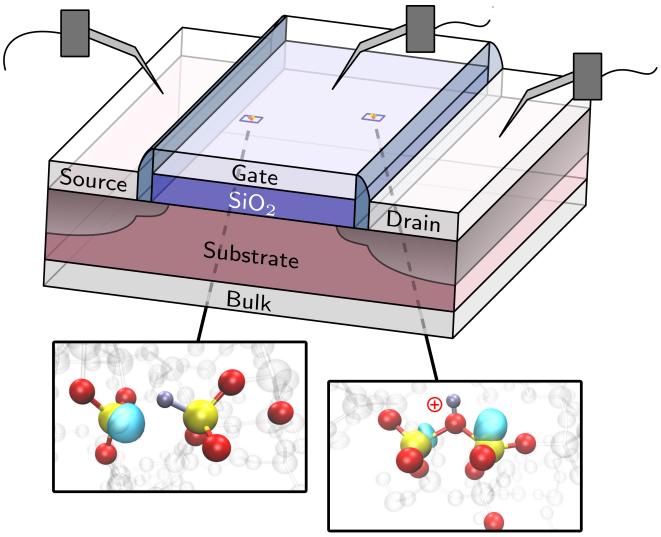

Fig. 1: Defects located at the Si/SiO_2 interface or defects prevalent in the insulating material determine the characteristics of integrated MOS transistors. The atomic configuration of the defects can be calculated from ab-initio methods, here shown is (lower left) the neutral configuration of the hydrogen bridge and (lower right) the charged configuration of the hydroxyl E' center (Si atoms are yellow, oxygen atoms are red, and electron density of the localized Kohn-Sham-eigenstate is shown as turquoise bubbles) [1]. For the characterization the devices are typically contacted directly at wafer level.

To study the impact of BTI on the device characteristics the observed drift of the current through the device recorded at constant bias is typically expressed as an equivalent drift of the threshold voltage ΔV_{th} [10–13]. The origin of the transient characteristics of ΔV_{th} lies in defects which can become repeatedly charged and discharged over time. Next to charge trapping involving existing defects, also new defects can be created during operation giving rise for a strongly time-dependent device reliability. The newly created defects not only affect BTI, but can further act as trap assisted tunneling centers and can thus can lead to an increase of the tunneling current through the insulator at low electric fields, which is referred to as SILC [14]. SILC can be particularly important for SRAMs, where an increase of the leakage current causes an unintentional discharging of memory cells and thus affects

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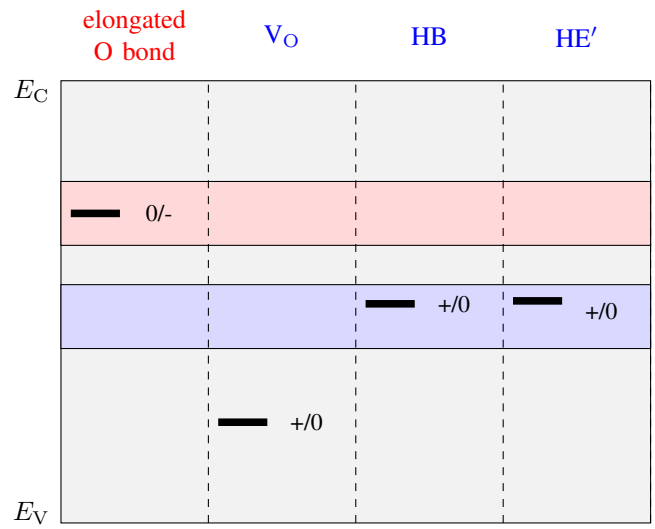

Fig. 2: The charge transition levels (CTLs) of different possible defect candidates for electron traps (red) and hole traps (blue) are given [23, 24]. Also the area for the active energy regions for charge trapping (red for electron trapping and blue for hole trapping) which can be typically accessed by electrical measurements are shown. As can be seen, the elongated oxygen bond is a suitable candidate with its CTL inside the AER relevant for charge trapping in nMOS devices. The CTL of the oxygen vacancy (V_O) is calculated to lie below the AER of hole trapping in pMOS transistors, and thus it will be unlikely that this defect changes its charge state during the experiment [23]. In contrast, the CTLs of the hydrogen bridge (HB) and the hydroxyl E' center are nicely arranged inside the AER for hole trapping [23].

the data rentation time [15].

II. Defects in MOS Transistors

So far, many studies have been devoted to point defects in the Si/SiO_2 material system, however their exact microscopic picture is still controversially discussed. For instance, electronic spin resonance (ESR) or electrically detected magnetic resonance (EDMR) measurements are used to study materials exhibiting unpaired electrons. In a magnetic field the unsaturated bonds can absorb a photon from microwaves, which can be measured and further analyzed [16–20]. Additional theoretical information on the atomic structure of possible defect configurations can be obtained from ab initio atomistic simulations using density functional theory (DFT) [21–23].

The defects identified to be responsible for the MOS device reliability can be generally classified into interface states and so called border traps. The interface states are commonly associated with P_b centers where several variants, depending on the crystal orientation, exist [25, 26]. While only one variant of P_b centers is available in (111) orientated Si/SiO_2 interfaces, two variants labeled P_{b0} and P_{b1} centers can be found in (100) orientated interfaces. A common property of all P_b centers is their amphoteric nature, meaning that their density of states distributions comprise two disjunctive peaks, one in each half of the band gap. The class of border traps includes for example the E' centers, which have been identified using ESR experiments, and can act as hole traps in pMOS transistors [19, 27]. Other studies suggest defects

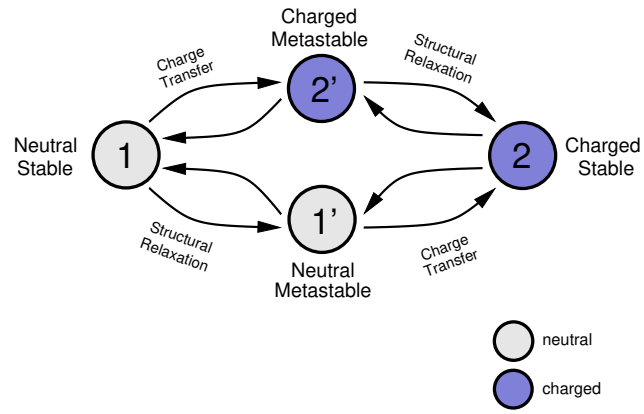

Fig. 3: To explain the charge trapping kinetics of single defects, i.e. their temperature and bias dependent charge capture and emission times, the four-state NMP model is regularly used. In general, the model considers two stable states 1 (neutral) and 2 (charged) and two metastable states 1′ and 2′. These states enable an accurate description of the observed bias and temperature dependence of charge capture and emission times.

involving hydrogen, namely defects in the hydrogen bridge configuration [28, 29] or hydroxyl E' centers [1] being suitable candidates for border traps too.

An important property of a suitable defect candidate in that regard is that its so-called charge transition level (CTL) lies within the active energy region (AER) of the respective measuring sequence, as shown in Figure 2 for electron and hole trap candidates. The borders of the AER are defined by the high and low gate bias which are used for characterization. Thus, at high gate bias conditions the energetic trap level E_T of the of a defect has to lie above the Fermi level of the carrier reservoir E_F in order that the defect can become charged, i.e. $E_T > E_F$. In case the low bias is applied and $E_T < E_F$ the defect can emit its charge and become neutral. Consequently, the CTL which is the trap level of the defect E_T has to lie inside the AER of the experiment in order to contribute to the measurement signal.

III. Modeling of Defects

There are essentially two approaches to explain the contribution of defects on the overall behavior of devices. These are empirical formalism, which represent the measured data in the form of purely mathematical expression, and often omit the physical origin of (single) charge trapping. The other approach is to make use of a stochastic charge trapping model which explains the trapping kinetics of individual defects. In order to provide a physics-based explanation for the charge states of the defects and the respective transitions between the model states, the non-radiative multiphonon (NMP) theory is used [30–32]. However, as the NMP model relies on Fermis golden rule and solving the complex equation system for real devices is computationally infeasible potential energy surfaces approximated by a harmonic oscillator are used in an 1D configuration coordinate diagram [23]. This approximation finally leads to the four-state defect model which has been successfully used to explain charge trapping in various Si technologies [33–35],

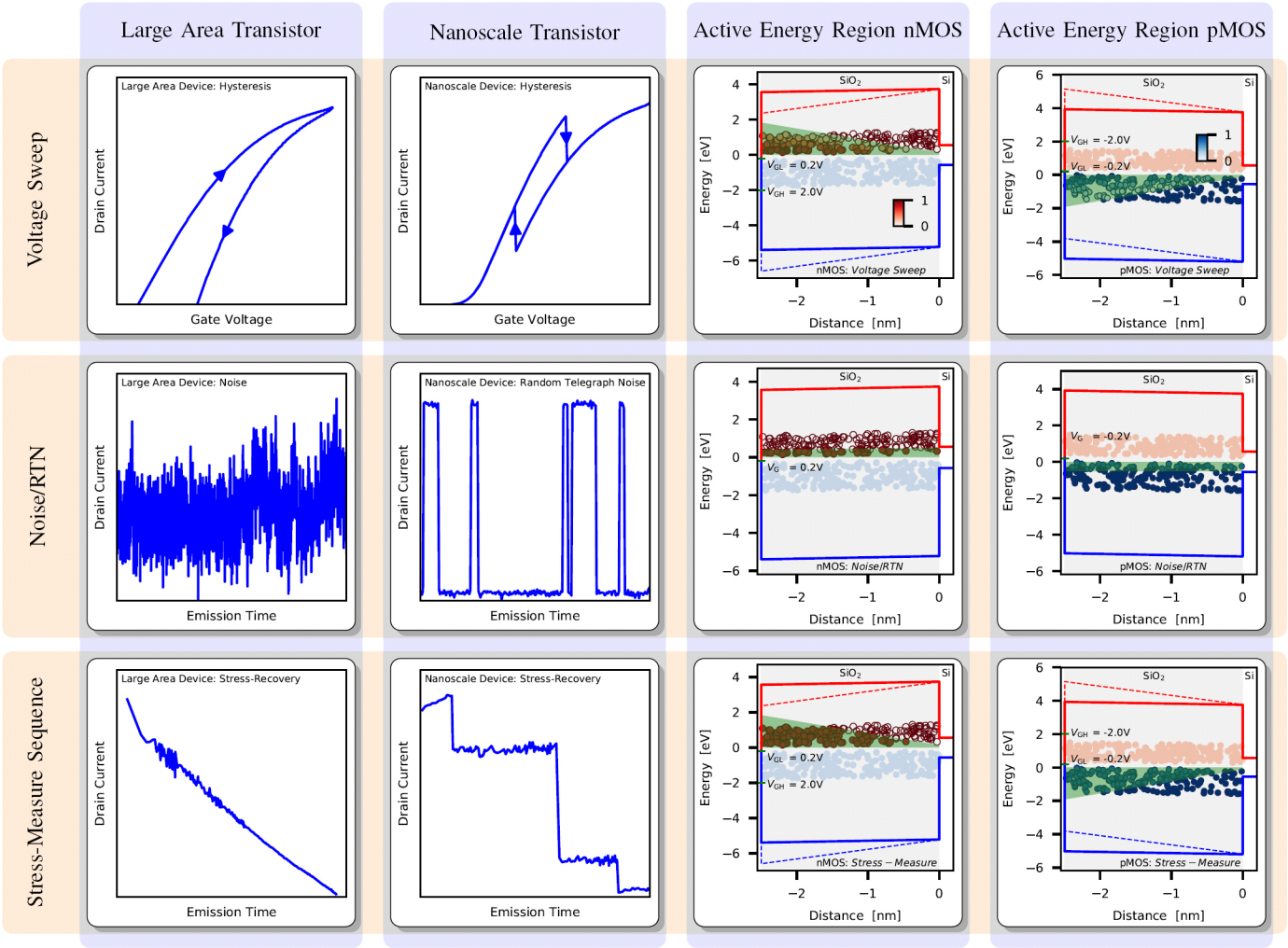

Fig. 4: When shifts of the threshold voltage or changes in the sub-threshold slope are studied typically **(top row)** voltage sweep measurements, **(middle row)** noise/RTN measurements and/or **(bottom row)** stress-recovery measurements are performed. A commonality of all techniques is that in **(first column)** large area devices continuous signals are observed, while on average the same behavior is visible in **(second column)** nanoscale devices, but here discrete steps appear in the measurement data. Each of these steps accord to a charge transition of a single defect. A difference of the three techniques is the number of defects which contribute to the measurement signal. The most fundamental prerequisite in that regard is that the trap level of the defects have to lie in the active energy region (AER, green area in the band diagrams) of the respective method. Only these defects can change their charge state during the experiment. The expansion of the AER is determined by the low and high bias used for the measurements. Note that although the same bias ranges are used for voltage sweeps and measure-stress-measure experiments, the number of defects which contribute to the current signal can significantly differ, as the sweep rate, i.e. the stress time, is an important parameter in that regard too. Defects with trap levels close to the higher boundary of the AER for voltage sweeps, only have less time to become charged compared to defects arranged closer to the lower boundary (indicated by the different brightness of the defects). In contrast, in measure-stress-measure experiments all defects have almost the same net stress time, i.e. the same amount of time for which their trap level lies below the channel Fermi level. The trap bands shown in the band diagram are according to recent consistent defect studies employing nMOS and pMOS transistors from various technology nodes [32].

see Figure 3, but also in devices employing wide band gap materials such as SiC [36] and GaN [37] and more exotic 2D materials [38].

IV. Device and Defect Characterization

As already has been said, the defects can change their charge state during device operation. This leads to altering of the surface potential along the channel and thus affects the current flux through the device. By performing electrical measurements the charge trapping of defects is deliberately triggered to study their effect on the device behavior at various biases, timings of the bias sequences applied at the device terminals and at different device temperatures. Typical characterization methods which are directly applicable to test structures range from $I_{\mathrm{D}}(V_{\mathrm{G}})$/hysteresis measurements [38–42], over noise measurements [38, 43] and measure-stress-measure experiments [11, 33, 44] to $C(V)$ measurements [45], see Figure 4. All of these methods have been initially developed around large area devices where the superposition of the electrical response of a multitude of defects is studied simultaneously as drift of the device parameters. However, with the availability of scaled transistors single defects manifest as

the main root behind the reliability issues in integrated MOS devices. While the number of defects per device N reduces with decreasing gate area A, i.e. $N \propto N_0/A$, the impact of a single defect on the device behavior gets pronounced in scaled nodes, i.e. $\eta \propto \eta_0 A$. As a consequence, the continuous current signals obtained from large area devices exhibit discrete steps in the current due to single charge capture and emission events in nanoscale devices, as also visible in Figure 4.

An essential difference between the measurement methods from Figure 4 is the number of defects and the energetic range of the trap levels of defects which can be accessed with the respective method:

(i) The alignment of the trap level of the defects with respect to the active energy region (AER) for charge trapping determines which defects can exchange a charge carrier during the experiment, and thus can contribute to a change in the drain-source current.

(ii) The timing of the sequence determines if a defect is provided enough time to change its charge state during the time while its trap level is below/above the Fermi level of the channel.

Note that both conditions are necessary for a single defect to contribute to the measurement signal. The area which is covered by the AER depends on the respective measurement technique and is defined by the applied biases. In the following the previously mentioned measurement techniques, their application for single defect characterization is discussed.

A. Voltage Sweep/Hysteresis Measurements

The most straight-forward approach to determine the shift of the threshold voltage of a MOS transistor is to measure a single $I_{\mathrm{D}}(V_{\mathrm{G}})$ characteristics after phases during which the stress biases has been applied, and the stress times have been iteratively increased, see Figure 5. From the $I_{\mathrm{D}}(V_{\mathrm{G}})$ curves the threshold voltage and sub-threshold slope can be determined very efficiently. However, as the charge transition times of defects are widely distributed in time, and not all defects in the corresponding AER see the same net stress time during a voltage sweep, this method tends to underestimate the drift of the threshold voltage. In order to suppress the impact of the voltage sweep on the ΔV_{th} ultra-fast $I_{\mathrm{D}}(V_{\mathrm{G}})$ setups which are capable to record a single $I_{\mathrm{D}}(V_{\mathrm{G}})$ withing a few microseconds only have been developed [46–49]. However, these techniques exhibit an uncertainty of at least a few mV of ΔV_{th} due to measurement noise, and thus their applicability is limited to large area devices or to devices which exhibit large drifts of V_{th} only. Although the $I_{\mathrm{D}}(V_{\mathrm{G}})$ contains more information on the device electrostatics than measure-stress-measure (MSM) experiments, their exact evaluation regarding charge trapping is very elusive.

An important parameter when measuring the $I_{\mathrm{D}}(V_{\mathrm{G}})$ characteristics is the selection of the bias ranges. For instance, $I_{\mathrm{D}}(V_{\mathrm{G}})$ measurements have been recently used to determine the permanent component of the threshold voltage shift [42]. In

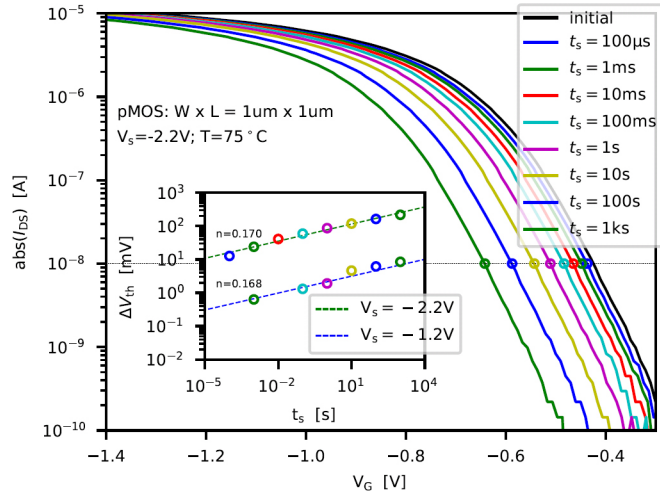

Fig. 5: One approach to approximate the shift of the threshold voltage after stress is to recorded $I_{\mathrm{D}}(V_{\mathrm{G}})$ characteristics after repeatedly applied stress cycles with increasing stress times. The threshold voltage shift can afterwards be determined by using a constant current criteria (dashed line). The inset shows that the observed increase of the absolute value of the threshold voltage follows a power law.

this experiments a notable impact on the measured permanent ΔV_{th} for different sweep ranges used for the gate bias is observed. The more the gate bias is shifted towards accumulation the smaller the permanent component gets, which is a consequence of the large amount of charge being remove during accumulation. The selected gate bias ranges are also very important when the hysteresis of the voltage sweeps are studied. This is especially the case for material systems which exhibit high defect densities, such as high-k materials or technologies employing wide band gap materials [40, 50, 51]. The width of the hysteresis has been observed to be very sensitive to the sweep bias range and duration of the up-and down-sweep. In order to observe a hysteresis the defects which become charged during the up-sweep should not have enough time to discharge during the down-sweep.

Nonetheless, $I_{\mathrm{D}}(V_{\mathrm{G}})$ measurements provide a very efficient way to gather statistical meaningful information from many thousands of transistors within a reasonable time. For instance, by using dedicated transistor arrays stress-$I_{\mathrm{D}}(V_{\mathrm{G}})$ experiments enable to collect information on the distribution of changes of V_{th} and carrier mobility after BTI or HC stress [41].

The voltage sweeps can also be applied to nanoscale devices. In such devices where the behavior is dominated by discrete charge capture and emission events of single defects, such transitions are also clearly visible in the $I_{\mathrm{D}}(V_{\mathrm{G}})$ characteristics and hysteresis [38, 42]. However, as the charge transition times strongly depend on the position of the trap level w.r.t. the device Fermi level, which changes during a voltage sweep, the extraction of the average charge capture and charge emission time from voltage sweeps is pretty elusive. For this noise measurements and MSM experiments which are discussed next are preferred.

B. Analysis of Noise in MOS Transistors

To study the noise in MOS transistors the power spectral density (PSD) of the current signal is usually analyzed. At low frequencies the PSD typically follows a $1/f^n$ behavior, with an exponent $n \approx 1$ [52]. McWorther proposed the observed $1/f$ behavior to be mainly due to the superposition of many Lorentzian-like spectra, $1/(1+(f/f_c)^2)$, of random telegraph noise (RTN) signals [53]. In principle RTN signals can be identified as discrete transitions of the ΔV_{th} between two distinct levels, see Figure 4 (middle row). Each level can be attributed to either the charged or neutral state of the defect. If one assumes many defects with log-uniformly distributed corner frequencies f_c, i.e. charge capture and emission times, the sum of spectra of the RTN signals finally gives the $1/f$ characteristic of large area devices [53]. With the availability of nanoscale devices RTN signals of single defects have been studied and the theory could be confirmed as the physical origin of $1/f$ noise in MOS transistors [54, 55].

From the modeling perspective, RTN signals can be described by a simple two-state defect model, where each charge state is ascribed to one state of the model. In order to provide a physics-based explanation for the two charge states, the NMP theory is used [31, 43]. In the case of RTN signals analytical expressions for the charge capture and emission times and their dependence on the gate bias and trap depth can be derived. However, RTN is observed to be more complicated than expected from a simple two-state defect. For instance anomalous RTN signals, where phases of RTN activity are interrupted by phases of inactivity, have been observed. Such a behavior requires a three-state model for its proper explanation. Quite recently, the superposition of two RTN signals where a defect only produces RTN when a second defect is active has been measured in GaN HEMT devices [37]. The modeling of this behavior is by no means unique. It can be either due to a complex state defect with four states, or due to two regular RTN defects with two states each, which are electrostatically coupled. After thorough analysis of the data and performing device simulations it turned out that signal is produced by two coupled defects [37]. Such intricate features of defects are only visible when individual defects are investigated, but are essential for correct physical models.

An significant advantage of RTN signals is that the charge capture and emission times can be directly extracted. As RTN is typically recorded under equilibrium conditions this technique is especially advantageous for material systems where stable operating conditions are difficult to achieve, as it is the case for wide band gap technologies or device employing 2D materials. However, the charge transition times are widely distributed, and thus RTN analysis will miss the majority of the defects. The very fast defects will only produce an average contribution to the measured current and the slow defects will not fit into a typical experimental window. In order to enhance the measurement window for single charge trapping measure-stress-measure experiments can be applied.

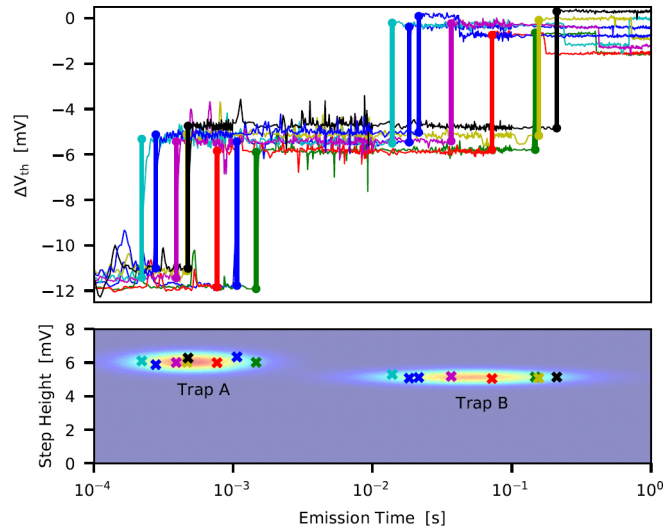

Fig. 6: (**top**) Discrete steps are visible in the recovery traces of nanoscale devices. After the recovery traces are analyzed the discrete ΔV_{th} steps (**bottom**) are collected in the emission time versus step height plane. These (τ_e, d) plots are called spectral map and visualize the emission time distribution of the single defects at a defined bias, stress time and device temperature. As can be seen, the single emission events form clusters which are the fingerprint of a single defect.

C. Measure-Stress-Measure Experiments

The deep level transient spectroscopy (DLTS) is an established method to detect a broad variety of traps in semiconductors [57]. DLTS makes use of short voltage pulses to shift a certain number of traps below the Fermi-level and to initiate a change in their charge state. The same principle is used within the recently proposed time-dependent defect spectroscopy [30]. In TDDS defined stress pulses are applied to the gate of a MOSFET to charge defects and afterwards during the recovery phase the defects can emit their charge. If the device are small enough discrete charge transitions become visible in the recovery traces, as shown in Figure 6 (top). As single charge trapping is of stochastic nature the MSM experiment is repeatedly performed using the same stress/recovery biases and times, as well as at the same device temperature. Afterwards the recovery traces are analyzed for discrete charge transitions, which are then plotted in the emission time versus step height plane, i.e. (τ_e, d). As can be seen from the so called spectral map from Figure 6 (bottom) the collected charge emission events tend to form clusters. Each cluster can be interpreted as the fingerprint of a single defect and enables to determine the average charge emission time by calculation of the mean of all emission events which are assigned to the respective cluster

$$\tau_e = \frac{1}{N_e} \sum_i \tau_{e_i}.$$

In this way the charge emission time can be extracted for different recovery biases and temperatures. In contrast to the charge emission time, the charge capture time cannot be extracted directly from a single TDDS measurement. To ex-

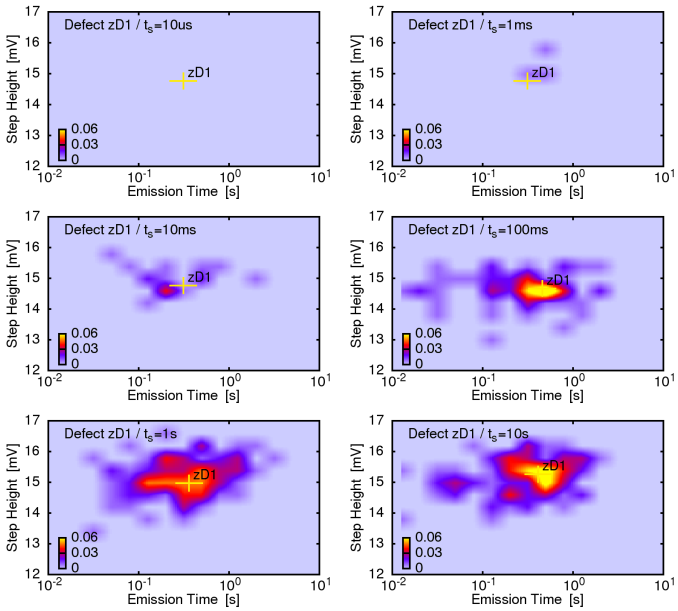

Fig. 7: The spectral maps show that with increasing stress time the cluster gets brighter, indicating that the number of emission events increases with stress time. From the spectral maps the occupancy can be directly calculated for each stress time as the ratio between the number of emission events and the number of traces measured.

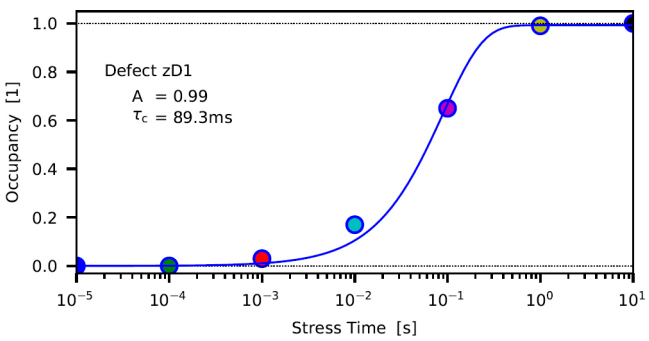

Fig. 8: The occupancy extracted from the data shown in Figure 7 clearly exhibits an exponential dependence on the stress time. This allows to estimate the charge capture time for a certain stress bias and device temperature.

tract the charge capture time MSM sequences with increasing stress times are applied. The expectation value of the defect occupancy O, i.e. the probability of a defect to become charged during stress, increases with stress time t_s

$$O(t_\mathrm{s}) = A(1 - \mathrm{e}^{-t_\mathrm{s}/\tau_\mathrm{c}})$$

with A the value of the occupancy obtained after indefinitely long time of stress. This trend can be seen in the spectral maps from Figure 7 as the visibility of the cluster becomes clearer towards increasing t_s. The occupancy at a certain stress time can be extracted from the spectral maps as the ratio between the number of emission events and the number of measured traces ($O|_{t_\mathrm{s}} = N_\mathrm{e}/N_\mathrm{N}$). In Figure 8 the formula for the occupancy is applied to the results from the spectral maps shown in Figure 7 and enables to extract the stress time for a certain stress bias and device temperature.

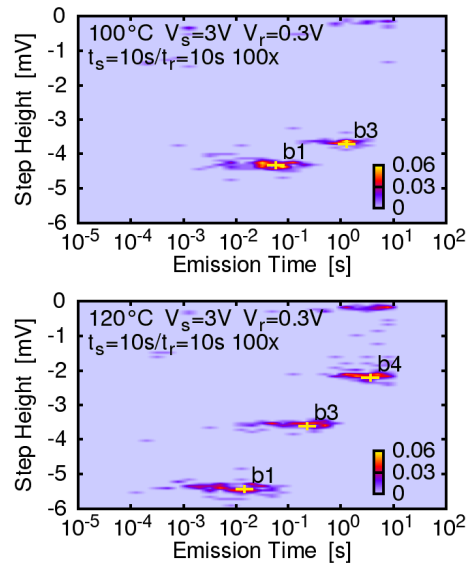

Fig. 9: The spectral maps for one device measured at two different temperatures are presented to demonstrate the temperature of single defects. (**top**) Two defects (namely defects b_1 ,b_3) are visible in the spectral map. (**bottom**) The charge emission times of these defects move towards lower emission times at higher temperature. Furthermore, new defects (as for instance defect b_4) can be shifted into the measurement window when the device temperature is increased.

In addition to the previously mentioned variation of the stress time to extract the charge capture time other experimental parameters can be deliberately adjusted to collect information of the trapping kinetics of single defects:

(i) Charge trapping is observed to be a strongly temperature activated process. The larger the device temperature becomes the faster charge capture and charge emission proceeds, as can be seen in Figure 9.

(ii) By increasing/decreasing the stress bias, the charge capture time of a defect changes. The larger the absolute value of the stress bias becomes the more likely a defect will become charged during the stress phase, and thus the charge capture time decreases/increases.

(iii) By varying the recovery bias, the emission time of a defect can change. In principle, the larger the absolute value of the recovery bias gets it will be for a defect more unlikely the defect will emit its charge during the recovery phase, and thus the emission time should increase (this behavior is referred to switching oxide traps as shown in Figure 10). However, by studying single defects it has been observed that defects can also exhibit recovery bias independent charge emission times, which are referred to fixed oxide traps. From a modeling point of view it is important that a suitable defect model can describe both characteristics.

By varying the aforementioned experimental parameters the charge trapping kinetics of single defects can be extracted over a wide bias and temperature range, as shown for a switching trap in Figure 10. To simulate the charge transition times of the

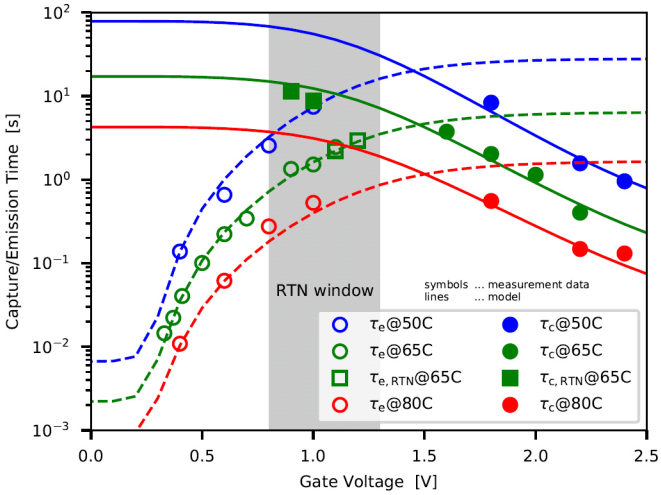

Fig. 10: Combining the analysis of RTN signals and TDDS the gate voltage dependence of the charge capture time τ_c and the charge emission time τ_e of single defects can be extracted. The charge trapping kinetics for the defect shown exhibits bias dependent charge capture and emission times, which is typically referred to as switching oxide traps. As can be seen, the NMP model nicely explains the observed trapping kinetics.

defect our four-state NMP model has been used in combination with the drift diffusion based device simulator MinimosNT. As can be seen, our simulations nicely explain the experimental data. With this calibrated toolset in hand one can now make accurate lifetime predictions for various operating conditions.

V. Conclusions

Charge trapping of single defects is the main root of reliability challenges prevalent in modern transistor technologies. Typically large area devices are investigated which exhibit a continuous drift of the MOS transistor parameters like the threshold voltage. This drift is caused by the superposition of many defects. However, with the availability of nanoscale devices, the charge trapping kinetics of single defects can be studied. The understanding of the bias and temperature dependence of the charge transition times of single defects is of particular importance for the development of accurate defect models enabling lifetime predictions for different operating conditions. For the characterization of single defects random telegraph noise measurements but also measure-stress-measure experiments can be performed. While the former is carried out when the device is in its equilibrium the latter aims at stressing the device in a targeted manner in order to deliberately charge defects. The difference of both methods is the active energy region of trap levels which can be accessed. When combined, the charge trapping kinetics of single defects can be efficiently extracted over a wide bias and temperature range.

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