Improved PBTI Reliability in Junction-Less FET Fabricated at Low Thermal Budget for 3-D Sequential Integration

Zhicheng Wu, Jacopo Franco, Anne Vandooren, Ben Kaczer, Philippe Roussel, Gerhard Rzepa, Tibor Grasser, Dimitri Linten, and Guido Groeseneken

***Abstract*—Junction-less FETs are used as top-tier devices in a 3-D sequential integration. Due to the low thermal budget allowed in the 3-D integration, conventional inversion mode FETs show extremely poor BTI reliability. In contrast, a junction-less FET shows improved BTI reliability, which is attributed to the reduced oxide electric field of operation. We observe that the reliability of junction-less FETs can be further improved by increasing the channel doping and/or the channel thickness. Correspondingly, a tradeoff exists between performance (sub-threshold slope, carrier mobility), reliability, and variability. This tradeoff is verified in both planar/FinFET structures and can serve as a device optimization matrix. Furthermore, we use the non-radiative multi-phonon (NMP) theory, as implemented in the imec/T.U. Vienna BTI simulation framework "Comphy," to investigate the degradation kinetics and show that the stress/recovery traces measured in inversion mode and junction-less nFETs can be reproduced with the same set of oxide defect parameters. This observation confirms that the reliability improvement in junction-less devices is inherent to their specific operation mode and not related to the different fabrication flows compared to standard inversion mode devices. Based on the calibrated Comphy model, we perform BTI lifetime projections, exposing for junction-less devices a substantial deviation from the commonly used power-law voltage acceleration.**

***Index Terms*—3D sequential integration, bias temperature instability, junction-less FET, semiconductor device reliability, variability, mobility, lifetime projection.**

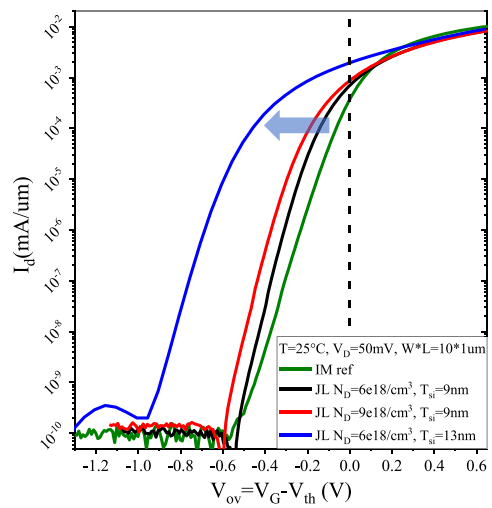

Fig. 1. Transfer characteristics for IM ref. and JL planar nFETs with different channel doping and channel thickness, I_D is plotted as a function of $V_{ov} = V_G$-V_{th}, where V_{th} is estimated with the maximum transconductance method. The higher the channel doping, and/or the thicker the channel, the more voltage is needed to deplete the channel majority carriers and therefore switch off the device (the arrow indicates the trend from IM to JL, from lower doping/thinner channel JL to higher doping/thicker channel JL).

I. Introduction

3D SEQUENTIAL integration is a very promising route to continue increasing the circuit density and functionality. In this integration scheme, a second-tier (top tier) is stacked and processed on top of a fully-processed device bottom tier. Since the bottom tier will also be subjected to thermal steps required for top tier fabrication, any additional high temperature step for the top tier fabrication will require additional thermal stability of the bottom tier. The most critical challenge of a 3D sequential integration is therefore the fabrication of functional top tier devices within stringent thermal budget restrictions.

Process thermal budget has a crucial role for curing oxide defects and demonstrating sufficient PBTI reliability [1]. To circumvent the thermal budget limitations for top tier processing in 3D sequential integration, junction-less (JL) transistor is investigated as a promising low thermal budget device for top tier. The JL device was proposed by Colinge *et al.* in 2010 as an alternative to conventional inversion mode FETs [2], which operates instead in the MOS accumulation regime. The channel current is sustained by the bulk majority carrier, and therefore a low oxide field is required for operating the device in on-state, while a negative oxide field is applied to deplete the channel and switch off the current flow [3], [4].

In this work, we show that the BTI reliability in low thermal budget planar JL outperforms its inversion mode (IM) counterpart and can be further improved with a higher channel

Manuscript received February 25, 2019; accepted March 18, 2019. Date of publication March 21, 2019; date of current version June 5, 2019. *(Corresponding author: Zhicheng Wu.)*

Z. Wu and G. Groeseneken are with Device Reliability and Electrical Characterization Group, imec, 3001 Leuven, Belgium, and also with ESAT-MICAS, KU Leuven, 3001 Leuven, Belgium (e-mail: zhicheng.wu@imec.be).

J. Franco, A. Vandooren, B. Kaczer, P. Roussel, and D. Linten are with Device Reliability and Electrical Characterization Group, imec, 3001 Leuven, Belgium.

G. Rzepa and T. Grasser are with the Institue for Microelectronics, Technische Universitat Wien, 1040 Vienna, Austria.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TDMR.2019.2906843

1530-4388 © 2019 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

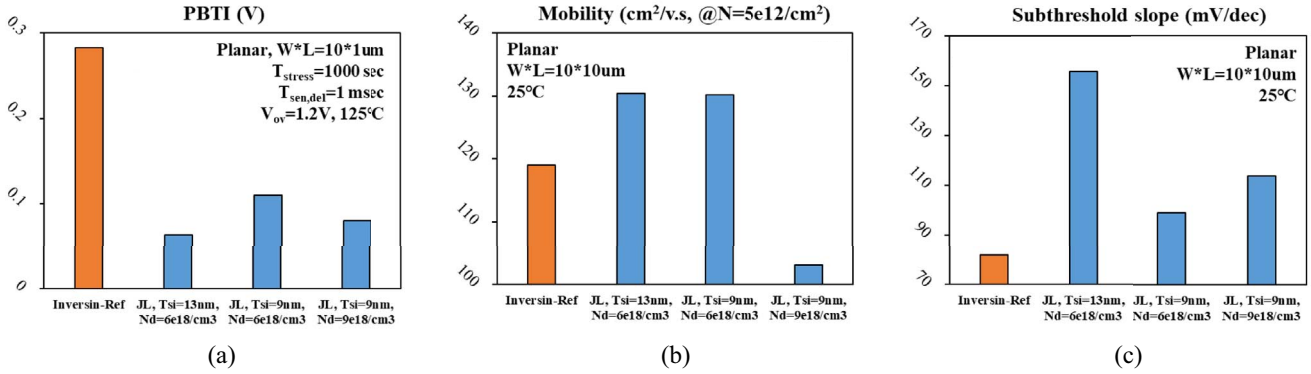

Fig. 2. Reliability and performance metrics for planar JL nFETs, includes threshold voltage shift (ΔV_{th}), long channel mobility μ and subthreshold slope (SS) in long channel. The inversion mode device is used as a reference. Values are median numbers measured on at least 10 nominally identical devices.

doping as well as a thicker channel. While a higher channel doping results in lower mobility and larger variability, a thicker channel degrades the subthreshold slope; therefore, a trade-off exists between performance, variability and reliability. This trade-off is verified in both planar and FinFET structures; however, the latter one shows reduced sensitivity to channel doping, as the channel depletion width is limited by the (half) fin width itself. With the simplified two-state NMP model, as implemented in the imec/T.U. Vienna BTI simulation framework "Comphy", we further show that the stress/relax dynamics in planar nFETs can be fully modeled with the same set of oxide defect parameters for both JL and IM planar nFETs.

II. Experimental

Planar and FinFET JL nFETs, as well as planar IM reference ("ref."), were fabricated on 300mm wafer with a gate-last process, with nominally identical gate stack ($SiO_2/HfO_2/TiN$). All devices featured an EOT of $\sim$ 0.95nm. The linear transfer characteristics of large area planar nFETs are shown in Fig. 1, by shifting the corresponding threshold voltages (extracted with the maximum transconductance method) to 0V for easier comparison. A trend can be clearly identified in Fig. 1: as the channel doping density or the channel thickness increases, more voltage is needed to pinch-off the channel and to reach a similar off-state current level. This observation yields the first consideration: due to the accumulation mode operation, both channel doping and channel thickness play important roles in the electrostatics of JL devices.

The eMSM technique is used to characterize BTI reliability [5]. Large area structures are used to minimize stochastic variations [6]. In Fig. 2 (a), the BTI-induced threshold voltage shift (ΔV_{th}) in planar nFETs was evaluated at fixed $V_{ov} = 1.2$V ($t_{stress} = 1$ ksec) at 125°C. All JL planar devices show reduced PBTI with respect to the IM counterpart; thicker channel and higher channel doping further improve the PBTI reliability of the JL. The latter observation is particularly interesting, as for IM devices a higher channel doping results in a larger oxide electric field at a given stress voltage due to the larger channel depletion charge [7].

Split-CV measurements were performed on long channel devices to estimate the carrier mobility. In order to visualize the intrinsic correlation between the device structural

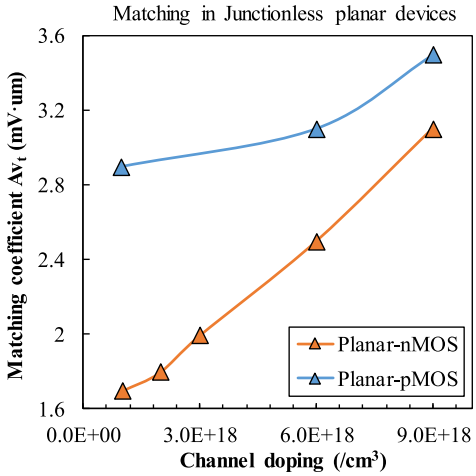

Fig. 3. Matching coefficient A_{Vt}vs. channel doping for planar devices [9]. A_{Vt} is obtained on matched pairs and shows increasing trend (i.e., larger V_{th} variability) with respect to the channel doping for both planar nMOS and pMOS, mainly due to random dopant fluctuation (RDF).

design (channel doping and thickness) and the device reliability (PBTI) and performance (carrier mobility, subthreshold slope), Fig. 2 summarizes the ΔV_{th} degradation, the long channel device mobility μ at fixed mobile charge density ($L_G = 10$um, $N = 5e12/cm^2$), and the long channel device subthreshold swing (SS, $L_G = 10$um, for excluding any different short channel effects and demonstrate the intrinsic trade-off): a thicker channel improves the reliability, but significantly degrades SS, which is due to the reduced gate electrostatic control over the channel portion that is far away from the HK/SiO_2-Si interface; on the contrary, a higher channel doping can also improve the reliability with a limited SS penalty; however, doping impacts the carrier transport, due to the increased impurity scattering [8], as can be seen from the lower mobility value extracted. Furthermore, since variability is the major concern in modern circuits exploiting nanoscale devices, the increasing device V_{th} mismatching for increasing channel doping further complicates the trade-off and impose more constraints on the junction-less device optimization (Fig. 3).

Junction-less FinFET devices (n-type) are also investigated for possible implementation in advanced nodes. Similar to Fig. 2, the reliability and performance metrics for different channel doping are summarized in Fig. 4. Similar trends can

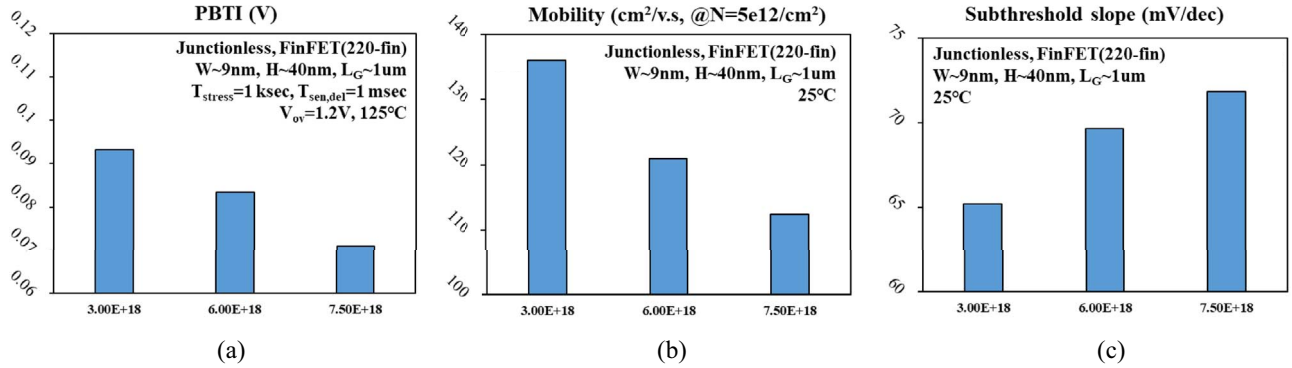

Fig. 4. Reliability and performance metrics for JL FinFET (n-type). The slightly better PBTI reliability in FinFET (N_D = 6e18/cm^3) compared to its planar counterpart [Fig. 2 (a), N_D = 6e18/cm^3 and T_{si} = 9nm] is mainly due to relative higher thermal budget during post-gate processing. No inversion mode reference is included in this figure. Values are median numbers measured on at least 10 nominally identical devices.

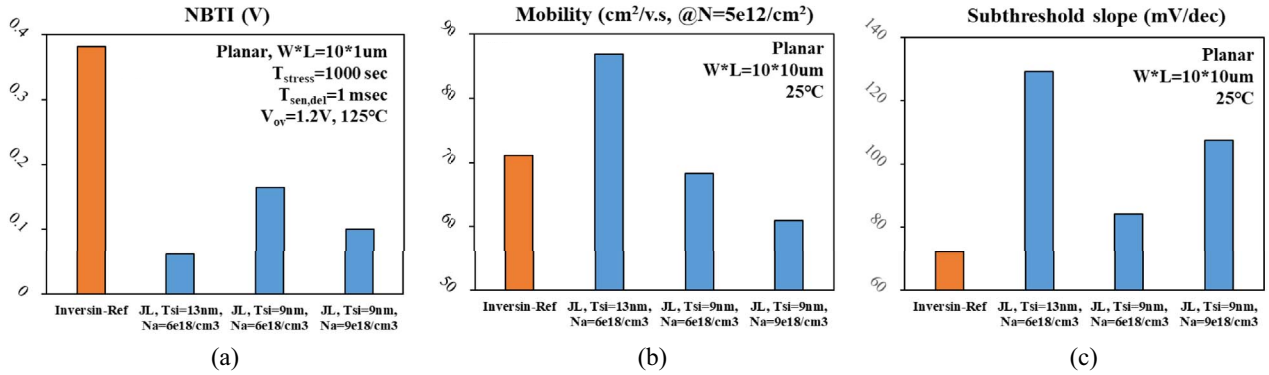

Fig. 5. Reliability and performance metrics for planar JL pFET, showing similar trends as in planar nFET (see Fig. 2). The pFET shows higher sensitivity of mobility to channel thickness reduction, which might be attributed to the remote scattering from the SiO_2 buried oxide impacting the carrier transport more in pMOS than in nMOS. The inversion mode device is used as a reference (baseline). Values are median numbers measured on at least 10 nominally identical devices.

be observed: a higher channel doping improves the reliability but degrades mobility as well as SS. It can be seen in Fig. 4 (c) that, unlike planar devices which show large SS degradation at high doping, FinFETs show a limited SS degradation at high doping.

Finally, for concluding the optimization space (trade-off) in junction-less devices, planar JL pMOS with same gate stack are also investigated (Fig. 5). Since we have showed the performance, reliability and variability trade-off to be similar in planar and FinFET n-channel devices, it is reasonable to expect similar trends also for p-channel JL FinFETs. The variability enhancement for planar pMOS with increasing doping density is also shown in Fig. 3.

III. Reliability Modeling and Discussion

In previous Section, the fundamental trade-off between performance, reliability and variability in junction-less devices has been demonstrated. In this Section, we explore the origin of improved BTI reliability in JL device with respect to its inversion mode counterpart, as documented in Fig. 6, where all JL devices show considerable PBTI reliability improvement compared to IM device, while channel doping and channel thickness variations in JL devices further modulate their PBTI reliability.

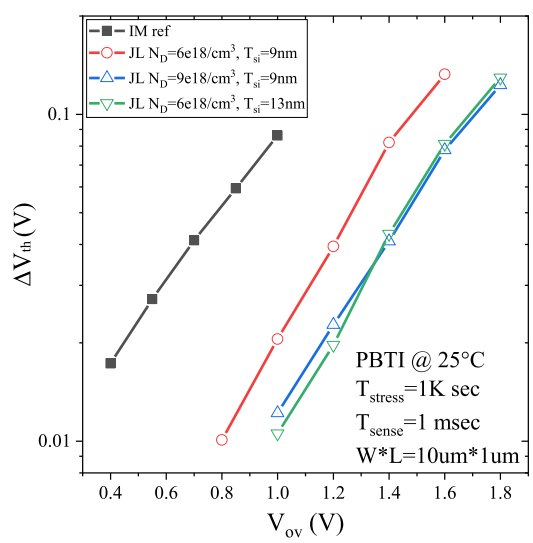

Fig. 6. PBTI V_{th} shift (ΔV_{th}) evaluated at t_{stress} = 1 ksec (T = 25°C) vs. gate overdrive voltage (V_{ov} = V_G-V_{th}) for IM ref. and JL planar nMOS. JL devices show improved reliability compared to the IM ref. Higher channel doping, or/and thicker channel further improve the reliability in JL.

To demonstrate that the reliability improvement in JL devices fully results from the shift of operation regime, i.e., from inversion mode to accumulation mode, and to understand the impact of channel doping and channel thickness on the BTI

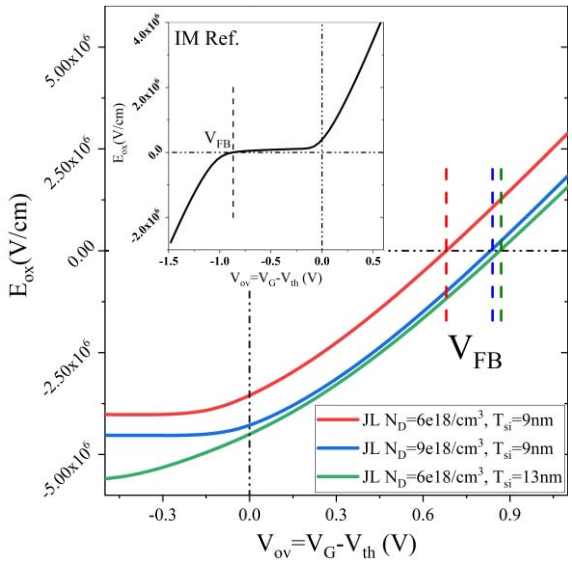

Fig. 7. Oxide electric field calculated from measured capacitance and voltage curves at 25°C, according to [11], [14]. Oxide electric field is significantly lower in JL planar nMOS compared with IM counterpart (in inset).

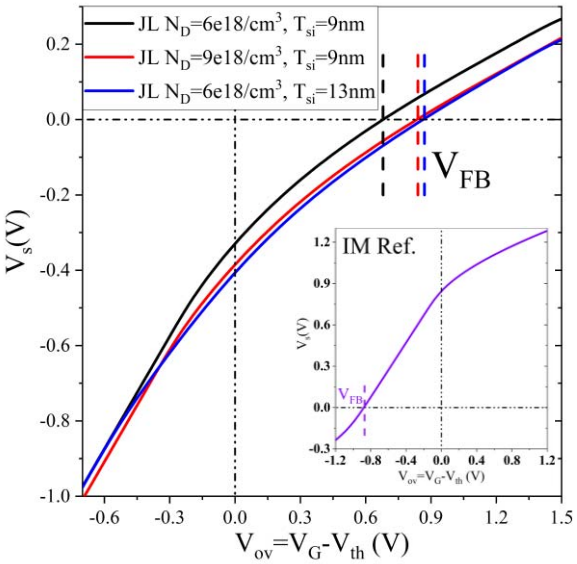

Fig. 8. Surface potential (Ψ_s) and flat-band voltage (V_{fb}) calculated from measured capacitance and voltage curves at 25°C for JL planar nMOS (IM ref. is shown in the inset), according to [11], [14].

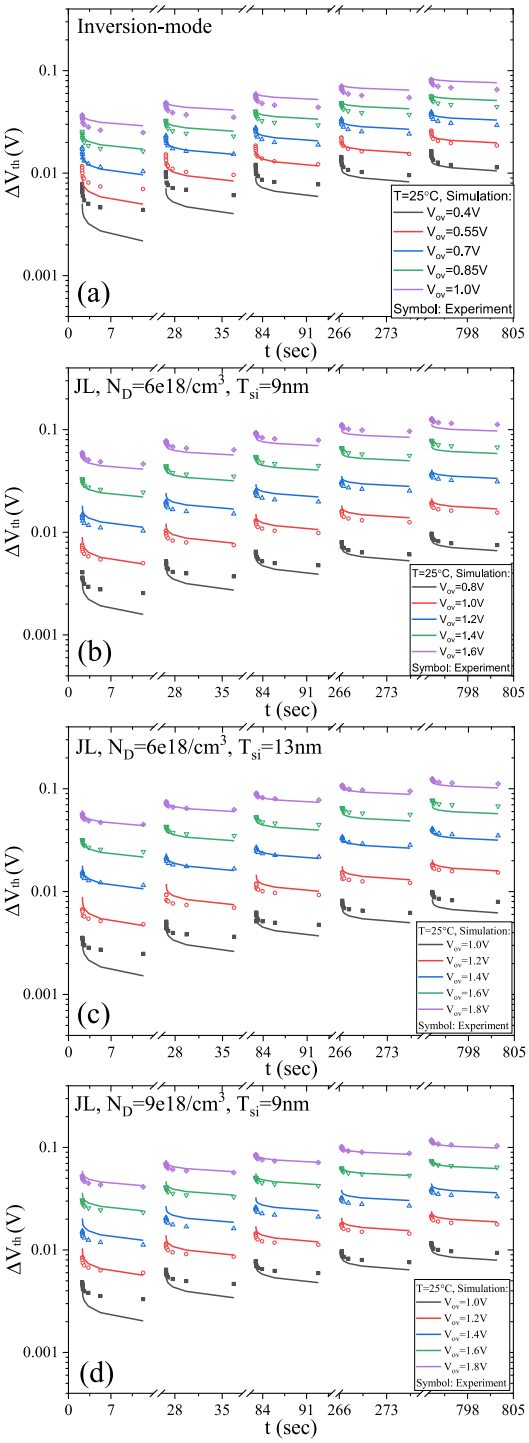

Fig. 9. BTI Stress/recovery kinetics is modeled with Comphy. A single set of modeling parameters (defect band configurations) is used for all IM ref. and JL planar nMOS, while the surface potential vs. V_G relation pertaining to each device type is considered (see Fig. 8). Simulated recovery traces (solid lines) after individual stress phases of increasing duration at various voltages show good agreement with the measurement data (symbols). Note: if any difference in the fabrication process of JL and IM would have resulted in different oxide quality, it would not be possible to describe all the BTI trends with a single set of defect parameters.

reliability of JL devices, we carefully model the capacitance vs. gate voltage curves for IM and JL planar nFETs in Fig. 6 (same devices as also listed in Fig. 2) to extract the oxide electric field as well as the surface potential relations to the applied gate voltage.

We have chosen to perform this detailed study on planar n-channel devices for a variety of reasons: 1) a planar structure allows to use the 1-D Poisson solver implemented in the CVC Hauser tool [10], to accurately model the C-V characteristics; on the contrary, for a FinFET structure one would need to perform a complete TCAD simulation and also account for geometric effects; 2) since the Debye length is inverse proportional to the channel doping [11], for lowly doped channel, the summation of Debye length and depletion region width at back interface may already be comparable with channel thickness (in planar device) or half of the fin width (~4.5nm, in FinFET), and therefore Eq. (1) would no longer estimate correctly the flat-band voltage; 3) nMOS PBTI is dominated by

high-k defects only [12], which reduces the Comphy modeling complexity compared to pMOS and ensures accurate lifetime projections even when model parameters are calibrated with a limited number of stress measurements as shown here [13].

For the IM ref., the electrostatics is modeled using CVC Hauser tool. For JL devices, oxide electric field (E_{ox}) and surface potential (ψ_s) are extracted based on the analytical method proposed in [14] (which neglects quantum mechanics corrections). Of critical importance is to estimate accurately the flat-band (V_{FB}) voltage for JL devices, for which we use Eq. (1) proposed by [11]. It is worth noting that Eq. (1) does not rely on accurate knowledge of channel doping concentration:

$$V_{FB} = \frac{C'C}{C'} + \frac{3}{2}\left(\frac{C}{3V_{therm}|C'|}\right)^{1/2} - 3 \quad (1)$$

Fig. 7 and Fig. 8 show the extracted E_{ox} and surface potential Ψ_s vs. V_{ov}. A reduction of E_{ox} is observed in JLs compared to IM ref. at same gate overdrive, which can explain the improved reliability in JLs. Another unique characteristic of JL devices is that: for the weak on-state range $V_{th}<V_g<V_{fb}$, the polarity of E_{ox} is opposite as compared to the strong on-state range $V_g>V_{fb}$; moreover, it is interesting to note that in this voltage range ($V_{th}<V_g<V_{fb}$), a larger V_{ov} results in a smaller $|E_{ox}|$. This conclusion agrees with our experimental observation: when JLs are stressed below certain voltages (in our case, this voltage was always roughly in-line with the calculated V_{fb}), no ΔV_{th} can be measured (see Fig. 6).

To prove that the same oxide defects are responsible for the different BTI stress/recovery kinetics measured in JL and IM devices, we use the compact physical BTI modeling tool "Comphy" [13], in which the capture/emission of defects is modeled with a simplified two-state Non-radiative Multi-Phonon (NMP) model. For all four devices listed in Fig. 6, the BTI measurement results can be fully reproduced with the same set of oxide defect parameters, by simply plugging in the correct surface potential to V_G relation extracted experimentally for each device type. A good agreement between measurement and simulation in Fig. 9 validates the hypothesis that the same oxide defects are responsible for PBTI in both IM and JL devices, while the latter one benefits from the reduced E_{ox} at a given gate overdrive voltage. It is also important to underscore here that for all four cases in Fig. 9, the defect bands parameters used for the Comphy simulations are identical, as listed in Table I.

Fig. 10 depicts the calculated trap occupancy at $V_{ov} = 1.12$V for both IM and JL devices, according to the calibrated defect parameters (Table I): despite the large number of High-K traps as well as their relatively low energy level with respect to the channel Fermi level (related to the low process thermal budget [15]), a significant reduction of occupied traps is obtained by moving from inversion-mode to accumulation-mode channel operation. This suggests that JL devices are potentially more suitable for low thermal budget 3D sequential integration, as they relieve the oxide quality requirements for sufficient PBTI reliability, circumventing one crucial challenge related to the thermal budget limitations.

Based on the good agreement between measurement and simulation in Fig. 9, we perform the lifetime projection using Comphy and compare it with the commonly used power law extrapolation. As can be seen in Fig. 11, the result further supports our previous observation [16]: empirical lifetime projection with power law is pessimistic as compared to physics-based BTI projection. Furthermore, in the particular case of JL, a power law extrapolation would induce a paradox: for all JL devices investigated in this work, under the criteria of $\Delta V_{th} = 30$mV at 25°C for 10-year operation, the maximum operating overdrive projected with a simple power-law would be below the calculated flat-band voltage (i.e., at a negative oxide field), where no measurable ΔV_{th} was observed experimentally. Therefore, we notice that BTI extrapolation based on power-law of the stress gate voltage or overdrive voltage are fundamentally unsuitable for accumulation-mode junctionless devices, while a physics-based extrapolation approach,

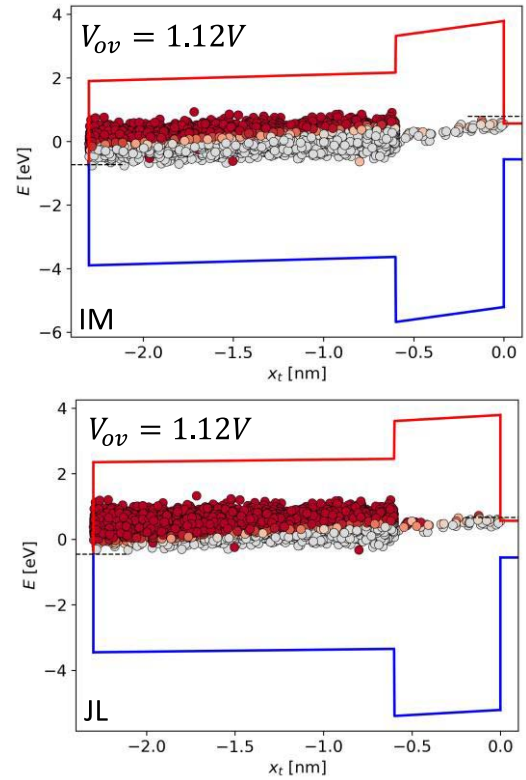

Fig. 10. Trap occupancy for IM ref. (top) and JL planar nMOS (bottom, $N_D = 6e18/cm^3$, $T_{si} = 9$nm) simulated with same defect bands configuration (Table I) and corresponding surface potential (Fig. 8). Trap occupancy probability at $V_{ov} = 1.12$V varies from 1 (white, occupied) to 0 (red, non-occupied). At the same stress condition, JL shows much less occupied traps compared to IM ref. solely due to the reduced operating electric field.

TABLE I
MODELING PARAMETERS (DEFECT BAND CONFIGURATION [13]) USED IN FIG. 9

	Unit	HfO_2	SiO_2
$<E_T>$	$[eV]$	0.68	0.54
σ_{E_T}	$[eV]$	0.22	0.11
N_T	$[cm^{-3}]$	4.61×10^{20}	8.88×10^{18}
$<S>$	$[eV]$	2.00	2.75
σ_S	$[eV]$	0.57	1.10
R	[1]	0.41	0.83

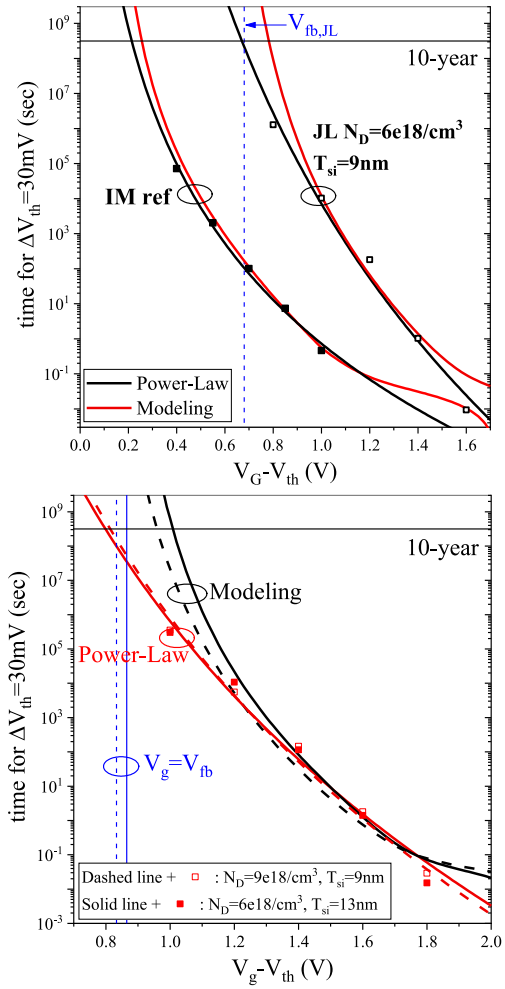

Fig. 11. Lifetime projection (25°C) comparing power-law and physics-based modeling approaches: symbols represent the measured data (see Fig. 9). Top: improvement in JL as compared to the IM ref., note the power law approach shows slightly pessimistic lifetime in IM ref. compared to Comphy modeling. For the JL device, the power law approach projects a maximum 10-year operating overdrive below the flat-band voltage. Bottom: higher channel doping and thicker channel further increase the maximum operating overdrive: power-law approach fails to distinguish between two very similar devices and again projects to voltage below flat-band, while the modeling approach projects different maximum operating overdrives for those two devices, which are all above flat-band and in-line with the trend in Fig. 6 (low overdrive range).

including an accurate estimation of the oxide electric field, guarantees universal applicability irrespective of the device operating modes.

IV. Conclusion

In this work, the fundamental trade-off between performance (mobility, subthreshold slope), reliability and variability has been demonstrated in n- and p-channel junction-less devices, including both planar and FinFET structures: in this device family, higher channel doping improves the BTI reliability, but degrades the performance, and exacerbates the variability concern; a thicker channel improves the BTI reliability, but significantly degrades the subthreshold slope. A reliability-oriented optimization (higher doping and/or thicker channel), which degrades performance, can be compensated by exploiting FinFET structures, which provides additional electrostatic control thanks to the possibility of fabricating very narrow fins. We demonstrate that by switching from conventional inversion mode operation to junction-less devices, which operates in accumulation mode, the BTI reliability for low thermal budget high-k metal gate stacks can be significantly improved thanks to the reduced operating oxide electric field. We systematically investigate the BTI stress/recovery kinetics by using the two-state NMP model as implemented in the imec/T.U. Wien "Comphy" framework and reproduce the measured data in both IM and JL devices with a single set of oxide defect parameters. We show that a lifetime projection based on a power-law of the stress overdrive voltage for JL contradicts experimental observations and results into a paradox (i.e., insufficient reliability at flat-band voltage, which corresponds by definition to zero electric field) and is therefore inapplicable for this device type.

References

[1] J. Franco *et al.*, "Suitability of high-k gate oxides for III–V devices: A PBTI study in In0.53Ga0.47As devices with Al2O3," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Jun. 2014, pp. 6A.2.1–6A.2.6. doi: 10.1109/IRPS.2014.6861098.

[2] J.-P. Colinge *et al.*, "Nanowire transistors without junctions," *Nat. Nanotechnol.*, vol. 5, pp. 225–229, Feb. 2010. doi: 10.1038/nnano.2010.15.

[3] M. Toledano-Luque *et al.*, "Superior reliability of junctionless pFinFETs by reduced oxide electric field," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1179–1181, Dec. 2014. doi: 10.1109/LED.2014.2361769.

[4] M. Cho *et al.*, "On and off state hot carrier reliability in junctionless high-K MG gate-all-around nanowires," in *Proc. Electron Devices Meeting (IEDM)*, Washington, DC, USA, Dec. 2015, pp. 14.5.1–14.5.4. doi: 10.1109/IEDM.2015.7409697.

[5] B. Kaczer *et al.*, "Ubiquitous relaxation in BTI stressing—New evaluation and insights," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Phoenix, AZ, USA, Apr. 2008, pp. 20–27. doi: 10.1109/RELPHY.2008.4558858.

[6] B. Kaczer *et al.*, "Benchmarking time-dependent variability of junctionless nanowire FETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Monterey, CA, USA, Apr. 2017, pp. 2D-6.1–2D-6.7. doi: 10.1109/IRPS.2017.7936266.

[7] J. Franco *et al.*, "NBTI in replacement metal gate SiGe core FinFETs: Impact of Ge concentration, fin width, fin rotation and interface passivation by high pressure anneals," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Pasadena, CA, USA, Apr. 2016, pp. 4B-2-1–4B-2-7. doi: 10.1109/IRPS.2016.7574533.

[8] S. M. Sze and K. N. Kwok, *Physics of Semiconductor Devices*. New York, NY, USA: Wiley, 2006. doi: 10.1002/0470068329.

[9] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct. 1989. doi: 10.1109/JSSC.1989.572629

[10] J. R. Hauser and K. Ahmed, "Characterization of ultra-thin oxides using electrical C-V and I-V measurements," *AIP Conf. Proc.*, vol. 449, no. 1, p. 235, Mar. 1998. doi: 10.1063/1.56801.

[11] B. Riccò, P. Olivo, T. N. Nguyen, T.-S. Kuan, and G. Ferriani, "Oxide-thickness determination in thin-insulator MOS structures," *IEEE Trans. Electron Devices*, vol. 35, no. 4, pp. 432–438, Apr. 1988. doi: 10.1109/16.2476.

[12] A. Kerber and E. Cartier, "Bias temperature instability characterization methods," in *Bias Temperature Instability for Devices and Circuits*. New York, NY, USA: Springer, 2014, pp. 3–31. doi: 10.1007/978-1-4614-7909-3_1.

[13] G. Rzepa *et al.*, "Comphy—A compact-physics framework for unified modeling of BTI," *Microelectron. Reliab.*, vol. 85, pp. 49–65, Jun. 2018. doi: 10.1016/j.microrel.2018.04.002.

[14] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. Hoboken, NJ, USA: Wiley, 2003, pp. 71–175. doi: 10.1116/1.571867.

[15] J. Franco *et al.*, "BTI reliability improvement strategies in low thermal budget gate stacks for 3D sequential integration," in *Proc. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2018, pp. 34.2.1–34.2.4. doi: 10.1109/IEDM.2018.8614559.

[16] G. Rzepa *et al.*, "Efficient physical defect model applied to PBTI in high-k stacks," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Monterey, CA, USA, Apr. 2017, pp. XT-11.1–XT-11.6. doi: 10.1109/IRPS.2017.7936425.

Authors' photographs and biographies not available at the time of publication.