An Efficient Analog Compact NBTI Model for Stress and Recovery Based on Activation Energy Maps

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Abstract—Despite considerable research efforts, efficient and accurate analog bias temperature instability (BTI) stress and recovery models are still urgently needed to evaluate aging in circuit simulators. We present a model for arbitrary analog BTI stress based on distributed first-order reactions to model the time dynamics responsible for the threshold voltage shift of BTI. We use a single activation energy map, which includes the voltage and temperature dependence of stress and recovery. To validate the model, we present the calculation of the threshold voltage shift after arbitrary gate bias stress with high accuracy, industry-compatible measurement effort, and stress time-independent computational effort and introduce a model suitable for circuit simulations.

Index Terms—Activation energy maps, bias temperature instability (BTI), capture and emission time (CET), modeling, recovery.

I. INTRODUCTION

RECOVERY is the most troublesome feature of negative bias temperature instability (NBTI) [1], [2], which is one of the most critical reliability issues for silicon-based MOSFETs [3]. In particular, modeling the degradation and recovery after arbitrary gate stress is a considerable challenge [4]–[7]. Up to now, there is no commercially available circuit-compatible model considering bias temperature instability (BTI) including recovery. A discussion of dozens of NBTI models published in the last decade is beyond the scope of this article. Alternatively, we define four requirements, all of which have to be met mandatorily for a model suitable for an aging simulator.

1) The model has to correctly treat degradation/recovery time constants from sub-s to 10 years. In addition, a minimum accuracy is required.
2) When modeling an actual stress condition, the model has to consider the complete stress history like temporal

changes, including stress/recovery voltage, peaks, temperature, and application modes such as, e.g., standby.
3) It is a well-known fact/feature [8], [9] that different components of BTI may be in different states of degradation/recovery at the same time, depending on the stress history and has to be considered within the model.
4) A model might be able to correctly model degradation for an arbitrary stress stimulus, e.g., by numerically solving differential equations, but such computations are time- and computing power-consuming, and as such unsuitable for use in circuit simulators. A practical stress stimulus may be complex but is periodic in general, and a model must be able to take advantage of this periodicity.
5) A final requirement for use in commercial simulators is that the effort to set up the model (mostly experimental) has to be feasible.

It is clear that an overwhelming majority of published models [10]–[13] – mostly predicting the time evolution due to one single stress/recovery sequence or a 2-level ac-condition – do not meet the above requirements. TCAD models [14], or models having to solve diffusion processes [15], are computationally too intensive. Giering *et al.* [16] used the advantage that the differential equation of the Markov-two-state NBTI model has an efficient numeric solution for periodic stress voltage. They used the TCAD defect database of [14], and thus also assumed 2-level defects, which is an approximation affecting the frequency dependence above ≥100 kHz. An approach without the need for a defect database is presented in this article using capture and emission time (CET) maps. None of the previous CET map approaches could calculate the arbitrary gate stress, which is required for circuit simulations. We thus enhance the CET map approach presented by Grasser [17] and Reisinger [11] by using voltage-dependent activation energy maps and a smart discretization of the analog stress pattern and the use of differential activation energy maps. The discretization is only possible because additionally the stress and recovery voltage dependence of the discretized activation energy maps is included.

In this article, we present an efficient compact model to analytically calculate the threshold voltage shift induced by NBTI after an arbitrary gate bias stress, fully meeting all the above stated five requirements. First, in Section II, the model itself is shortly described and in Section III, the details of the voltage-dependent activation energy maps

are presented. Second, with the presented approach, for the calculation of the degradation after arbitrary stress, the separation into several voltage classes is needed and introduced in Sections IV and V. Third, measurement and simulation of several arbitrary stress patterns, as well as a circuit-relevant stress pattern (inverter within a chain of inverters), are compared in Section VII. We conclude with the discussion of the approximations and the model properties in Section VIII.

II. MODEL DESCRIPTION

The model is formulated in a closed analytical form based on a defect-centric perspective using the voltage dependent activation energy map as shown in [18]. More details about measurements etc. can be found in [11], [19].

1) The goal of the model is to reproduce all features of BTI, like stress-voltage dependence, long-term recovery, recovery during and after ac stress, and degradation during analog stress.
2) The accuracy of the model, that is, the agreement between the model and the experimentally observed ΔV_{th} is intended to be less than 10% relative, which is a typical sample/sample variation for wide MOSFETs.
3) The defect kinetics are described for each individual defect by CET constants [20], where the time constants correspond to the reciprocal rates of chemical reactions [10].
4) A single CET map is valid for a given temperature, stress, and recovery voltage. To extract a single CET map, preferentially, very long recovery traces of more than 10^5 s are required, as shown in [21].
5) In this article, these long recovery times are accelerated by the **T**emperature **A**ccelerated measure-stress-measure (TA-MSM) measurements at a constant stress voltage with linear temperature ramps [19], thus reducing the total measuring time from more than 300 hours to less than 10 hours in measurement time per stress voltage. To cover the full voltage dependence, several measurements at different combinations of stress- and recovery-voltages are needed as demonstrated in [18].
6) Instead of the calculation of discrete CET combinations as tried in [21], an analytic formulation of the topology of the CET maps is used [17].
7) Rather than extracting CET maps for different temperatures, a unified activation energy maps representing CET maps for all temperatures is used. In addition, the stress voltage dependence of the activation energy map has to be included [18], and will be described in Section III.
8) As a final step, an optimizer is used to do a common fit of all model parameters to the experimental stress and recovery traces for all temperatures and voltages.

To include arbitrary voltage stress in the model, the following steps have to be performed, and are discussed in Section IV.

9) The stress pattern can be approximated by a digital ac pattern by discretizing the pattern with N_V defect classes.
10) The defect occupation after two-level digital ac stress can be easily calculated as described in [11].

11) For each defect class, a differential activation energy map is calculated using the voltage-dependent model.
12) The recovery voltage dependence has to be included in the calculation of the defect occupation.
13) The overall threshold voltage shift after arbitrary gate stress is then calculated as the sum of all contributions of the voltage classes.

III. VOLTAGE DEPENDENT ACTIVATION ENERGY MAP

As demonstrated in [17], the most important experimentally observed features of NBTI can be explained in an analytical form using activation energy maps. The defect density map can be described in agreement with previous work by two bivariate Gaussian distributions [20], [22]: One bivariate Gaussian distribution for the recoverable component and one distribution for the mostly permanent component (in typical experimental windows) [23], [24]. The temperature dependence of the defect time constants for capture and emission has been shown to follow the Arrhenius law [19], [25]:

$$\tau = \tau_0 \cdot \exp\left(\frac{E_a}{k_B T}\right) \tag{1}$$

with an activation energy E_a, Boltzmann's constant k_B and the temperature-independent constant τ_0. The activation energy map is a temperature-independent map, whereas the CET maps at a constant temperature are calculated using (1) with one characteristic temperature-independent constant $\tau_{0,r}$ for the recoverable and $\tau_{0,p}$ for the quasi-permanent defects [26]. The main parameters are the mean values of the capture and emission activation energies E_c and E_e (μ_c and μ_e), as well as the standard deviations of the mean values (σ_c and σ_e) describing the position and the width of defect density distributions. The model assumes that defects with higher capture activation energies E_c also have larger emission activation energies E_e: $E_e = E_c + \Delta E_e$. Furthermore, the correlation of the standard deviations $\sigma_e^2 = r\sigma_c^2 + \sigma_{\Delta_e}^2$ is modeled as shown in [22], with r being the correlation parameter $0 \leq r \leq 1$ (no correlation $r = 0$ between the capture and emission energies, $r = 1$ correlation), independent for each component. Thus, the charged trap density $g(E_c, E_e)$ for each component is given by

$$g(E_c, E_e) = \frac{A}{2\pi\sigma_c\sigma_{\Delta_e}}$$
$$\times \exp\left(-\frac{(E_c - \mu_c)^2}{2\sigma_c^2} - \frac{(E_e - (rE_c + \mu_{\Delta_e}))^2}{2\sigma_{\Delta_e}^2}\right). \tag{2}$$

The amplitudes A_r, A_p give the maximum obtainable degradation. if all defects are charged. The threshold voltage shift is the integral over all charged defects [17]

$$\Delta V_{\text{th}}(t_s, t_r) = \int_{E_c=0}^{\infty} \int_{E_e=0}^{\infty} P(E_c, E_e, t_s, t_r)$$
$$\times g(E_c, E_e) \, dE_e \, dE_c. \tag{3}$$

with $P(E_c, E_e, t_s, t_r)$ being the defect occupancy map for a given stress/recovery pattern. To obtain the activation energy map parameters, we perform a least-squares minimization for
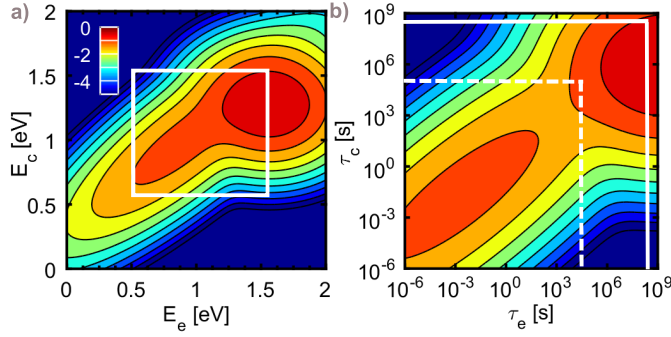
Fig. 1. Activation energy and CET maps extracted from the data presented in [19] for $V_{gs} = -2$ V. All maps are shown on a logarithmic color scale; 0 corresponds to a ΔV_{th} of 10^0 mV/10^{-4}eV^2. (a) Activation energy map for the recoverable and quasi-permanent component. The white square indicates the experimental window. (b) CET maps at $T = 150$ °C calculated from (a) with a typical experimental window for constant temperature measurements (dashed square) and the experimental window covered by TA-MSM measurements (solid square).

TABLE I
ACTIVATION ENERGY MAP PARAMETERS OF FIG. 1

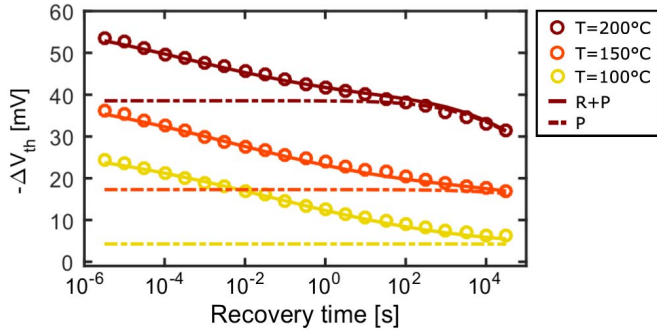|	$\tau_0 [ns]$	$\mu_c [eV]$	$\sigma_c [eV]$	$\mu_{\Delta e} [eV]$	$\sigma_{\Delta e} [eV]$	$V_0 [V]$	m	r
R	$5.5 \cdot 10^{-5}$	0.97	0.3	-0.08	0.2	-4.8	3	1
P	0.57	1.28	0.1	1.47	0.2	-4	2.8	0

Fig. 2. Temperature dependence: Recovery measurements (circles) after 10-ks stress with $V_{gs} = -2$ V. Simulations (lines) with the activation energy map (see Fig. 1) show that the temperature dependence is fully covered by the Arrhenius law with $\tau_{0,r}$ and $\tau_{0,p}$ given in Table I. At $T = 200$ °C also, recovery of the quasi-permanent (dashed lines) component is observed (full set of MSM data were published in [19]).

the TA-MSM measurement data with the analytic activation energy map model ((3), see data in [18] and [19]).

The defect density as a function of the activation energy for charge capture and emission is shown in Fig. 1(a) with the fit parameters (see Table I). The square indicates the measurement range of the TA-MSM measurements in energy space. A recovery time of 100 ks at $T = 200$ °C corresponds to more than 10^8 s at $T = 100$ °C. In Fig. 2, we compare simulations (with the activation energy map shown in Fig. 1) with measurements of the recovery after 10 ks stress for three different temperatures. The temperature dependence is fully described by the Arrhenius law and the temperature-independent constants $\tau_{0,r}$ and $\tau_{0,p}$ given in Table I for Infineon's 130 nm technology.
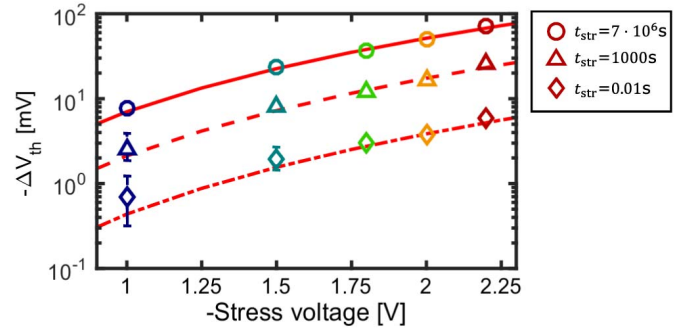

Fig. 3. Voltage dependence: Degradation as a function of stress voltage after different stress times and $t_r = 1$ μs (symbols: measurement data with error bars). The analytic model (lines) for each stress time is calculated with the voltage dependent activation energy map and the parameters given in Table I (Full set of TA-MSM data were published in [18]).

To model the voltage dependence of the activation energy maps, TA-MSM measurements at different stress voltages are performed. ΔV_{th} after three exemplary stress times is shown in Fig. 3 for all five stress voltages which have been used to obtain the voltage dependence of the activation energy map. To cover the experimentally observed voltage dependence, we extended the model to have a voltage-dependent defect density amplitude for each component (A_r and A_p) as

$$A = \left(\frac{V_{stress}}{V_0} \right)^m \tag{4}$$

with the constants m and V_0 [17]. Previous studies on individual defects [27] have shown that the mean value μ_c of each distribution linearly decreases with increasing stress voltage (capture times decrease with increasing stress voltage). We thus model the linear decrease with increasing stress voltage by $\mu_c = \mu_{c,0} + k V_{stress}$, where μ_{c0} denotes the mean value of activation energy constants for the charge capture at 0V and k is the voltage acceleration factor. The emission times remain unaffected by the stress voltage; accordingly, we model: $\mu_{\Delta e} = \mu_{\Delta e0} - k V_{stress}$ and we obtain $k_r = 0.01$ eV/V and $k_p = 0$ eV/V. All simulations are performed with the parameters given in Table I. Figs. 2 and 3 demonstrate the excellent accuracy of the model with a maximum deviation of $\delta \leq 5\%$. Further measurements showing the full stress and recovery time dependence of Fig. 3 and discussions on the obtained parameters can be found in [18].

IV. DEFECT CLASSES

To calculate the threshold voltage shift after arbitrary stress signals, we divide the defects into N_V defect classes. Each defect class can only be charged when a certain stress voltage is applied. This is illustrated in Fig. 4(a)–(c) for the three cases: a) applied flat band voltage with all defects (within the oxide and at the interface) located above the Fermi level E_F. When applying a stress voltage to the gate as shown in Fig. 4(b) and (c), all defects are shifted depending on the stress voltage to lower energies. If below the Fermi level E_F, the defects are charged within a capture time τ_c
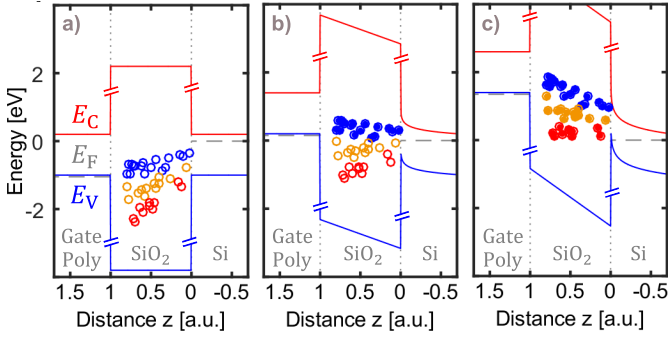
Fig. 4. Exemplary schematic of defect classes (only for illustration, not used for the simulation). We assume that when the defects are below the Fermi level of the substrate, the defects get charged within a finite capture time. (a) The flat band voltage is applied. All defects remain uncharged. (b) $V_{gs,blue}$ stress voltage is applied, all defects are shifted. Blue defects are located below the Fermi level. (c) Increased stress conditions $V_{gs} = V_{gs,blue}$, all defects are shifted further and are located below the Fermi level. The capture times for the blue and orange defects are reduced (see Fig. 5). The distance dependence is experimentally not accessible and not required for the model.
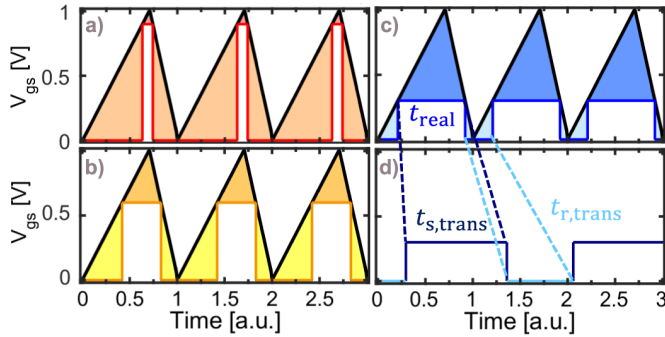

Fig. 5. Exemplary discretization of a sawtooth V_{gs} stress pattern versus time for: (a) red, (b) orange, and (c) blue defects. If the stress voltage is higher than the defect class voltage (dark red/orange/blue shaded area in (a)–(c)), the effective stress time is increased according to (5). For recovery voltages lower/higher than the initial threshold voltage (light red/orange/blue shaded area in (a)–(c), the effective recovery time is accelerated/decelerated. (d) Example of the transformed stress and recovery times for the blue defect class.

(depending on the type and location of the defect within the oxide). We discretize the stress pattern according to the defect classes. For the sake of simplicity, a sawtooth signal is shown in Fig. 5(a)–(c) and only three voltage classes are considered. A real analog signal may assume any level of complexity and instead of a simple pulse per period will produce a more complex digital pattern for each V_i, as shown for example in Fig. 8. The digital stress pattern, e.g., for the blue defect class, is shown in Fig. 5(c), with stress for $V_{gs} \geq V_{gs,blue}$ and recovery for $V_{gs} \leq V_{gs,blue}$. Furthermore, it has to be considered that the capture time constant is accelerated for $V_{gs} \geq V_{gs,blue}$. The acceleration is calculated for the analog V_{gs} stress with a transformed stress time $t_{s,trans}$, as shown in Fig. 5(d) and is extracted from time dependent defect spectroscopy (TDDS) measurements (data not shown, presented in [27]), and is modeled as

$$t_{s,\text{trans}} = t_{s,\text{real}} \cdot 10^{a_s \cdot \left(e^{-\frac{V_{gs}}{b_s}} - e^{-\frac{V_i}{b_s}} \right)} \qquad (5)$$
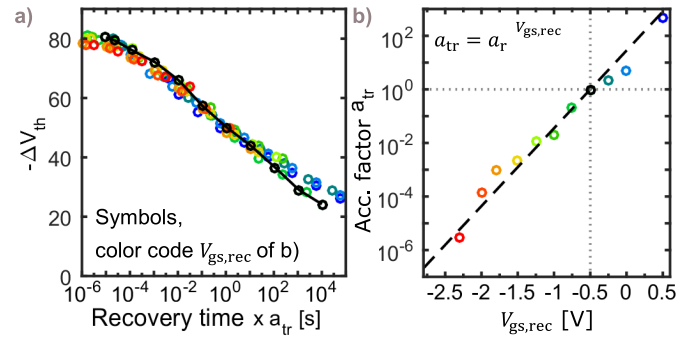

Fig. 6. Recovery time dependence with recovery voltage: (a) Recovery after the same amount of degradation for different recovery voltages. (b) Extracted acceleration factor in dependent on the recovery voltage. Multiplication of the recovery time with the acceleration factor $a(V_{gs,rec})$ shown in Fig. 6(b) leads to a universal recovery curve.

with $a_s = 11.5$ and $b_s = -1.3$ V. For an unknown technology, either TDDS measurements can be used to extract a_s, b_s or digital ac measurements with varied V_{low}, as shown in Fig. 10. Furthermore, TA-MSM measurements and the corresponding extracted activation energy maps are recorded at one recovery voltage, e.g., $V_{gs} = V_{th}$. But, as can be seen in Fig. 6, recovery is slowed down for $V_{th} < V_{gs,rec} < V_{gs,stress}$ and accelerated for $V_{gs,rec} < V_{th}$ In Fig. 6(a), recovery after the same amount of degradation is shown for different recovery voltages. Multiplication of the recovery time with an acceleration factor $a(V_{gs,rec})$ (see Fig. 6(b) leads to a universal recovery curve. We thus model the recovery voltage dependence as

$$t_{r,\text{trans}} = t_{r,\text{real}} \cdot a_r^{V_{gs,rec}} \qquad (6)$$

with $a_r = 8 \cdot 10^2$. The threshold voltage shift when changing the stress voltage from V_i to V_{i+1}: is calculated using differential activation energy maps for each defect class

$$g_d(E_c, E_e) = g(V_{i+1}) - g(V_i, \Delta E_c) \qquad (7)$$

$g(V_{i+1})$ is calculated with (2), while the additional shift in the capture activation energy of $g(V_i)$ has to be considered via

$$\Delta E_c = k_b T \left(\log \left(\frac{t_{s,\text{real}}}{\tau_0} \right) - \log \left(\frac{t_{s,\text{trans}}}{\tau_0} \right) \right). \qquad (8)$$

In Fig. 7, differential activation energy maps are shown for a) $V_1 = 1$ V, $V_2 = 1.1$ V and b) $V_1 = 2$ V, $V_2 = 2.1$ V. As described in Section III Fig. 7(a) and (b), there is a voltage dependence of the amplitude for the quasi-permanent component and the recoverable component. On increasing the stress voltage, the capture activation energies for the recoverable component decrease, whereas nearly no shift of the quasi-permanent component is observable (dashed lines are guide to the eye). The discrete defect classes are chosen such that each defect class roughly contributes the same change in ΔV_{th}. Therefore, the voltage levels of the defect classes are distributed on a logarithmic scale with decreasing voltage steps toward higher stress voltages following (4).

V. OCCUPATION MAPS

To calculate the threshold voltage shift contributed by each defect class V_i following (3), the occupation maps of each
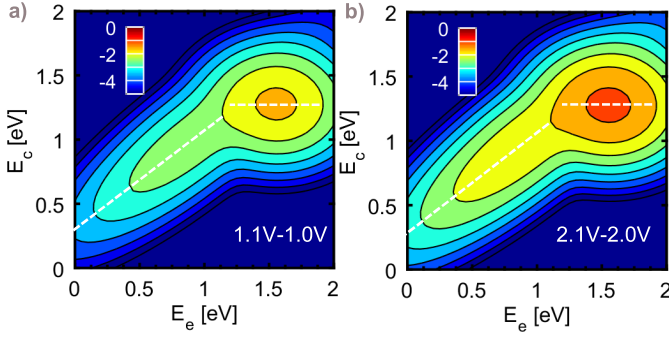
Fig. 7. Differential activation energy map obtained with the parameters presented in Table I, showing the contribution of defects being activated within a change of stress from $V_{gs} = V_1$ to $V_{gs} = V_2$. All maps are shown on a logarithmic color scale, 0 corresponds to a ΔV_{th} of 10^0 mV/10^{-4} eV^2. (a) $V_2 = -1.1$ V. $V_1 = -1$ V. (b) $V_2 = -2.1$ V, $V_1 = -2$ V.
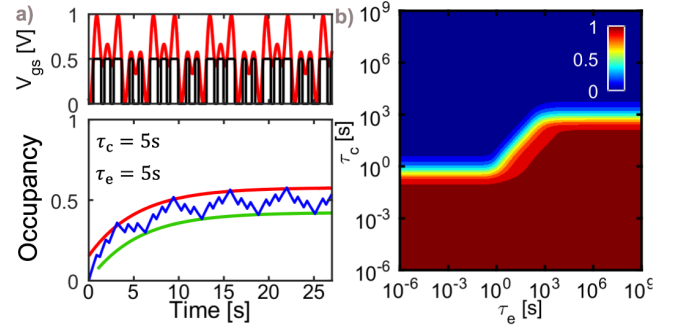

Fig. 8. Occupation probability after an exemplary pulse pattern: (a) Charging/decharging pattern (black) extracted from an exemplary stress pattern (red, superpositioned sine) (top). (a) Recursively calculated occupancy with stress time t_{ac} for a single defect (blue) (bottom). The envelope function calculated using (15) for the highest (red) and the lowest occupancies (green). (b) Occupancy map $P(t_s, t_r, \tau_c, \tau_e)$ for the highest occupancy in the pattern shown in (a) for all τ_c, τ_e combinations and $t_{ac} = 1000$ s.

defect class have to be calculated individually. The stress pattern of each defect class V_i is obtained as demonstrated in Fig. 5 for $n = 1$. For a complex signal, it consists of n stress and recovery pulses as shown in Fig. 8. A mathematical description for each defect is an asymmetric Resistor Capacitor (RC)-element [11], [12]. The occupancy $P(t_s, t_r)$ after a stress time t_s or recovery time t_r, respectively, can be described by

$$P(t_s) = P(t_s = 0) \times \left(1 - e^{-\frac{t_s}{\tau_c}}\right) \qquad (9)$$

$$P(t_r) = P(t_r = 0) \times e^{-\frac{t_r}{\tau_e}}. \qquad (10)$$

The probability that a defect is occupied after application of a stress pattern can be iteratively calculated step-by-step (as shown in Fig. 8(a). This is time-consuming and the computational effort strongly depends on the signal frequency and the number of pulses n. Following [11] for $n = 1$, the envelope function of a periodical stress pattern after a stress time t_{ac} with one charging pulse of length t_s and one discharging pulse of length t_r and duty cycle β can be calculated analytically as

$$P_L(t_{ac}) = \left(1 - e^{-\frac{t_{ac}}{\overline{\tau}}}\right) \times \frac{d_1 - d_1 u_1}{1 - d_1 u_1} \qquad (11)$$

$$P_H(t_{ac} - \Delta T \times (1 - \beta)) = \left(1 - e^{-\frac{t_{ac}}{\overline{\tau}}}\right) \times \frac{1 - u_1}{1 - d_1 u_1} \qquad (12)$$

with

$$\frac{1}{\overline{\tau}} = \frac{\beta}{\tau_c} + \frac{1 - \beta}{\tau_e} \qquad (13)$$

with the abbreviations (in this case, $n = 1$)

$$u_n = e^{-\frac{\Delta t_{s,n}}{\tau_c}}, \quad d_n = e^{-\frac{\Delta t_{r,n}}{\tau_e}}. \qquad (14)$$

For n pulses, following (12) and (13), we derive the envelope function of the last recovery pulse within the pulse pattern as

$$P_{L,n} = (d_n - u_n d_n + d_{n-1} u_n d_n - u_{n-1} d_{n-1} u_n d_n$$
$$+ \cdots - u_1 d_1 \ldots u_{n-1} d_{n-1} u_n d_n) \times \frac{1 - e^{\frac{t_{ac}}{\overline{\tau}}}}{1 - u_1 d_1 \ldots u_n d_n}$$
$$= \left(d_n + \sum_{i=0}^{n-1} \left(\prod_{j=0}^{i} u_{n-j} d_{n-j}\right) (d_{n-i-1} - 1)\right)$$
$$\times \frac{1 - e^{\frac{t_{ac}}{\overline{\tau}}}}{1 - \prod_{k=1}^{n} u_k d_k} \qquad (15)$$

with $d_0 = 0$ and $\overline{\tau}$ is the ac-charging time constant, which writes for n alternately stress and recovery pulses

$$\frac{1}{\overline{\tau}} = \frac{t_{s,tot}}{t_{tot} \cdot \tau_c} + \frac{t_{r,tot}}{t_{tot} \cdot \tau_e} \qquad (16)$$

with the total stress time $t_{s,tot} = \sum_{i=1}^{n} \Delta t_{s,i}$, the total recovery time $t_{r,tot} = \sum_{i=1}^{n} \Delta t_{r,i}$, and the total period time $t_{tot} = t_{s,tot} + t_{r,tot}$ of the n pulses. For the extracted digital pulse pattern of an exemplary stress, the occupation probability of a single defect and the corresponding occupancy map $P(t_{s,n}, t_{r,n}, \tau_c, \tau_e)$ are shown in Fig. 8. Instead of the real stress times in Fig. 8, the transformed stress and recovery times for each defect class V_i have to be used for the calculation of the occupancy maps $P(t_s, t_r)$. For the calculation of the threshold voltage shift, the occupation map has to be transformed into the energy space following (1) for the recoverable and quasi-permanent components independently due to different temperature dependencies, so $P(t_{s,n}, t_{r,n}, V_i) \leftrightarrow P(E_{s,n}, E_{r,n}, V_i)$. The threshold voltage shift induced by one defect class V_i is then given by

$$\Delta V_{th}(t_{ac}, V_i) = \int_{E_c=0}^{\infty} \int_{E_e=0}^{\infty} P(E_{s,n}, E_{r,n}, V_i)$$
$$\times g_d(V_i) \, dE_e \, dE_c. \qquad (17)$$

The overall threshold voltage shift is calculated as

$$\Delta V_{th}(t_s, t_r) = \sum_{i=1}^{N_V} \Delta V_{th}(t_{ac}, V_i). \qquad (18)$$

VI. EXPERIMENTAL DETAILS

All measurements were performed on productive quality MOSFETs of a 130 nm smart power technology with a 2.2 nm nitrided gate oxide. All measurements were performed using the ultra-fast measure-stress-measure (MSM) technique as described in [28], with a measurement delay of 1 s. TA-MSM measurements, as described in [19], were performed to obtain the fit parameters for our 130 nm technology as given in Table I.
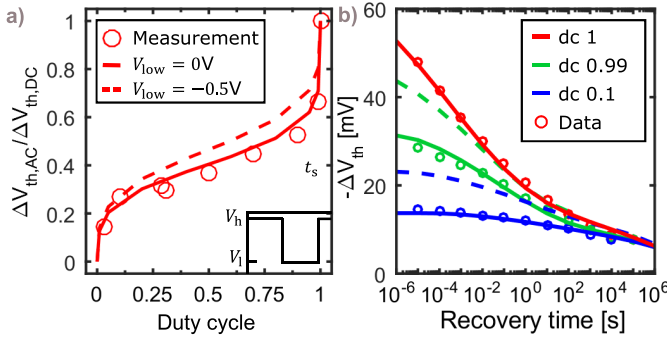
Fig. 9. Duty cycle dependence: Experimental data (circles) from [11]. The solid/dashed lines show the simulation results with our model for $V_{gs,low} = 0$ V and $V_{gs,low} = -0.5$ V, respectively. (a) Experimental and simulated dependence of ΔV_{th} versus duty factor with $T = 175$ °C and $V_{gs,high} = -2.7$ V, $V_{gs,low} = 0$ V, $f = 100$ kHz, and $t_s = 10$ ks, and a measuring delay of 1 μs. (b) Measured and simulated recovery after stress with duty cycle 1/0.99/0.1 with t_{ac} 100/101/1000 s such that all measurements have the same accumulated stress times. Simulations and measurements are in perfect agreement.

VII. MODEL VERIFICATION

The presented model is able to reproduce and explain all important typical characteristics of NBTI. We present measurements and simulations of the duty cycle dependence, recovery after different digital ac stress patterns, dependence on the recovery voltage as well as different analog stress patterns such as sine, sawtooth, triangle, and circuit relevant stress patterns.

The duty cycle dependence of ac-NBTI has been reported in many publications. ΔV_{th} versus duty cycle as shown in Fig. 9(a) always shows the typical shape like a lying "S" with sharp rises between $\beta = 0$–10% and $\beta = 90$–100%. We verify the "S-shape" dependence with our model and compare the simulation results with measurement data from [11] of the same technology. Measurements and simulations show an excellent agreement, even without the consideration of the frequency dependence due to metastable states [29]. In [11], the occupancy map has been calculated without considering the recovery dependence when decreasing $V_{low} = V_{th}$ (condition of the CET map) to $V_{low} = 0$ V (see the dashed line with $V_{low} = V_{th}$). In Fig. 9(b), the recovery is compared for three different duty cycles after the same net stress times. Due to the same net stress time, all recovery traces have to merge at a well-defined point in time, depending on their duty cycle and the recovery during the ac stress. We further study the acceleration/deceleration of the recovery time with recovery voltage and varying V_{low} while keeping constant V_{high} for a digital ac stress pattern. Measurements and the corresponding simulations are shown in Fig. 10. The threshold voltage shift as a function of V_{low} is well modeled. Almost no recovery within the ac stress can be observed for $V_{low} = -1.5$ V and $V_{low} = -1.0$ V. A stronger effect of the recovery can be seen by decreasing the $vlow$ to $V_{low} = 0$ V. Further recovery acceleration is achieved with positive $V_{low} = 0.5$ V. Only smaller differences can be observed on changing the frequency from $f = 100$ kHz to $f = 10$ kHz with $V_{low} = 0$ V. The effect of temperature is accurately captured as well. In Fig. 11, we show the recovery subject to two different analog patterns
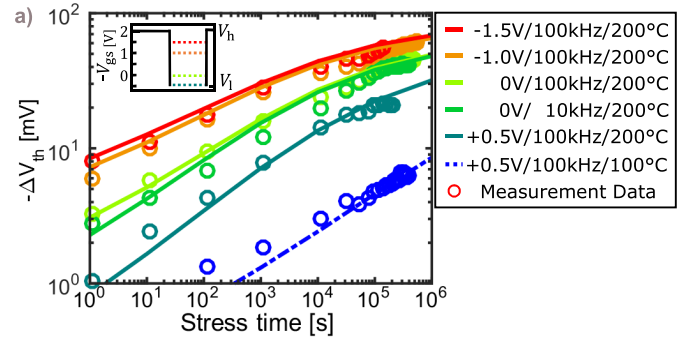

Fig. 10. Digital ac stress: Varied low level at two temperatures and two frequencies, readout at the end of V_{low}. The legend denotes the applied V_{low}/frequency/temperature with $V_{gs,high} = -2$ V and duty cycle $\beta = 0.5$. A good agreement between the model (lines) and measurements (circles) is achieved for all stress conditions.
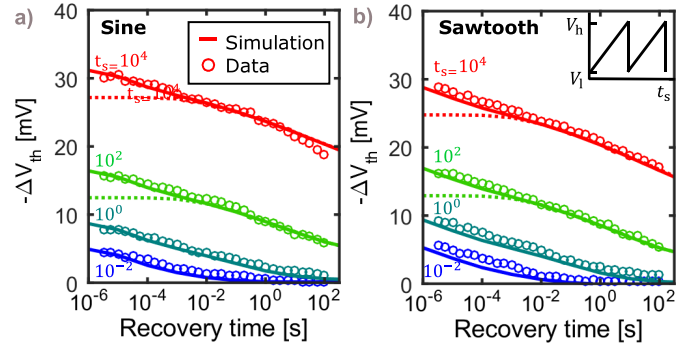

Fig. 11. MSM measurements as published in [16] (circles) and simulations (lines) of a periodical analog stress between $V_{low} = 0$ V and $V_{high} = -2.8$ V with $f = 2$ kHz and $T = 125$ °C: (a) Sine. (b) Sawtooth. The stress is interrupted for (a) at $V = -1.4$ V and for (b) at $V_{high} = -2.8$ V, and the solid lines are simulations at this condition, whereas the dashed lines correspond to simulations with the stress interrupted at $V_{low} = 0$ V.

(sine and sawtooth) after different stress times. Measurements and simulations show an excellent agreement for all stress and recovery times. The degradation with stress time after the end of V_{high}, as shown in Fig. 12, is as expected, the highest for the digital stress and the lowest for the sawtooth stress. The difference is about 20%, which is about the highest possible difference for stress signals with the same duty cycle. Of course, discretizing the arbitrary stress signal causes a deviation from the optimal solution. In Fig. 12, the simulation error as a function of the number of defect classes is shown. To obtain a reasonable simulation time of $\ll 100$ ms per transistor, we use $N_V = 20$ for all simulations shown in this article, and the simulation error is then below 2.5%.

For analog circuits, a correct consideration of the low level is very important and is, e.g., especially required for comparators. Therefore, we validate the low-level dependence by applying an analog triangle stress signal to the gate with varied low level as shown in Fig. 13. The comparison with the dc stress shows only a minor reduction of the degradation for $V_{low} = -1$ V, but a much stronger reduction for zero or positive low levels. As seen in Fig. 13 mainly relevant for the lifetime estimation in analog circuits is the correct modeling of the quasi-permanent component, which is guaranteed by our
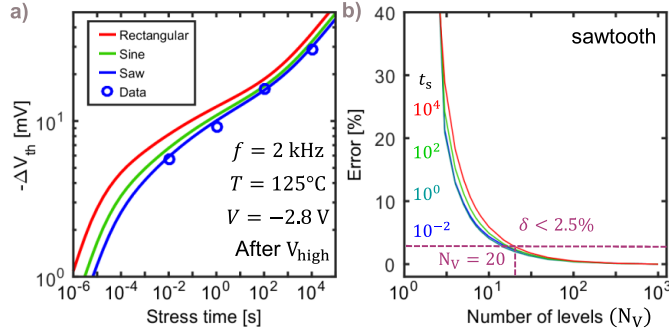
Fig. 12. (a) Simulated periodical analog stress with stress time after the end of V_{high}. Circuits correspond to measurement data for the sawtooth from Fig. 11. For long stress times, the degradation after rectangular stress is 20% higher than for a sawtooth signal. (b) Simulation error due to discretization using a discrete number of levels. For $N_V = 20$, the error is below 2.5%.
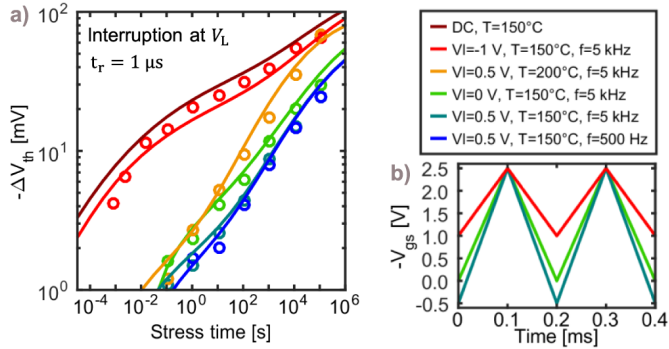

Fig. 13. Triangular ac stress for different low levels, frequencies, and temperatures with $V_{high} = -2.5$ V. (a) ΔV_{th} with stress time. Circles: measurement; solid lines: simulation. (b) $V_{gs}(t)$ for three different low levels $V_{low} = -1, 0, +0.5$ V with $f = 5$ kHz.
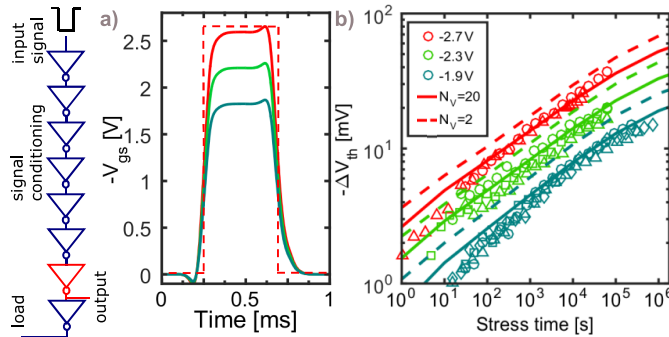

Fig. 14. Circuit relevant stress: (a) Typical inverter stress pattern (one inverter in a chain of inverters) for $V_{dd} = -1.9/-2.3/-2.7$ V with $f = 1$ kHz and $T = 150$ °C. (b) Measurement (circles) of the threshold voltage shift versus stress time at $T = 150$ °C with the applied stress pattern shown in (a) and $V_{ds} = 0$ (up to five samples per stress condition). Simulations with the model (solid lines) show a good agreement with the measurement data. Simulations approximating the stress by a digital signal (dashed lines) overestimate the actual threshold voltage shift by a factor of two.

TA-MSM approach. To show the applicability of the model to more realistic stress patterns, we present single transistor measurements with typical analog stress patterns as expected in a circuit. These patterns were obtained from independently run SPICE simulations of a chain of inverters as shown in Fig. 14(b) [30]. The gate stress pattern is stretched in time

by a factor of 1000 to simplify the experimental stress-setup. We keep $V_{ds} = 0$ for this experiment to suppress hot carrier stress (HCS). In Fig. 14(a), measurements and simulations of ΔV_{th} show an excellent agreement for all V_{dd}. The comparison with a model without consideration of the real waveform and solely approximating the stress with a digital stress pattern (dashed lines) shows an overestimation of the actual threshold voltage shift by a factor of two. Additional comparison of different analog ac stress patterns with TCAD and the model presented by Giering et al. [16] can be found in [31], together with circuit aging simulations of the frequency shift of different ring oscillators.

VIII. MODEL CHARACTERISTICS AND CONCLUSION

The presented model is intended for simulation of the threshold voltage shift after arbitrary analog BTI stress within a circuit simulator. The experimental effort is below 50 hours for the whole model and has been reduced with the new TA-MSM method. Furthermore, no time-consuming TDDS measurements are required. The whole model consists of 19 parameters: 8 parameters each for the recoverable and for the quasi-permanent component including the temperature and voltage dependence (see Table I) and 3 parameters for the consideration of the stress and recovery time acceleration/deceleration. Parameter extraction is performed with a standard least-squares minimization algorithm. The model includes the following assumptions and approximations:

1) The collective defect behavior is modeled and the 2-stage approximation is used [29], [32], therefore high-frequency ac dependencies are not covered [33].
2) For simplicity, the model does not include random telegraph noise.
3) We use a closed form description of the activation energy maps and no single defects were studied.
4) While the stress and recovery acceleration factors (see 5 and 6) are individual defect properties, in this model, only the mean values are used.
5) We discretize the stress pattern into N_V voltage classes with each class contributing roughly the same ΔV_{th} to the overall ΔV_{th}, following (4). Simulations with $N_V = 20$ show a simulation accuracy of $\leq 2.5\%$.
6) Periodical stress patterns over the lifetime or periodically recurring application modes (e.g., alternating standby, ON-state) are required. Without periodicity, the occupancy has to be calculated iteratively, which is time-consuming; however, meaningful for circuit simulators are only periodical stress patterns.

Due to the closed form of the model, the computational effort is stress time- and frequency-independent. For example, to calculate ΔV_{th} after 10 years for 1000 transistors with Mathworks MATLAB 2015b takes $\ll 10$ s for a discretization with $N_V = 20$ on an Intel Core i5 4300M 2.60 GHz. Variability can be added to the model by considering a Poisson distribution of charged traps, instead of an average, as well as the Weibull distributed step heights of each single defect caused by the interaction with random dopant distribution [34], [35]. Furthermore, the dependence on V_{ds} [36] is a possible add-on to a future version.

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