annealing damage, especially in the non-implanted quadrant. We have also noticed a conspicuous current scaling with the dose in this sample, indicating that active acceptors are contributing to the current transport. We will also investigate the impact of different contact metals on the contact resistance, and analyze the temperature-dependent Hall measurement to verify transport mechanisms.

12:45 PM C06
(Student) Growth and Characterization of GaN p-i-n Rectifiers Using Ion-Implantation Isolation Marzieh Bakhtiary-Noodeh, Chuan-Wei Tsou, Minkyu Cho, Mi-Hee Ji, Shyh-Chiang Shen, Theeradetch Detchprohm and Russell Dupuis; Georgia Institute of Technology, United States

Gallium nitride (GaN) devices are appropriate candidates for high-voltage applications because of their wide bandgap (~3.4 eV) and high breakdown electric-field (~3.3 MV/cm) characteristics. Proper device isolation and field termination are keys to suppressing the leakage current in the fabrication of vertical GaN power devices. Mesa etching is one of the major challenges in the fabrication of these devices, that usually leads to sidewall leakage currents and premature reverse-bias breakdown. Vertical GaN rectifiers using nitrogen-ion implantation as a mean of device isolation, have shown large blocking voltages (BV) and high drive currents and this technique could become an effective approach for the manufacture of high-performance vertical GaN devices. In this study, GaN-based rectifiers were grown by metalorganic chemical vapor deposition (MOCVD) on bulk GaN substrates having a low dislocation density. Vertical GaN power rectifiers grown on bulk GaN substrates having a low dislocation density (~10^3 cm^{-2}) can be a viable technology for high-power switching applications. In this work, we demonstrate 1130 µm diameter GaN *p-i-n* rectifiers having a blocking voltage (BV) of 1.2 kV and an ON-state current drive of 10 A. Ion implantation using nitrogen ions as used for device definition and electrical isolation. The epitaxial layers for GaN *p-i-n* rectifiers were grown using a close-coupled-showerhead AIXTRON 6x2" MOCVD system on bulk GaN substrates and fabricated using ion-implanted device isolation. The epitaxial layer growth consisted of the following layers: 1.0 µm thick *n*-GaN:Si layer (*n*~7×10^{18} cm^{-3}), 4.0 µm thick *n*⁻-GaN:Si layer (*n*~2.5×10^{16} cm^{-3}), 6.0 µm thick undoped-GaN, 0.45 µm thick *p*-GaN:Mg layer (*p*~6×10^{17} cm^{-3}). This epitaxial structure was designed for a target reverse-bias breakdown voltage of 1.2 kV. The MOCVD growth employed ammonia (NH_3) and trimethylgallium (TMGa) as primary precursors and biscyclopentadienemagnesium (Cp_2Mg) and silane (SiH_4) as dopants. The free-carrier concentration and resistivity of the doped layers were evaluated by Hall-effect characterization. Secondary ion mass spectrometry (SIMS) measurements were performed to confirm the doping profile of the layers. X-ray diffraction (XRD) was used for the characterization of the crystallographic quality of the PIN structure. The full width at half maximum of the rocking curve derived from (002) and (102) diffraction exhibit values of 90 and 130 arc-sec, respectively, primarily determined by the properties of the GaN substrate. Atomic force microscopy (AFM) was used to study the surface morphology and the corresponding root-mean-square (RMS) of the GaN *p-i-n* rectifier epitaxial structures. The RMS values for scanning area of 5×5 μm^2 is ~ 2.0 nm for the typical case. The rectifier device fabrication employed a backside *n*-metal contact formation of a Ti/Al-based metal stack, followed by a Ni/Ag-based *p*-metal contact on the front side of the wafer. Ion implantation of nitrogen ion species were used to provide device isolation. The evaluated devices have the diameters of 280, 830, and 1130 µm and the reverse-biased characteristics of these devices were measured. A BV of 1.2 kV was measured for 1130-µm-dia. devices, defined as the voltage where reverse current density $J_R = 10^{-2}$ A/cm^2. A slightly higher BV was measured for smaller device sizes. A BV of 1.3 kV was observed for devices with 280 µm dia. At a forward bias of 6.2 V, a forward current > 11 A was achieved for 1130-µm-dia. devices. A current drive of 10 A was achieved at a forward bias of ~7 V for 830 µm dia. devices. For *p-i-n* rectifiers with 280-µm dia., a value of R-ON of 0.28 mΩ. cm^2 was measured at I = 3.2 A (J = 5.2 kA/cm^2). In this talk, we will further describe the MOCVD growth, device processing, and rectifier electrical characteristics.

SESSION D: 2D Devices
Session Chair: Kevin Daniels
Session Hosts: Qiang Guo and Michael Spencer
Wednesday Morning, June 24, 2020
Location: ZoomRoom 4

11:30 AM D01
Low Variability and 10^{10} On/Off Current Ratio in Flexible MoS_2 FETs with Al_2O_3 Encapsulation Improved by Parylene N Yury Illarionov[1,2], Theresia Knobloch[1], Michael Waltl[1], Sayani Majumdar[3], Miika Soikkeli[3], Wonjae Kim[3], Stefan Wachter[4], Dmitry Polyushkin[4], Sanna Arpiainen[3], Mika Prunnila[3], Thomas Mueller[4] and Tibor Grasser[1]; [1]TU Wien, Austria; [2]Ioffe Institute, Russian Federation; [3]VTT Technical Research Centre, Finland; [4]Institute for Photonics, TU Wien, Austria

Introduction: Encapsulation of MoS_2 FETs presents an important step towards top-gated devices which are required for circuit integration. This is because insulators employed to protect the channel from the ambient can be subsequently scaled and used as top gate insulators. However, encapsulation layers themselves can as a side effect also degrade the device performance. For example, the encapsulation can increase device-to-device variability, reduce the mobility, or cause negative shifts of the threshold voltage which is often observed in MoS_2 FETs protected with Al_2O_3 [1,2]. Thus, possible limitations of different encapsulation schemes have to be understood prior to the next step, fabricating top-gated devices. **Devices:** We examine flexible CVD-MoS_2 FETs with 30nm thick Al_2O_3 grown by ALD as a gate insulator. The devices were encapsulated using four different schemes, namely Al_2O_3, Al_2O_3/Parylene N, Parylene N/Al_2O_3/Parylene N and Parylene C/Al_2O_3/Parylene N. In all cases the growth of Al_2O_3 was performed at 200°C, while Parylene N or C was deposited after 3 hours annealing at 130°C followed by 12 hours pumping. **Experimental technique:** We measure static I_D-V_G characteristics using the autorange mode and the hysteresis using different sweep rates S and times t_{sw}. The hysteresis dynamics is expressed by $\Delta V_H(1/t_{sw})$ traces [3], where ΔV_H is the hysteresis width extracted near the threshold voltage V_{th}. To verify the stability of our devices, we perform our measurements in the ambient and in vacuum before, during and after annealing at 165°C. For each encapsulation scheme we examine tens of devices to benchmark their variability. **Results:** Similar to previous literature reports [1,2], our results show that the I_D-V_G characteristics of MoS_2 FETs with Al_2O_3 encapsulation have a strongly negative V_{th} due to an n-type doping of the channel by positive charges inside Al_2O_3. At these negative V_G there is a substantial thermionic gate leakage current, which leads to a reduced on/off current ratio of only about 10^6. The use of Parylene N/Al_2O_3/Parylene N encapsulation makes V_{th} considerably more positive and thus allows achieving values up to 10^{10}. A Parylene C layer underneath the Al_2O_3 also suppresses the negative shift of V_{th}. However, the ON current is a few orders of magnitude lower as compared to Parylene N devices. Also, the mobility in MoS_2 FETs with Parylene C encapsulation is much smaller than in their counterparts with Parylene N, which is likely due to scattering of carriers at Cl atoms in Parylene C.
We also found that the use of Parylene N/Al_2O_3/Parylene N encapsulation makes the I_D-V_G characteristics of our MoS_2 FETs non-sensitive to the ambient environment and annealing at 165°C, while leading to the smallest device-to-device variability in performance parameters and hysteresis dynamics. However, the hysteresis in these devices is still sizable, which is caused in part by oxide defects in the Al_2O_3 and in part by adsorbates introduced during fabrication. The contribution coming from adsorbates is pressure-dependent [4], which results in a decreased hysteresis when measuring in vacuum. **Conclusions:** We performed a systematic study on the impact of encapsulation on the I_D-V_G characteristics and hysteresis in flexible MoS_2 FETs. We found that a highly stable Parylene N/Al_2O_3/Parylene N encapsulation allows to efficiently suppress the negative shift of V_{th} and to achieve an on/off current ratio of up to 10^{10}, while maintaining low device-to-device variability. Further steps should be to optimize device processing by avoiding air exposure in between device fabrication and encapsulation, which is expected to reduce the number of adsorbates and further suppress the hysteresis.
References: [1] J. Na et al, Nanoscale, 6, 433 (2014).; [2] N. Liu et al, ACS Appl. Mater. & Interfaces, 9, 42943 (2017).; [3] Y. Illarionov et al, 2D Mater., 3, 035004 (2016).; [4] A. Di Bartolomeo et al, 2D Mater., 5, 015014 (2017).

11:45 AM D02
New Methods and Observations in Contact Scaling for 2D FETs Zhihui Cheng[1,2,3], Hattan Abuzaid[1], Yifei Yu[4], Shreya Singh[1], Linyou Cao[4], Curt Richter[2] and Aaron D. Franklin[1,1]; [1]Duke University, United States; [2]National Institute of Standards and Technology, United States; [3]Purdue University, United States; [4]North Carolina State University, United States

Introduction: Atomically thin two-dimensional (2D) crystals are promising channel materials for extremely scaled field-effect transistors (FETs). For devices at the sub-10 nm technology nodes, both channel length (distance from source to drain contacts) and contact length (distance that the contacts overlap the 2D channel) must be scaled. However, contacting 2D materials at scaled contact lengths (L_c < 30 nm) has rarely been pursued or studied in-depth[1]. In this work, we experimentally scaled the L_c for MoS_2 2D FETs and found that, contrary to most previous reports, **top contacts can be scaled down to ~25 nm without noticeable degradation in contact resistance**. We also observed **significant self-heating in scaled contacts in the saturation regime**. While the first observation is promising for extremely scaled FET technologies, the second illustrates that current crowding in metal-2D contacts is a challenge toward the development for future scaled devices. **Contact scaling**: Ni contacts with L_c ranging from ~110 nm to ~25 nm were fabricated on the same bilayer MoS_2. Note that the channel length, ~460 nm, is identical between these devices. The I_D-V_{GS} curves of the devices show that although they have different threshold voltage (V_{TH}), their performance is similar after considering the overdrive voltage $V_{OV} = V_{GS} - V_{TH}$. Since the only difference in the devices is L_c, the variation in V_{TH} is caused by the change of L_c and the mechanism behind it merits further investigation. Accounting for the V_{TH} shift, we analyzed the I_D-V_{DS} curves and confirmed the very similar contact resistance and on-current across different L_c as the source. A slight negative differential resistance (NDR) is observed for devices with an $L_c \approx 25$ nm source at a relatively high carrier density of 7.2×10^{12} cm^{-2}, suggesting self-heating. **Self-heating and early saturation**: To further explore the self-heating phenomenon, we also fabricated devices with asymmetrical contacts—one side of the contacts with $L_c \approx 110$ nm and the other side with $L_c \approx 25$ nm. When the source contact is 25 nm, NDR is