Analysis of single electron traps in nano-scaled MoS₂ FETs at cryogenic temperatures

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Introduction. MoS_2 FETs hold the promise to overcome the challenges related to ultra-scaled FETs, as the 2D material MoS_2 allows to maintain sizable mobilities at the ultimate scaling limit [1]. However, the performance and long-term stability of many MoS_2 FETs is reduced by the hysteresis in the transfer characteristics and drifts in the threshold voltage [2]. It is challenging to identify the main cause for these phenomena in particular for the prototypelevel devices available. One method to isolate possible causes is to scale down the FETs, thereby reducing the number of active defects until the single-defect limit is reached (see Fig. (1a)). We analyze discrete steps in the drain current of nano-scaled FETs caused by single electron traps in random telegraph noise (RTN) and time-dependent defect spectroscopy (TDDS) measurements [3]. Going beyond previous RTN studies on MoS_2 FETs [4] we study RTN and TDDS at cryogenic temperatures below 100 K. We demonstrate experimentally for the first time that electron transfer rates to the trap sites become temperature independent below ≈ 50 K. Thus, charge trapping does not freeze out but retains its impact on the device behavior which is essential for devices operating at cryogenic temperatures such as devices for space applications, high-performance computing and quantum computing [5].

Devices and RTN Measurements. We fabricated nano-scaled MoS₂ FETs by mechanical exfoliation of few-layer MoS₂ on 20 nm SiO₂/Si. The channel was patterned on selected flakes by electron beam lithography and plasma etching followed by subsequent evaporation and lift-off of 60 nm Ni to define source and drain. In Fig. (1b) the schematic device layout and an atomic force microscopy (AFM) scan of the topography are shown. The transfer characteristics of a FET are given in Fig. (1c). Electrical measurements were performed under vacuum conditions ($p < 10^{-7}$ Torr) using custom-built electrical equipment [6]. Fig. (2a) shows an RTN trace recorded at $V_G = -1.51$ V and $V_D = 1$ V at 25 K. On this device we identified two independent electron traps that are distinguishable by the magnitude of the drain current steps $\triangle I$ caused by the charge trapping event, i.e. the step heights. The time constants are given by the time difference between subsequent capture and emission events and their distribution is shown in Fig. (2b). Fig. (2c) gives the gate voltage dependence of capture and emission times for the defect with larger $\triangle \overline{I} \approx 0.025 \,\mu\text{A}/\mu\text{m}$.

Defect Location and Temperature Dependence. The defect location in the device determines the gate voltage dependence of the capture and emission times. A defect deep in the oxide has a stronger voltage dependence as the trap level shifts more with applied bias, see the left part of Fig. (3a). The defect location was estimated to be $d \in [-0.7, -1.4]$ nm in the SiO₂ away from the interface. The atomic structure of the MoS₂/SiO₂ interface is shown in Fig. (3b). The defect was monitored from 10 K to 80 K. At low temperatures the time constants become temperature independent which is clearly visible in the Arrhenius plot at a voltage of $V_G = -1.3$ V in Fig. (3c). As predicted by theory [7], at cryogenic temperatures the electron transfer rate becomes temperature independent as the reconfiguration of atoms at the defect site is dominated by nuclear tunneling (tunneling of the nuclei through the barriers in the potential energy surface), see the right part of Fig. (3a). The temperature dependence of the rate is given by the theoretical lineshape function which fits the experimental data well (see Fig. (3c)) resulting in an activation energy of about $E_A \approx 65/85$ meV at higher T. Such a small activation energy is an indication for a defect close to the interface [8].

Trigger Trapping Events. By applying a charging voltage to the gate before recording the current we deliberately activated electron trapping in MoS₂ FETs. In a TDDS measurement sequence we applied $V_{G,S} = 16 \text{V}$ for $t_S = 100 \text{s}$ and directly after switching the gate bias to $V_{G,R} = 8 \text{V}$ recorded the drain current for $t_R = 100 \text{s}$. On a new device 100 traces for a stress of $t_S = 0.1/1/10 \text{s}$ were measured including the exemplary trace in Fig. (4a). The emission times are shown in Fig. (4b) for all events (blue) and the steps belonging to the cluster with a step height of about $\Delta \bar{I} \approx 3.7 \text{ nA}/\mu\text{m}$ (red). By repeating the same sequence for $T \in [20 \text{ K}, 100 \text{ K}]$ the temperature dependence of the emission time constant is analyzed in Fig. (4c) and the temperature independent emission rate in the cryogenic regime is confirmed.

Conclusions. We report the first experimental demonstration of gate voltage triggered single electron emissions in MoS_2 FETs, which is an indication for border traps. The gate voltage dependence of the defects analyzed points towards defects within 2 nm distance from the interface which agrees well with the small activation energies. This corroborates our understanding that the high defect density for MoS_2/SiO_2 devices is related to the properties of the MoS_2/SiO_2 interface that may intrinsically show a higher defect density if compared to Si/SiO_2 . In addition, we provide the experimental proof that at temperatures below $100 \, \text{K}$ the charge transfer process is dominated by nuclear tunneling and thus temperature independent. As a consequence charge trapping remains significant in MoS_2 FETs even at cryogenic temperatures and will have to be taken into account for device applications at these temperatures.

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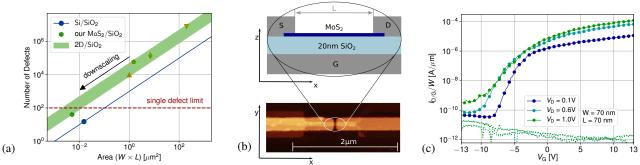


Fig. 1: (a) Single defect limit, given by the extrapolated number of defects per device area for Si/SiO_2 and $2D/SiO_2$ devices. (b) The schematic device layout of our nano-scaled multi-layer MoS_2 FETs including the AFM topography. (c) The transfer characteristics of a representative device (solid line - drain current, dotted line - gate leakage current).

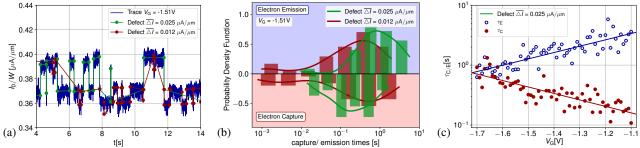


Fig. 2: RTN trace measured at 25 K showing two defects. (a) Part of the 100 s trace with steps of two different step heights corresponding to the two defects highlighted. (b) The capture and emission times of the two defects are extracted and the distribution of the times is shown. (c) Time constants as a function of gate voltage for the defect at $\Delta \bar{I} \approx 0.025 \,\mu\text{A}/\mu\text{m}$.

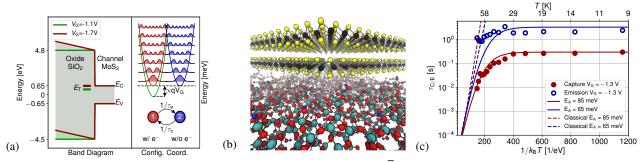


Fig. 3: Defect location and temperature dependence for the defect with $\triangle I = 0.025 \,\mu\text{A}/\mu\text{m}$. (a) E_T shifts by applying a gate voltage (left) and the vibronic transition of the defect between charged (1, red) and uncharged (2, blue) state (right). (b) The atomic structure of the interface of the MoS₂ channel and the amorphous SiO₂ where the defect is located. (c) Arrhenius plot at $V_G = -1.3 \,\text{V}$ including a fit of the lineshape function that dominates the temperature dependence of $\tau_{e/c}$.

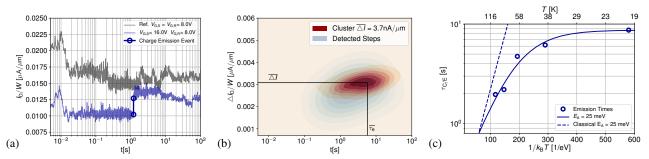


Fig. 4: A stress pulse at $V_{G,S} = 16 \text{ V}$ before the recovery trace triggers the emission of electrons in a TDDS measurement. (a) 25 TDDS traces for $t_s = 100 \text{ s}$ stress at $V_{G,S} = 16 \text{ V}$ and recovery at $V_{G,R} = 8 \text{ V}$ and 20 K. (b) All detected step heights (blue) and steps belonging to the cluster at $\Delta I \approx 3.7 \text{ nA}/\mu\text{m}$ (red). (c) Arrhenius plot of the emission times.

