2020 IEEE International Integrated Reliability Workshop (IIRW) 978-1-7281-7058-9/20/$31.00 ©2020 IEEE DOI: 10.1109/IIRW49815.2020.9312864

Modeling the Hysteresis of Current-Voltage Characteristics in 4H-SiC Transistors

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***Abstract*—4H-SiC MOSFETs exhibit a hysteresis of the transfer characteristics due to electrically active traps near the SiC/SiO$_2$ interface. Our measurements, conducted within the temperature range of 150-260 K revealed an interesting behavior, namely a notable decreasing hysteresis width towards higher T. During the up–sweep of gate voltage V_{gs} curves are shifted towards higher gate voltages compared to the curves acquired at the down–sweep of V_{gs}. This implies that more traps are negatively charged at higher V_{gs} conditions, and we attribute this behavior to acceptor–like border traps in oxide having its charge transition level 0/-1 near the SiC conduction band edge. To model electron capture and emission events of these oxide traps, we use the non–radiative multiphonon model. We calculate the capture and the emission times. The temperature dependence of the latter is the dominant feature which decreases the hysteresis width with increasing T. Our modeling approach is capable of reproducing the hysteresis width over the measured T range with good accuracy.**

***Index Terms*—Hysteresis, 4H-SiC, physical modeling, MOSFETs, non–radiative multiphonon model, border traps**

I. INTRODUCTION

Although silicon carbide (SiC) possesses a number of unique properties, which renders it an excellent material for high-power electronics, the disadvantage of SiC is its border traps close to the SiC/SiO$_2$ interface which deteriorates the channel mobility. [1]. Thus, the performance of fabricated SiC MOSFETs does not keep up with their hypothetical counterparts with idealized interfaces. A closely related issue typically observed in SiC devices, which stems from these border traps, is the hysteresis of current-voltage characteristics, see Figs. 1 and 3 [2, 3]. Consequently, a physically sound modeling approach is a vital component of understanding border traps in SiC transistors and should help to elaborate measures on how to suppress it and improve device performance. Recent efforts focused on modeling reliability issues in SiC devices were intensed in bias temperature instability and traps mediated behavior of current-voltage characteristics [2, 4–14]. However, to the best of our knowledge, a physics-based simulation framework, which captures the hysteresis in SiC devices, is still missing.

To accurately investigate this phenomenon we present a consistent physics based modeling approach that properly captures the complex hysteresis behavior of 4H-SiC MOSFETs over a wide temperature range, and for positive gate voltage only.

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II. DEVICES AND EXPERIMENT

The employed 4H-SiC device is of planar architecture with n$^+$ poly gate. This device has a gate length of 7.5 μm and a SiO$_2$ thickness of $\sim$50 nm. A SiO$_2$ film was grown by chemical vapor deposition followed by a post oxidation anneal in an NO ambient. Transfer $I_\mathrm{d} - V_\mathrm{gs}$ characteristics (where I_d is the drain current) were measured at a fixed drain voltage of V_ds = 0.1 V. Gate voltage up and down-sweeps were performed within a range of 0-20 V, a step size of 0.8 V, and a rate of $\sim$3.2 V/s. Measurements were conducted for different temperatures within the range of 150-260 K, see Figs. 1 and 3.

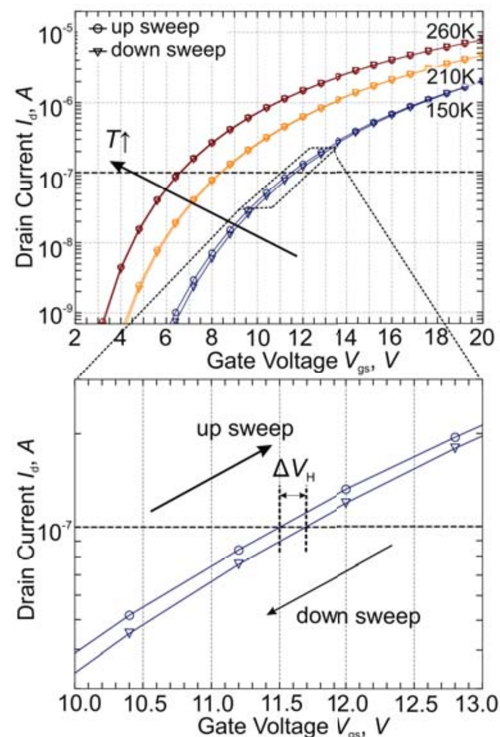

Fig. 1: A series of $I_\mathrm{d} - V_\mathrm{gs}$ curves measured over a wide temperature range between 150 and 260 K using gate voltage up– and down–sweeps. A reference current of 10^{-7} A was used to determine the hysteresis width taking the up and down sweeps into account; their difference determines the hysteresis width ΔV_H.

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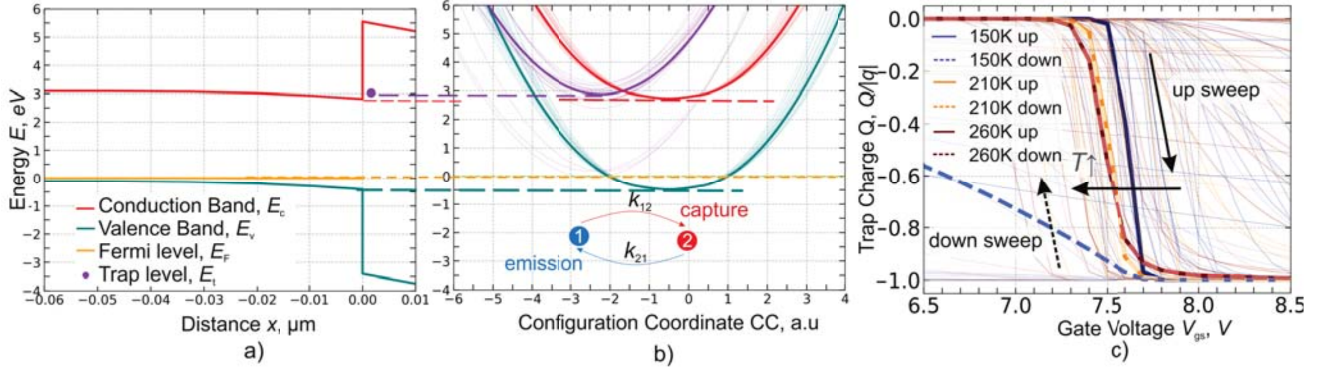

Fig. 2: a) The band diagram with the charge transition level of the acceptor–like trap used in the model at T = 260 K, V_{gs} = 0 V, b) the configuration coordinate diagram together with the schematic electron capture and emission reactions, c) the charge Q stored on a trap (in the elementary charge unit) as a function of V_{gs} for T = 150, 210, and 260 K. Thick lines represent the mean $Q(V_{\mathrm{gs}})$ curves.

The hysteresis width ΔV_{H} was defined as the difference between the gate voltages which correspond to a reference drain current (of 10^{-7} A) measured at up- and down-sweeps (the extraction procedure is shown in Fig. 1, bottom panel). Fig. 3 depicts the obtained width ΔV_{H} as a function of temperature T; one can see that ΔV_{H} decreases with T. In other words, the hysteresis becomes more pronounced at lower T and negligible at high temperatures.

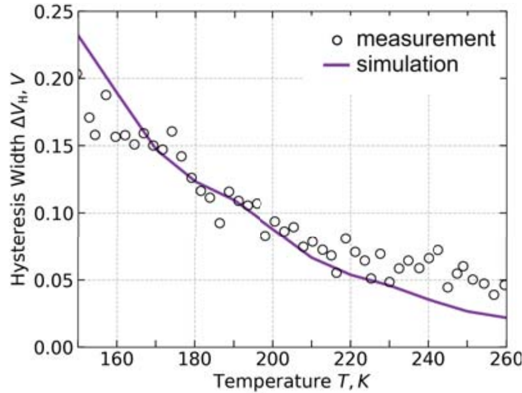

Fig. 3: Simulated vs. measured ΔV_H values as functions of temperature T.

III. The Modeling Framework

Fig. 1 (top panel) shows that the threshold voltage V_{th} shifts by 5 V towards lower gate voltage when the temperature increases. At low temperatures (Fig. 1, bottom panel) the current-voltage curves measured during the down-sweep exhibit a positive shift compared to the corresponding up-sweep curves, thereby suggesting that the involved defects become more negatively charged with increasing V_{gs}. We assume that the observed hysteresis originates from acceptor-like traps (with charge states 0/-1) located in the SiO_2 layer which can capture charge carriers from the SiC substrate [15]. At elevated temperatures, these traps are neutralized due to the T dependence of capture and, in particular, emission times. Therefore, the threshold voltage drift, i.e. the hysteresis width, reduces towards higher T. The trap levels are assumed to be normally distributed with a mean value of $\langle E_{\mathrm{t}} \rangle$ = 0.07 eV above the SiC conduction band edge (the position of the charge transition level, see Fig. 2b) and a standard deviation of σ_{E} = 0.15 eV.

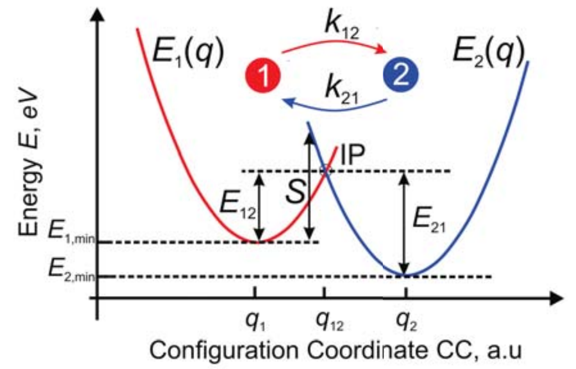

Fig. 4: Schematic configuration coordinate diagram of the two-state non–radiative multiphonon model for describing capture k_{12} and emission k_{21} rates of individual traps.

The capture and emission times of each defect can be described by a two-state non–radiative multiphonon (NMP) model for two charge states which are represented by the potential energy surfaces $E_1(q)$ and $E_2(q)$ (where q is the configuration coordinate), and correspond two parabolas, see Fig. 4 [16, 17]. In this case state 1 corresponds to the minimum energy $E_{1,\mathrm{min}}$ when an electron is at the trap and equals the trap level, and state 2 corresponds to the minimum energy $E_{2,\mathrm{min}}$ when an electron is in the channel and conventionally equals conduction band edge, see Fig. 2b. When this trap system switches from state 1 to state 2, electrons are emitted to the channel with corresponding capture time τ_{c} and is determined by the barrier E_{12}. Opposite of this, when this trap system switches from state 2 to state 1, electrons are captured by the traps with corresponding emission time τ_{e} and is determined by the barrier E_{21}.

These energy barriers are given by the intersection point (IP) (Fig. 4) of the two trap states represented by $E_1(q)$ and $E_2(q)$ and described by equation (1) [17].

$$
\begin{aligned}
E_1(q) &= E_{1,\mathrm{min}} + c_1(q - q_1)^2 \\
E_2(q) &= E_{2,\mathrm{min}} + c_2(q - q_2)^2 \\
R^2 &= \frac{c_1}{c_2}, \qquad S = c_1(q_2 - q_1)^2
\end{aligned}
\tag{1}
$$

Where c_1, c_2 are curvature, and q_1, q_2 are configuration coordinate for each state of the system. The energy barriers

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E_{12} and E_{21} have been adjusted by changing the respective fundamental underlying parameters such as the relaxation energy S and the trap level E_t. The number of traps N_t had been taken into account for the quantitative correct shift of V_th and the hysteresis width ΔV_H. Traps are randomly located from the SiC/SiO_2 interface to the 1 nm depth in oxide, and the parabolic curvature ratio R assumed constant, see Table I.

To calculate capture and emission times we used band edge approximation, see equation (2) [18].

$$\begin{aligned} \frac{1}{\tau_c} &= k_{12} = n v_{th,n} \sigma_{0,n} \nu_n \mathrm{e}^{-\frac{E_{12}}{k_B T}} \\ \frac{1}{\tau_e} &= k_{21} = n v_{th,n} \sigma_{0,n} \nu_n \mathrm{e}^{-\frac{E_{21}}{k_B T}} \end{aligned} \quad (2)$$

Where n is electron concentration, $v_{th,n}$ is the thermal velocity, $\sigma_{0,n}$ is the effective capture cross section, ν_n is the tunneling factor, k_B is the Boltzmann constant.

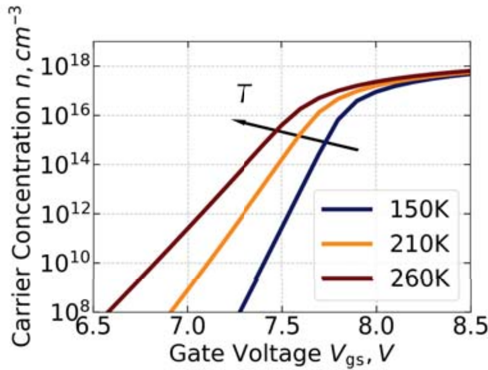

Fig. 5: Carrier concentrations in the channel at T = 150, 210 and 260 K.

TABLE I: Parameters for modeling.

Parameter	Value	Unit
Trap concentration, N_t	10^{19}	cm^{-3}
Trap distance from the interface, x_t	$0 \ldots 1$	nm
Relaxation energy, $\langle S \rangle$, σ_S	0.8 ± 0.1	eV
Parabolic curvature ratio, $\langle R \rangle$, σ_R	1 ± 0.01	1
Trap level energy $\langle E_\mathrm{t} \rangle$, σ_{E_t}	$E_\mathrm{C} + 0.07 \pm 0.15$	eV

Note that we do not aim to model a self–consistent response of the charged traps onto the electrostatics. Instead, we employ the charge sheet approximation, i.e. the effective gate voltage is calculated as a post processing step taking the total charge in the oxide layer into account. To model capture and emission, we employ the NMP model [17, 18] implemented in the device and circuit simulator MiniMOS-NT [19] used within the GTS framework [20].

IV. Results and Discussions

Our simulated result of the hysteresis width together with measurement is shown in Fig. 3. One can see that the hysteresis width decreases when temperature increases. To explain this trend, we have calculated capture τ_c and emission τ_e times (in the two-state configuration of the NMP model they are equivalent to the reciprocal capture/emission rates [16, 17]) as a function of the gate voltage and are described by (2), see Figs. 6 and 7. The electron capture and emission rates are determined by the energy barriers E_{12} and E_{21}, respectively, see Fig. 4. The asymmetry of those barriers introduces a disparity between the capture and the emission rates.

During the up-sweep, when $V_\mathrm{gs} < V_\mathrm{th}$ the barrier E_{12} is small, electrons are emitted to the channel (Fig. 6), and traps are neutralized. This behavior can be represented by the charge Q (normalized to the elementary charge) stored on a single trap plotted as a function of V_gs, see Fig. 2c.

In strong inversion ($V_\mathrm{gs} > V_\mathrm{th}$), the conduction and valence band bends and the Fermi level partly "scans" the SiC band gap. At elevated T the electron concentration in the channel increases already at low gate voltages due to an enhanced carrier generation rate (Fig. 5), and electrons are captured by the traps, see Fig. 7. In this regime, electrons are stored on traps and the traps are predominantly in the -1 charge state, see Fig. 2c.

Whereas during the down-sweep electrons are captured by the traps but barrier E_{12} is small and they tend to be emitted back to the channel. At low temperature, the capture time is long and lies outside the measurement window (Fig. 6), and only a few electrons are stored on traps, see Fig. 2c dashed lines.

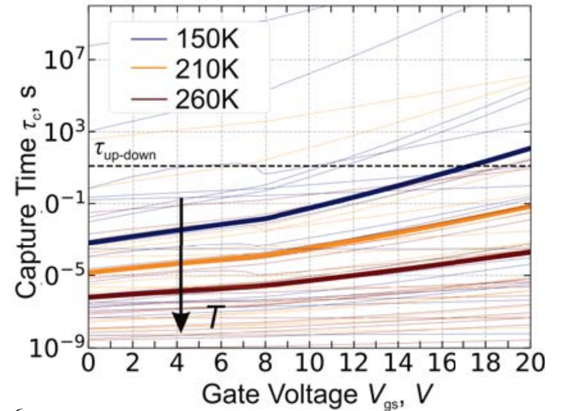

Fig. 6: Simulated capture time as functions of V_gs for three different temperatures, namely T = 150, 210, and 260 K. The plot shows 20 selected traces (thin lines) together with the mean characteristics (thick lines) which take all defect configurations into account.

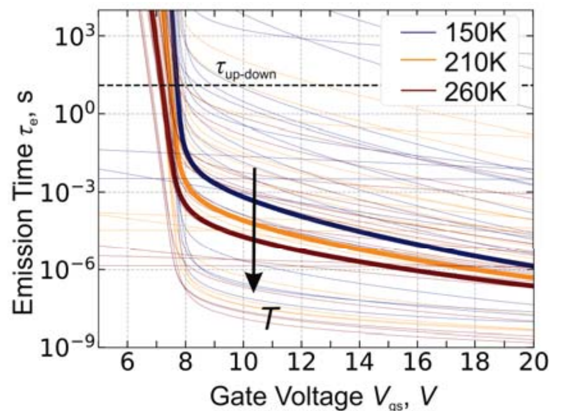

Fig. 7: Simulated emission time as functions of V_gs for three different temperatures, namely T = 150, 210, and 260 K.

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As can be seen in Fig. 2c, $V_{\rm gs}$ at which the charge transition process ($0 \rightarrow$ -1 transition) occurs is decreased at higher T, leading to a decreasing asymmetry in the charge and discharge rates and, hence, a reduced hysteresis width.

The traps capture and emit electrons with substantially different rates (which are characterized by a broad dispersion). These traps are not in a quasi–equilibrium state within the experimental time window. At higher temperatures, during the down-sweep, the emission process has a shorter characteristic time (higher rate), as shown in Figs. 6 and 7, and the ratio of capture and emission time is small, therefore resulting in a narrower hysteresis width, see Fig. 3.

However, at low temperatures, during the down sweep, not all traps have already emitted their charges and some remain negatively charged because the capture time is longer than the emission time. The ratio between these times is large. Exactly this remnant charge is stored on traps (electrons which were not released) and is responsible for the large hysteresis width $\Delta V_{\rm H}$, see Fig. 3.

Finally, *our modeling framework can capture* the experimental dependency of the *hysteresis width* over the entire T range with *good accuracy*.

V. Conclusions

We showed that physical modeling of charge capture and emission by/from in pre–existing defects is capable of describing the observed transfer characteristic hysteresis of 4H-SiC transistors during gate voltage sweeps over a broad temperature range. The charging and discharging kinetics of the responsible acceptor–like traps, with 0/-1 charge transition levels around $\sim$0.07 eV above the SiC conduction band, has been described by applying the non–radiative multiphonon model. The ratio of the respective charge capture- and emission times is determined by the energy barriers E_{12} and E_{21}. The dependence of these barriers on T and $V_{\rm gs}$ determine the exhibition of the hysteresis. Furthermore, our approach is consistent with the observed temperature dependence of the hysteresis and capable of adequately capturing the changing width with temperature.

Acknowledgements

The financial support by the Austrian Federal Ministry for Digital and Economic Affairs and the National Foundation for Research, Technology and Development, and Austrian Science Fund (FWF), project No. 31204-N30 is gratefully acknowledged.

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