# Defect Spectroscopy in SiC Devices

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***Abstract*— Transistors employing silicon carbide (SiC) substrates exhibit excellent electrical properties for high-voltage power conversion applications. Even though the fabrication processes of SiC transistors are continuously optimized the exploitation of their full potential is still limited by a significant number of defects. The defects can be generally classified into interface states and oxide traps, and are responsible for degradation of device performance over time. In principle, by exchanging a carrier with the conducting channel, the defects can perturb the surface potential, alter the threshold voltage, and thus affect the current flux through the channel. It has been observed, that the altering of the threshold voltage is more severe for SiC devices than it is for conventional Si transistors. In order to collect measurement data different characterization methods and the respective consequences for charge trapping considering planar SiC MOS transistors are discussed. To describe the observed drift of the threshold voltage charge trapping of individual defects is considered and described using the non-radiative multiphonon model. Finally, a brief summary of possible defect candidates which have been discussed in the literature is given.**

## I. Introduction

Transistors fabricated on substrates utilizing wide-bandgap materials such as gallium nitride (GaN) or silicon carbide (SiC) have shown a lot of promise for high-voltage applications [1, 2, 3, 4, 5]. In particular, a lot of effort has been put into the development of SiC metal-oxide-semiconductor (MOS) transistors as they provide *(i)* a much lower specific on-resistance for a given blocking voltage and *(ii)* can operate at higher temperatures compared to conventional Si transistors [4]. The advantages of SiC based MOS transistors arise from the superior properties of SiC, such as high breakdown voltage, large bandgap, and high thermal conductivity, see Table I. Furthermore, compared to GaN or other wide-bandgap materials SiC has the ability to form silicon oxide ($SiO_2$) as its native oxide, which makes SiC even more attractive for the fabrication, as the electrical properties of $SiO_2$ have been extensively studied for many decades for Si technology. Note that crystalline SiC can be grown in several polytype variants, amongst which the 4H-SiC polytype is mainly used for power devices as it shows the highest electron bulk mobility among all polytypes. This polytype is commonly referred to throughout this work when considering SiC devices.

| Property | | Si | 4H-SiC | unit |
|---|---|---|---|---|
| $E_G$ | bandgap at $T = 20\,^{\circ}C$ | 1.12 | 3.26 | eV |
| $v_{sat}$ | saturation velocity | 1.0 | 2.2 | $10^7\,cm\,s^{-1}$ |
| $v_{crit}$ | critical electrical field | 0.3 | 2.8 | $MV\,cm^{-1}$ |
| $\varepsilon_r$ | relative permitivity | 11.7 | 9.76 | 1 |
| $\mu_n$ | bulk electron mobility | 1500 | 1200 | $cm^2\,V^{-1}\,s^{-1}$ |
| $\mu_p$ | bulk hole mobility | 480 | 120 | $V^{-1}$ |
| $\kappa_{th}$ | thermal conductivity | 1.5 | 4.9 | $W\,cm^{-1}\,K^{-1}$ |

**TABLE I:** The material parameters of Si and 4H-SiC showing the superior properties of SiC for power MOS transistors [7].

### A. Device Structures

Typical device structures for MOS transistors are shown in Figure 1. The planar MOS structure has been used during the development of the fabrication process and to analyze interface/bulk carrier mobility where dedicated hall structures are employed. Also charge trapping has been analyzed in such structures, though planar MOS transistors are not considered for commercial SiC power devices. As the blocking voltage of planar devices is determined by the bulk doping and the distance between the drain and source contact, devices with high blocking voltages would require a very large chip area. For power MOS transistors typically DMOS transistors, as shown in Figure 1(b), have been used. The on-resistance of such a SiC DMOS transistor is basically determined by the channel resistance due to the typically lower electron mobility than in the drift region. To further reduce the channel resistance without the need to increase the required chip area so called trench MOS transistors, i.e. vertical MOS transistors, can be used, see Figure 1(c). One big advantage of trench devices is that the conducting channel can be fabricated to be aligned along a-face plane, which exhibit higher electron mobility than channels aligned along the Si-face plane [6].

As in Si MOS transistors, the performance of SiC transistors is seriously affected by defects which can be located in the oxide and at the oxide/semiconductor interface, see Figure 1 (red symbols). Although the fabrication of SiC MOS transistors is to some extend compatible with the well-established processes used in Si technology, both the standard thermal oxidation process on SiC and the deposition of the oxide on SiC results in a considerably increased number of interface states as compared to the thermally grown $SiO_2$ on Si substrates. By introducing a post oxidation anneal (POA) in nitric oxide (NO), the electrical properties of the $SiO_2$/SiC interface have been significantly improved, enabling commercial available SiC MOS devices [8, 9, 10, 11, 12, 13]. However, the channel mobility observed for these devices is still significantly lower

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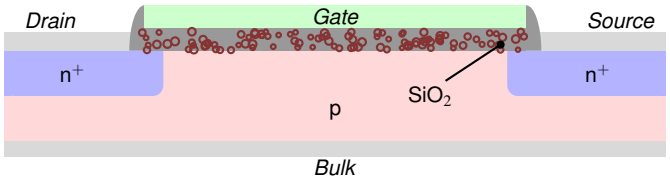
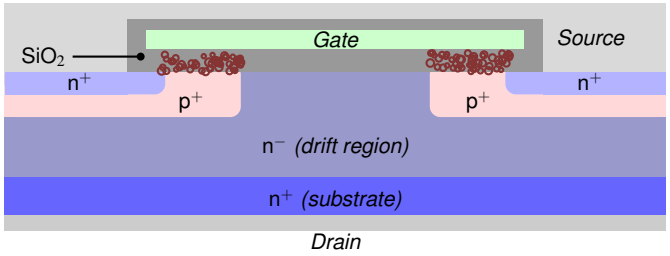
(a) Planar MOS Transistor




(b) DMOS Transistor




(c) Vertical MOS Transistor

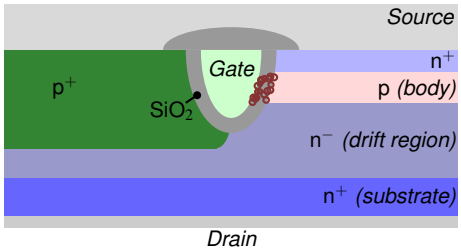



**Fig. 1:** The **(a)** planar MOS structures have been used to develop the fabrication processes, and to study the impact of annealing processes on the carrier mobility. In order to increase the blocking voltage and the current rating of the devices at reasonable chip area lateral device structures like **(b)** DMOS transistors and **(c)** trench devices are commonly used in power electronics. In all three device structures the active channel area is marked by the position of possible defects leading to a drift of the threshold voltage during operation are highlighted.

than the bulk mobility. Further improvement of the channel mobility has been achieved by using $NH_3$ for POA [14], where an improved mobility in the range of $\mu$ =50-60 $cm^2/Vs$ ($\mu$ =35 $cm^2/Vs$ for NO annealed samples [15]) could be observed [16].

### *B. Characterization of Devices and Defects*

The overall performance of SiC transistors has been significantly improved over the last years, but their characteristics is still affected by a number of existing defects. For SiC devices a defect density in the range of $N_{it} \approx 10^{12} - 10^{13} cm^{-3}$ has been reported [8], which is about a factor of hundred higher than in Si devices where values in the range of $N_{it} \approx 10^{10} - 10^{11} cm^{-3}$ are typically observed. The higher observed defect density is consistent with recent reports where the hysteresis of voltage sweeps [17] and BTI [18] have been investigated. To characterize the hysteresis of a device a voltage sweep measurement is performed at a constant sweep rate and the drain current is recorded. Particularly in the case of SiC transistors an almost fully recoverable variation of the shift of the threshold voltage of more than 1V can be observed for these measurements [17]. To characterize BTI, a constant voltage is applied at the gate terminal of the transistor and the drain current through the transistor is measured over time. The so observed drift of the current can afterwards be converted to an equivalent drift of threshold voltage. To accelerate BTI degradation for the sake of enabling characterization within reasonable measurement times typically large gate biases which are significantly higher that nominal operating voltages are applied. By doing so drifts of the $\Delta V_{th}$ of SiC devices can be studied efficiently [18, 19, 20]. Both observations, hysteresis of voltage sweeps and BTI, can be attributed to repeated charging and discharging of interface states and oxide defects, which is discussed later in more detail.

For a defect to be able to affect the behavior of a transistor its charge transition level (CTL), or at least one of its CTLs if several exist, must lie in the so-called active energy region (AER) of the respective operational case. Considering measure-stress-measure (MSM) experiments a defect can become charged if its CTL is shifted below the Fermi-level of the channel during the stress phase, i.e. the phase when typically a high bias is applied at the gate. After switching the gate bias back to a value around the threshold voltage $V_{th}$ of the device, the defect can emit its charge if its corresponding CTL is shifted above the Fermi-level of the channel. During the phase in which a low gate bias is applied typically a drift of the current can be observed, which is due to the superposition of charge capture and emission events of a large number of single defects. The limits for the energetic area covered by the AER is determined by the breakdown field of the oxide.

Next to altering of the threshold voltage leakage currents through the insulator can provide important information on the defect density. To measure such currents gate voltages fairly exceeding the nominal device operating conditions have to be applied. Quite recently leakage currents have been studied for SiC MOS transistors considering NO and $NH_3$ POA anneal [16]. For NO annealed samples only gate leakage current contributions from Fowler-Nordheim tunneling which is dominating at high electric fields could be observed. But for $NH_3$ a small increase of the gate leakage at low fields might give rise for trap-assisted-tunneling. Thus the advantage of the improved mobility of $NH_3$ annealed devices comes with the disadvantage of an slightly increased gate leakage current.

### *C. Importance of Accurate Description of Device Behavior*

A correct and consistent description of the above mentioned reliability phenomena is generally important for the development and simulation of integrated circuits [19]:

(i) Large device-to-device variation of the threshold voltage, defect density, and defect distribution can lead to an unbalanced operation of SiC MOS transistor when connected in parallel modules. This issues is even more severe for SiC technology due to higher trap density compared to Si devices.

(ii) The approximation

$$R_{\mathrm{ch}} \approx \frac{L}{W \mu_{\mathrm{n}} C_{\mathrm{ox}} (V_{\mathrm{G}} - V_{\mathrm{th}})}$$

for the channel resistance $R_{\mathrm{ch}}$ reveals that a drift of the threshold voltage can cause a significant change of the on-resistance ($R_{\mathrm{on}} \propto R_{\mathrm{ch}}$) too. As larger drifts of the threshold voltage $\Delta V_{\mathrm{th}}$ are observed for SiC transitors than for Si devices [17, 18], considering a variation of the channel resistance could be of interest for certain applications.

(iii) A decrease of the threshold voltage below a certain value can cause a parasitic turn-on which is detrimental for the functionality of the circuit and for the power consumption of the device and circuit.

Furthermore, a reliable extraction of the device lifetime under different operating conditions strongly relies on the accuracy of the employed model. To describe the observation mathematical formulas based on a power-law are often used. However, in the general case of BTI the power-law is not able to explain the saturation of the shift of threshold voltage $\Delta V_{\mathrm{th}}$ with increasing stress time, but converges to infinitely large $\Delta V_{\mathrm{th}}$ which makes the model non-physical [21]. Another approach, which has been successfully developed to describe charge trapping and BTI for Si devices, relies on the physical modeling of charge trapping kinetics of individual defects employing the non-radiative multiphonon theory [22, 23]. By considering the overall measured device degradation as the superposition of many of such defects the bias- and temperature dependence of the drift of the threshold voltage can be nicely explained [18]. In the following, recent advances in defect modeling and characterization will be discussed followed by an overview of possible candidates for defects in SiC transistors.

## II. Modeling of Charge Trapping in MOS Devices

To explain charge trapping empirical models are often used due to their simplicity. However, they can not explain the intricate behavior of charge trapping. Another approach has been proposed by Tewksbury [24] who has assumed elastic tunneling between carriers from the substrate and defects in the oxide as the origin for charge trapping. During an elastic tunneling process the charge carrier does not change its energy, i.e. the defect in the oxide has the same energy level as the carrier in the channel. However, the charge transition times from elastic tunneling are proportional to the trap depth $\tau \propto \exp(-x/x_0)$ [25], and thus only a narrow distribution of charge emission times can be described for devices with thin oxides [26]. Also, elastic tunneling is inherently temperature independent, and thus does not enable to describe the strong temperature activation of charge trapping as well as the asymetric stress and recovery behavior [27].

A promising modeling approach is based on a stochastic charge trapping model considering the overall degradation behavior of the device as the superposition of contributions

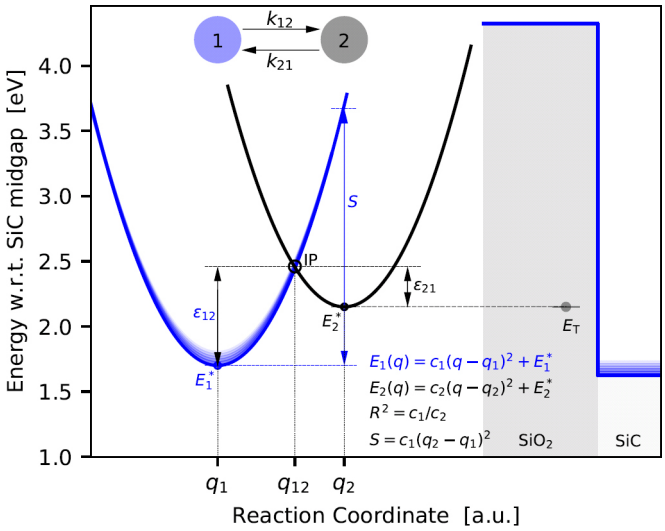



**Fig. 2:** The two-state NMP model can be used to describe the charge trapping dynamics of individual defects. In this representation where electron traps are considered state '1' refers to the ground state and state '2' is considered the charged state. In order to capture a charge from a carrier reservoir, i.e. from the conduction band, the carrier has to overcome a certain energy barrier $\varepsilon_{12}$. It has to be noted that the barriers for forward and backward transitions $\varepsilon_{12}$ and $\varepsilon_{21}$ depend on the applied gate bias, as the position of the trap level w.r.t. the conduction band shifts with the gate voltage.

from a multitude of single defects. The charge trapping kinetics of each defect is further described by the non-radiative multiphonon (NMP) theory [28]. As computation of the complex equation system of the NMP model for a large number of defects contributing to the behavior of real devices is very inefficient, the charge transfer transitions of the defects are calculated from energy barriers which have to be overcome to change the charge state, see Figure 2. The energy barriers are derived from the intersection point of two parabolas which approximate the potential energy surfaces for the two charge states close to the defect site. As such, in this model each defect is described by a two-state Markov chain, and in the classical formulation the transition between the two states is determined by the barrier height $\varepsilon_{12}$ or $\varepsilon_{21}$ for charge capture and charge emission, respectively. For an nMOS transistor, state '1' can be considered as the minimum energy of an electron dwelling in its reservoir, which is considered the conduction band edge. State '2' describes the minimum energy of the carrier aside the defect itself, i.e. the so called trap-level. The trap-level of a defect given by $E_2$ further shifts with an applied gate voltage depending on the trap position

$$E_2(V_{\mathrm{G}}) = \frac{-q(V_{\mathrm{G}} - \psi_{\mathrm{s}})}{t_{\mathrm{ox}}} x_{\mathrm{T}} + E_{\mathrm{T0}} \tag{1}$$

where $\psi_{\mathrm{s}}$ is the surface potential, $x_{\mathrm{T}}$ is the position of the trap referred to the interface, and $E_{\mathrm{T0}}$ is the trap level at zero gate bias.

In principle, the two states of the model can be described by a Markov chain, which assumes a memory-less system, i.e. the charge transition depends only on the current state and not on its history. By doing so analytical expression can be derived

for charge capture and charge emission [22, 23]. To efficiently simulate the impact of a large number of defects on the drift of the threshold voltage $\Delta V_{\mathrm{th}}$ a 1D compact physics modeling framework (Comphy) has been recently proposed [23]. So far Comphy has been used to explain BTI in Si technologies, but has been recently extended to model charge trapping in SiC transistors [18]. The computation of charge trapping relies on the two-state defect model, and for the estimation of the trap-depth dependent contribution of a defect $\Delta V_{\mathrm{th,i}}$ Comphy makes use of the charge sheet approximation

$$\Delta V_{\mathrm{th,i}} = -q\frac{1}{C_{\mathrm{ox}}}\left(1-\frac{x_{\mathrm{T}}}{t_{\mathrm{ox}}}\right) \tag{2}$$

with the elementary charge $q$, the oxide capacitance $C_{\mathrm{ox}}$. The total change of the threshold voltage $\Delta V_{\mathrm{th}}$ can be finally computed as the sum of contributions from a large ensemble of defects. In the following section recent characterization results and the respective modeling approaches will be discussed.

## III. Characterization and Simulation of SiC Device Behavior

The intuitively most straight-forward method to characterize a device is to perform an $I_{\mathrm{D}}(V_{\mathrm{G}})$ sweep. However, already during $I_{\mathrm{D}}(V_{\mathrm{G}})$ measurements a certain number of defects can capture and emit their charge, perturb the surface potential of the device and alter the device characteristics. In order to provide a physical explanation of the behavior of the devices under test the detailed knowledge of the entire measurement history is essential. Considering the device history becomes even more important the larger the number of defects which contribute to changes of the device performance gets. With high trap densities also challenges for simulations evolve. In this case the simulations should preferably be carried out self-consistently to consider the feedback of the trapped charge at every simulation step to ensure high accuracy of the simulation results.

Next to the device history, the timing of any sequence and measurement delays are further crucial parameters for the characterization of SiC transistors [29, 30]. Lelis *et. al* [31] showed, that in the case of SiC devices, if the measurement time for a voltage sweep is reduced from 1 s to 20 µs the measured threshold voltage $V_{\mathrm{th}}$ can be by a factor of four larger. The measurement delays can for instance be optimized by increasing the sampling rate, i.e. increasing the signal bandwidth. However, this also enhances the noise of the recorded signals and reduces the measurement resolution which adversely affects the accuracy of the extraction. But employing an accurate description of the device behavior can compensate for the lack in high speed measurements. Furthermore, an accurate physical description of the device behavior is essential to estimate the time-to-failure under various operating conditions.

By extending the $I_{\mathrm{D}}(V_{\mathrm{G}})$ measurements with a subsequent down-sweep of the gate bias to its initial value a significant hysteresis of the transfer characteristic can be observed [17, 32, 33]. Another technique which is typically used to characterize BTI relies on repeatedly applied stress-measurement cycles with iteratively increasing stress time, so called extended measure-stress-measure (eMSM) measurements [34]. By doing eMSM experiments the drift of the threshold voltage $\Delta V_{\mathrm{th}}$ can be studied over time thoroughly. As previously mentioned, for both techniques the exact timing of the experiments, and measurement delays is of utmost importance as this can lead to certain inaccuracies for the interpretation of the observed degradation.

### A. Voltage Sweep Measurements

In [35, 36] the deviation between real and idealistic device $I_{\mathrm{D}}(V_{\mathrm{G}})$ characteristics of SiC transistors has been explained considering interface traps modeled using the Shockley-Read-Hall model. Furthermore, the temperature dependence of $I_{\mathrm{D}}(V_{\mathrm{G}})$ curves measured in the range of 300 K up to 500 K could also be nicely explained. For their simulations the density of interface states has been considered consistently as proposed by Afanas'ev *et. al* [37], which has been extracted from deep level transient spectroscopy measurements, see Figure 6 (column labeled $\mathrm{N_{it}}$). Later Tyaginov *et. al* [38] showed that considering only the impact of interface states the increase of the drain current measured in strong inversion of the transistor towards higher temperatures cannot be explained properly. They extended their simulation setup by two trap bands, one donor trap band ($\approx 1.36$ eV above SiC mid-gap) and one acceptor trap band ($\approx 0.06$ eV above SiC mid-gap) which enabled the proper explanation of the temperature dependence of the $I_{\mathrm{D}}(V_{\mathrm{G}})$ characteristics in the temperature range of 200 K to 350 K. The charge transitions of the considered border traps have been modeled employing the previously discussed effective two-state NMP model. Furthermore, their extracted trap-levels showed good agreement with CTLs of nitrogen related defects $N_{\mathrm{C}}V_{\mathrm{Si}}$ [39], see Figure 6.

### B. Hysteresis Measurements

The sub-threshold hysteresis of the drain current of SiC nMOS devices has been investigated in [17]. For this up- and down-sweeps of the gate voltage have been measured without any interrupt, considering a different rise and fall time for the voltage sweep. It has been observed, that the width of the hysteresis strongly depends on the low value of the gate bias used for the sweep, see Figure 3. As can be seen, the more negative the gate bias is the larger the hysteresis becomes. This behavior can be explained by an increase of the AER for charge trapping with decreasing gate bias. Furthermore, due to different time intervals used for the up- and down-sweep the traps have more time to capture a charge during the up-sweep, as for charge emission during the down-sweep. As for voltage sweeps typically a large AER for charge trapping is being scanned, such measurements can be used to estimate the border states within the band-gap of SiC. Next to the observed dependence of the width of the hysteresis on the gate bias, the width of the hysteresis tends to become constant when the

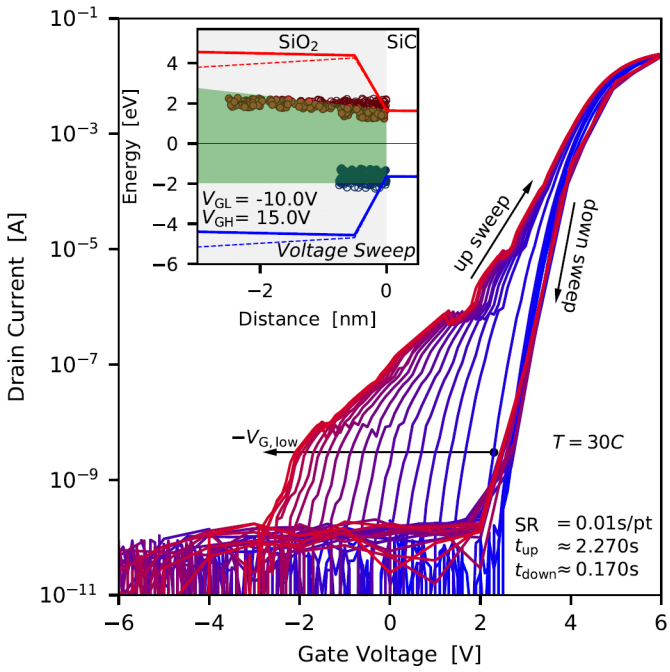



**Fig. 3:** A series of up- and down-sweeps of the gate voltage have been measured and analyzed in [17]. As can be seen, a clear hysteresis of the voltage sweep characteristics can be observed. The width of the hysteresis increases with decreasing gate bias, as the active energy region of the sweep increases. In the inset, the band diagram with the AER (green) is shown. The indicated trap bands for electron and hole traps have been extracted from eMSM measurements in [18].

Fermi-level of the channel approaches the valence band of SiC. Thus defects in the mid-gap of SiC are considered to affect the hysteresis, while electron traps close to the conduction band and hole traps close to the valence band of SiC are considered to affect the mobility [17] and are responsible for a change of the threshold voltage over time [18].

Rescher *et. al* further compared the hysteresis behavior of a Si-face (planar) and an a-face (trench) MOS transistor. From the more pronounced hysteresis of the trench transistor it can be concluded that a higher border state density around the mid-gap of SiC has to be present in these devices, compared to the planar SiC MOS devices. However, the trench devices exhibit a significantly higher mobility when operated in full inversion. As the hysteresis has no major relevance for device reliability in high power switching applications the higher carrier mobility of the trench MOSFET makes this structure more performant than planar MOS devices.

### C. Measure-Stress-Measure Characterization

The most established method to characterize BTI is to perform eMSM measurements where each measurement cycle consists of a stress and a recovery phase, see Figure 4. During the stress phase a typically large bias is applied at the gate terminal of the transistor, while all the other terminals are kept at zero volt. In this phase the defects which have their trap level below the Fermi-level of the channel can become

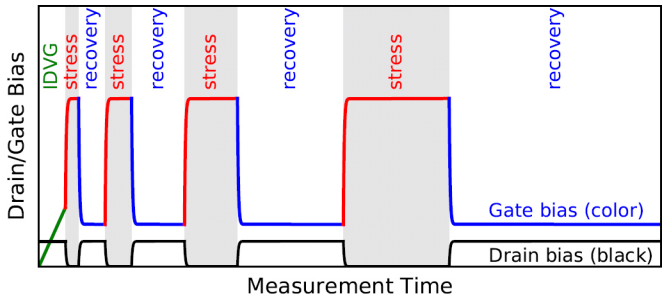



**Fig. 4:** Initially an $I_D(V_G)$ characteristics of a pristine device is measured and later used to convert the recovery drain current into an equivalent drift of the threshold voltage $\Delta V_{th}$. Typical for an eMSM sequence are the repeatedly applied phases of stress and recovery bias. After each cycle the stress time and the recovery time is increased. It has to be noted, that the initial $I_D(V_G)$ affects the charge state of a number of traps, and thus has to be considered during the simlations [18].

charged, if their charge capture time is small compared to the stress time. After the stress time has elapsed the gate bias is switched to the recovery bias, which is typically in the order of the threshold voltage of the device, and additionally a drain bias is applied. During the recovery phase the charged defects can transit to the neutral state if their trap-level is shifted above the Fermi-level of the channel when switching from the stress bias to the recovery bias. The superposition of the many charge emission events of defects can lead to a decrease of the threshold voltage over time, which can be measured as a drift in the drain current when the applied biases are kept constant. Afterwards the drain current is typically converted to an equivalent drift of the threshold voltage $\Delta V_{th}$ using an initially measured $I_D(V_G)$ characteristics.

As pointed out in [31] the measurement delay is a crucial parameter for the characterization of SiC transistors. Furthermore, apparently simple voltage sweeps used for $I_D(V_G)$ measurements can already lead to a remarkable change of the threshold voltage $V_{th}$ and modify the device electrostatics of a pristine transistor. In order to achieve highest accuracy for the modeling part the entire history of the device in terms of applied biases and timing has to be considered during the simulations. Thus, each eMSM sequence is applied as shown in Figure 4 and is measured without any interrupt. To determine the defect parameters to explain the measurement data the entire eMSM sequence is simulated using Comphy.

*1) Classical MSM:* For the classical eMSM sequences the interface of the SiC transistor is put into inversion by applying a large positive stress bias. The AER region for these experiments is arranged above the Fermi-level of the channel and thus mainly the impact of electron trapping on the $\Delta V_{th}$ can be studied. In Figure 5 a good agreement between contributions of extracted electron trap bands and experimental data can be observed. In [18] a fast electron trap band has been proposed to capture the fast recoverable component after stress release, and a shallow electron trap band has been introduced the explain the long-term recovery data. The combination of contributions from both trap bands enable to explain the

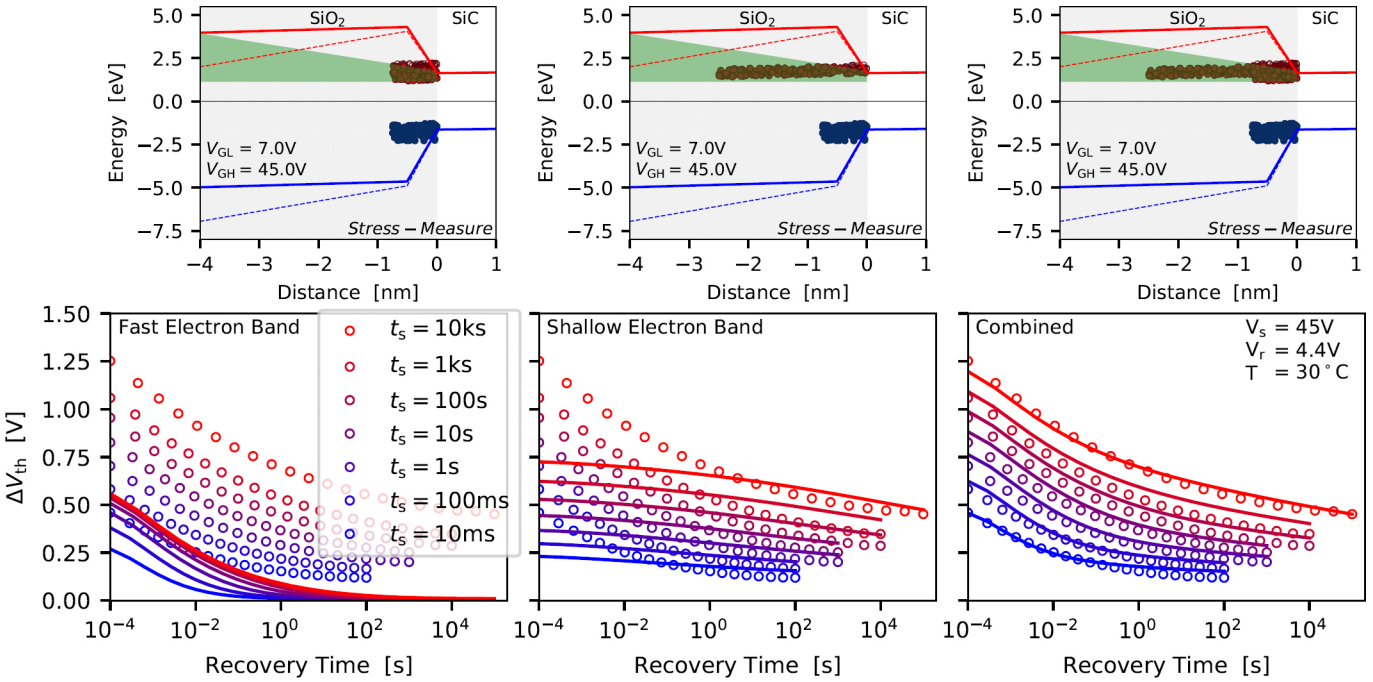



**Fig. 5:** (**top**) The band diagrams with the respective active energy region for charge trapping (green) are shown for (**top, left**) the fast electron trap band, (**top, center**) the shallow electron trap band, and (**top, right**) the overall trap distribution which has been proposed in [18] to explain the (**bottom**) eMSM sequence measured employing a planar SiC MOS transistor. As can be seen, the traps assigned to the fast electron trap band describe the recovery behavior immediately after stress release, while the shallow electron trap band captures the slowly recovering component. The superposition of all trap contributions nicely explain the overall drift of the threshold voltage. For the sake of completness, the hole trap band (blue) is also shown, which has been extracted using pulse MSM measurements [18].

experimental data. For the sake of completeness it has to be mentioned that in [18] eMSM sequences at different biases and temperatures have been evaluated too in order to account for the bias- and temperature dependence of charge trapping. The extracted trap levels show nice agreement with CTLs of various possible defect candidates, see Figure 6, which will be discussed later.

*2) Pulse MSM:* When classical MSM measurements are applied to an nMOS transistor, typically the contribution of electron traps is studied. If the measurement sequence is now extended by an additional accumulation pulse after the stress phase, but before the recovery phase, the AER for charge trapping can be significantly enhanced. *(i)* By doing so the charge emission of the electron traps can be accelerated, which enables to optimize the model parameters, and *(ii)* hole traps can become charged during the accumulation pulse and thus can contribute to the measured recovery behavior. In [18] experimental data has been recorded employing pulse MSM sequences, and the difference to the classical MSM case where the $\Delta V_{th}$ is shifted towards negative values has been explained by contributions of additional hole traps which are located close to the valence band of SiC.

## IV. Possible Defect Candidates for SiC Devices

As previously mentioned, the defects can be roughly classified into *(i)* interface defects, *(ii)* oxide defects and *(iii)* bulk defects. In contrast to Si substrates where interface of the thermally grown $SiO_2$ can be passivated with $H_2$-POA nearly perfectly, an oxide grown on SiC exhibits a large number of defect-states within the energy gap. Also, the presence of a second atomic species, C, implies additional chemical complexity and might support the formation of additional defects in the adjacent $SiO_2$ layer [37]. Furthermore the higher band-gap of SiC compared to Si enables more near-interfacial defects to become electrically active, see Table I. Furthermore, as the oxidation process of SiC depends on the crystal surface orientation [47, 48] and thermal oxidation creates C-residues chemical vapor deposition (CVD) from TEOS [49] is commonly used for the fabrication of the gate insulators. The quality of the interface strongly depends on the surface termination as well as on the temperature used for POA. As possible defect candidates for interface states the silicon vacany $V_{Si}$ and carbon dangling bonds $P_{bC}$, have been recently proposed [40]. Their CTLs have been calculated by density function theory (DFT) simulations and are found to lie within the relevant AER for charge trapping in SiC transistors, see Figure 6. Both defects exhibit CTLs withing the AER of typical MSM sequences and thus can contribute to the measurement signal.

Next to the interface states of the $SiO_2$/SiC system, defects in the SiC substrate like the silicon vacancy $V_{Si}$ and carbon vacancy $V_C$ are also potential traping sites and can seriously hamper device performance and affect transistor lifetime. Both kinds of defects exhibit a variety of different configurations.

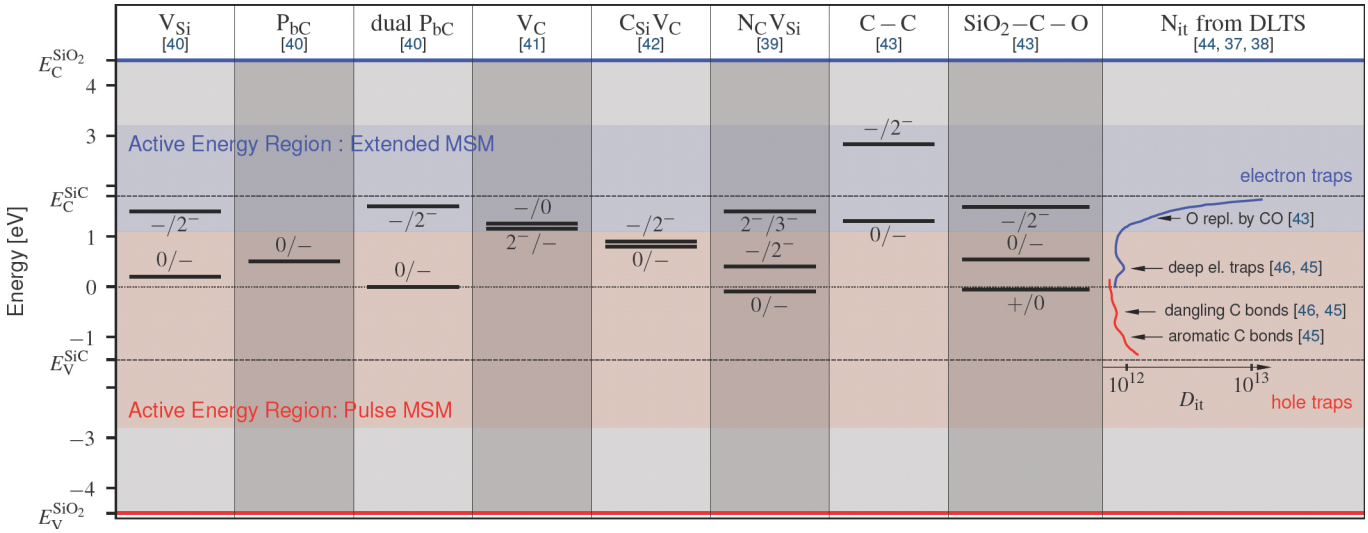



**Fig. 6:** Various different defect structures for potential defect candidates being present in SiC MOS transistors have been proposed in the literature. Some of the proposed defect candidates can be ruled out as they exhibit formation energies being way too high to be relevant for the material system. Next to interface states and oxide defects extracted from DFT calculations DLTS measurements have been performed and from this a distribution of interface states has been proposed.

The most favorable states are $V_{Si}{}^{-1}$ and $V_C{}^{+1}$ and their CTLs are summarized in Figure 6. As can be seen, both kinds of defects show CTLs within the AER of the SiC nMOSFET. Quite interestingly, while the silicon vacancy as bulk defect has been extensively investigated, the $V_{Si}{}^{-1}$ at the interface has been studied only recently by analysis of electrically detectable magnetic resonance (EDMR) spectra with *ab-inito* calculations [50, 51, 52, 40]. Another class of defects are antisite-vacancies where in an AB compound an atom of type A can diffuse away to become replaced by an atom of type B, thereby forming an antisite and a vacancy, which is for instance the case for the $C_{Si}V_C$ center [42]. The corresponding CTLs of such a defect estimated by *ab-initio* calculations of the respective defect structure are shown in Figure 6.

As nitrogen is used for n-doping, nitrogen related defects are very likely present in the SiC substrate, and have been the subject of recent DFT calculations based on measurements performed using the spin dependent recombination (SDR) technique [53, 39]. Among the studied nitrogen vacancy centers, namely the $N_CV_{Si}$, the $N_{Si}V_C$, and $N_CC_{Si}$ configurations, only the $N_CV_{Si}$ is expected to be visible in the SDR spectra. As can be seen in Figure 6, *ab-initio* calculations of the $N_CV_{Si}$ defect revealed relevant CTL for this particular structure within the bandgap of SiC [39].

A large variety of defects prevalent in SiC transistors exists which can seriously affect the device performance and operation stability. It is very difficult, not to say almost impossible, to rule out a single defect being responsible for altering of the device characteristics. However, a consistency between defect parameters extracted from ab-initio simulations, physical device simulations and experiments is essential to validate the models and methods. Furthermore, to estimate the device lifetime for various operation conditions an accurate description of the charge trapping in SiC MOS devices is inevitable.

## V. Conclusions

The performance of SiC MOS transistors is seriously affected by charge trapping of defects during device operation under nominal operating conditions. As a consequence, the threshold voltage of the MOS devices can change over time. This effect is more pronounced in SiC devices compared to Si technology due increased trap densities. In order to identify the origin of charge trapping and to provide a physics based explanation for this phenomenon the two-state defect model is employed. Using this model the complex temperature dependence of the $I_D(V_G)$ characteristics of SiC devices can be explained. Furthermore, extensive MSM experiments are performed, where the drift of the current during the recovery phases is recorded. Afterwards the temporal evolution of the current has been successfully modeled using our reliability simulator Comphy. By introducing an accumulation pulse in the MSM sequence, charge trapping of hole traps close to the valence band starts to affect the device behavior. Finally, a physics based description for the observed charge trapping behavior relying on two identified electron trap bands, and one hole trap band is given. With the calibrated model in hand one can extract the device lifetime under various operating conditions way more accurate and than with empirical formulations.

## VI. Acknowledgement

Stimulating discussions with C. Schleich, D. Waldhoer, B. Stampfer, M. Kampl, T. Grasser (TU Wien), G. Rzepa (Global TCAD Solutions), G. Pobegen (KAI), T. Aichinger, G. Rescher, P. Ellinghaus, R. Elpelt (Infineon) and S. Tyaginov (imec) are greatfully acknowledged.

## REFERENCES


[1] J. Casady and R. Johnson. "Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review". In: *Solid-State Electron.* 39.10 (1996), pp. 1409–1422. DOI: 10.1016/0038-1101(96)00045-7.

[2] W. Choyke, H. Matsunami, and G. Pensl. *Silicon Carbide: Recent Major Advances*. Springer, 2004.

[3] S. Wang, D. Ang, and G. Du. "Effect of Nitrogen on the Frequency Dependence of Dynamic NBTI-Induced Threshold-Voltage Shift of the Ultrathin Oxynitride Gate P-MOSFET". In: *IEEE Electron Device Lett.* 29.5 (2008), pp. 483–486. DOI: 10.1109/LED.2008.919793.

[4] S. Sridevan and B. Jayant Baliga. "Lateral n-channel inversion mode 4H-SiC MOSFETs". In: *IEEE Electron Device Lett.* 19.7 (1998), pp. 228–230. DOI: 10.1109/55.701425.

[5] S. Sridevan and B. Jayant Baliga. *Inversion layer mobility in SiC MOSFETs*. 1998.

[6] D. J. Lichtenwalner, L. Cheng, S. Allen, J. W. Palmour, A. Lelis, and C. Scozzie. "Comparison of channel mobility and oxide properties of MOSFET devices on Si-face (0001) and A-face (11-20) 4H-SiC". In: *MRS Proceedings* 1693 (2014). DOI: 10.1557/opl.2014.530.

[7] T. Kimoto and J. A. Cooper. *Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications*. John Wiley & Sons, 2014.

[8] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, M. Di Ventra, S. T. Pantelides, L. C. Feldman, and R. A. Weller. "Effect of nitric oxide annealing on the interface trap densities near the band edges in the 4H polytype of silicon carbide". In: *Appl.Phys.Lett.* 76.13 (2000), pp. 1713–1715. DOI: 10.1063/1.126167.

[9] P. Jamet and S. Dimitrijev. "Physical properties of N2O and NO-nitrided gate oxides grown on 4H SiC". In: *Appl.Phys.Lett.* 79.3 (2001), pp. 323–325. DOI: 10.1063/1.1385181.

[10] H.-f. Li, S. Dimitrijev, H. B. Harrison, and D. Sweatman. "Interfacial characteristics of N2O and NO nitrided $SiO_2$ grown on SiC by rapid thermal processing". In: *Appl.Phys.Lett.* 70.15 (1997), pp. 2028–2030. DOI: 10.1063/1.118773.

[11] V. V. Afanas'ev, A. Stesmans, F. Ciobanu, G. Pensl, K. Y. Cheong, and S. Dimitrijev. "Mechanisms responsible for improvement of 4H-$SiC/SiO_2$ interface properties by nitridation". In: *Appl.Phys.Lett.* 82.4 (2003), pp. 568–570. DOI: 10.1063/1.1532103.

[12] J. Rozen, S. Dhar, S. T. Pantelides, L. C. Feldman, S. Wang, J. R. Williams, and V. V. Afanas'ev. "Suppression of interface state generation upon electron injection in nitrided oxides grown on 4H-SiC". In: *Appl.Phys.Lett.* 91.15 (2007), p. 153503. DOI: 10.1063/1.2790374.

[13] J. Rozen, S. Dhar, M. E. Zvanut, J. R. Williams, and L. C. Feldman. "Density of interface states, electron traps, and hole traps as a function of the nitrogen density in $SiO_2$ on SiC". In: *J.Appl.Phys.* 105.12 (2009), p. 124506. DOI: 10.1063/1.3131845.

[14] E. Pippel, J. Woltersdorf, H. Ö. Olafsson, and E. Ö. Sveinbjörnsson. "Interfaces between 4H-SiC and SiO2: Microstructure, nanochemistry, and near-interface traps". In: *J.Appl.Phys.* 97.3 (2005), p. 034302. DOI: 10.1063/1.1836004.

[15] J. Berens, G. Pobegen, G. Rescher, T. Aichinger, and T. Grasser. "$NH_3$ and NO + $NH_3$ Annealing of 4H-SiC Trench MOSFETs: Device Performance and Reliability". In: *IEEE Trans. Electron Devices* 66.11 (2019), pp. 4692–4697. DOI: 10.1109/TED.2019.2941723.

[16] J. Berens, F. Rasinger, T. Aichinger, M. Heuken, M. Krieger, and G. Pobegen. "Detection and Cryogenic Characterization of Defects at the SiO2/4H-SiC Interface in Trench MOSFET". In: *IEEE Trans. Electron Devices* 66.3 (2019), pp. 1213–1217. DOI: 10.1109/TED.2019.2891820.

[17] G. Rescher, G. Pobegen, T. Aichinger, and T. Grasser. "On the sub-threshold drain current sweep hysteresis of 4H-SiC nMOSFETs". In: *Proc. Intl. Electron Devices Meeting (IEDM)*. 2016, pp. 10.8.1–10.8.4. DOI: 10.1109/IEDM.2016.7838392.

[18] C. Schleich, J. Berens, G. Rzepa, G. Pobegen, G. Rescher, S. E. Tyaginov, T. Grasser, and M. Waltl. "Physical Modeling of Bias Temperature Instabilities in SiC MOSFETs". In: *Proc. Intl. Electron Devices Meeting (IEDM)*. 2019.

[19] T. Aichinger, G. Rescher, and G. Pobegen. "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs". In: *Microelectronics Reliability* 80 (2018), pp. 68–78. DOI: 10.1016/j.microrel.2017.11.020.

[20] K. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin, and H. Reisinger. "Review on SiC MOSFETs High-Voltage Device Reliability Focusing on Threshold Voltage Instability". In: *IEEE Trans. Electron Devices* 66.11 (2019), pp. 4604–4616. DOI: 10.1109/TED.2019.2938262.

[21] M. Waltl, G. Rzepa, A. Grill, W. Gös, J. Franco, B. Kaczer, L. Witters, J. Mitard, N. Horiguchi, and T. Grasser. "Superior NBTI in High-k SiGe Transistors - Part I: Experimental". In: *IEEE Trans. Electron Devices* 64.5 (2017), pp. 2092–2098. DOI: 10.1109/TED.2017.2686086.

[22] T. Grasser. "Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities". In: *Microelectronics Reliability* 52.1 (2012), pp. 39–70. DOI: 10.1016/j.microrel.2011.09.002.

[23] G. Rzepa, J. Franco, B. J. O'Sullivan, A. Subirats, M. Simicic, G. Hellings, P. Weckx, M. Jech, T. Knobloch, M. Waltl, P. J. Roussel, D. Linten, B. Kaczer, and T. Grasser. "Comphy – A Compact-Physics Framework for Unified Modeling of BTI". In: *Microelectronics Reliability* 85.1 (2018), pp. 49–65. DOI: 10.1016/j.microrel.2018.04.002.

[24] T. Tewksbury. "Relaxation Effects in MOS Devices due to Tunnel Exchange with Near-Interface Oxide Traps". Ph.D. Thesis. MIT, 1992.

[25] T. Grasser, B. Kaczer, W. Goes, T. Aichinger, P. Hehenberger, and M. Nelhiebel. "A two-stage model for negative bias temperature instability". In: *Proc. Intl. Rel. Phys. Symp. (IRPS)*. 2009, pp. 33–44. DOI: 10.1109/IRPS.2009.5173221.

[26] J. P. Campbell, P. M. Lenahan, C. J. Cochrane, A. T. Krishnan, and S. Krishnan. "Atomic-scale defects involved in the negative-bias temperature instability". In: *IEEE Trans.Dev.Mat.Rel.* 7.4 (2007), pp. 540–557. DOI: 10.1109/TDMR.2007.911379.

[27] W. Goes. "Hole Trapping andthe Negative Bias Temperature Instability". Ph.D. Thesis. TU Wien, 1992.

[28] T. Grasser, H. Reisinger, P. J. Wagner, F. Schanovsky, W. Goes, and B. Kaczer. "The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability". In: *Proc. Intl. Rel. Phys. Symp. (IRPS)*. 2010, pp. 16–25. DOI: 10.1109/IRPS.2010.5488859.

[29] D. B. Habersat, A. J. Lelis, and R. Green. "Measurement considerations for evaluating BTI effects in SiC MOSFETs". In: *Microelectronics Reliability* 81 (2018), pp. 121–126. DOI: 10.1016/j.microrel.2017.12.015.

[30] D. B. Habersat, A. J. Lelis, and R. Green. "Influences of Bias Interruption and Reapplication on High-Temperature Threshold-Voltage Shifts of SiC DMOSFETs". In: *Material Science Forum*. Vol. 924. July 2018, pp. 743–747. DOI: 10.4028/www.scientific.net/MSF.924.743.

[31] A. J. Lelis, D. Habersat, R. Green, A. Ogunniyi, M. Gurfinkel, J. Suehle, and N. Goldsman. "Time Dependence of Bias-Stress-Induced SiC MOSFET Threshold-Voltage Instability Measurements". In: *IEEE Trans. Electron Devices* 55.8 (2008), pp. 1835–1840. DOI: 10.1109/TED.2008.926672.

[32] R. Green, A. Lelis, and D. Habersat. "Threshold-voltage bias-temperature instability in commercially-available SiC MOSFETs". In: *Jap.J.Appl.Phys.* 55.4S (2016). DOI: 10.7567/jjap.55.04ea03.

[33] D. Peters, T. Aichinger, T. Basler, G. Rescher, K. Puschkarsky, and H. Reisinger. "Investigation of threshold voltage stability of SiC MOSFETs". In: *Intl. Symp. on Pwr. Semic. Dev. and ICs (ISPSD)*. 2018, pp. 40–43. DOI: 10.1109/ISPSD.2018.8393597.

[34] B. Kaczer, T. Grasser, J. Roussel, J. Martin-Martinez, R. O'Connor, B. J. O'Sullivan, and G. Groeseneken. "Ubiquitous relaxation in BTI stressing - New evaluation and insights". In: *Proc. Intl. Rel. Phys. Symp. (IRPS)*. 2008, pp. 20–27. DOI: 10.1109/RELPHY.2008.4558858.

[35] M. Hasanuzzaman, S. K. Islam, L. M. Tolbert, and M. T. Alam. "Temperature dependency of MOSFET device characteristics in 4H- and 6H-silicon carbide (SiC)". In: *Solid-State Electron.* 48.10 (2004), pp. 1877–1881. DOI: 10.1016/j.sse.2004.05.029.

[36] S. Potbhare, N. Goldsman, A. Lelis, J. M. McGarrity, F. B. McLean, and D. Habersat. "A Physical Model of High Temperature 4H-SiC

MOSFETs". In: *IEEE Trans. Electron Devices* 55.8 (2008), pp. 2029–2040. DOI: 10.1109/TED.2008.926665.

[37] V. V. Afanas'ev, M. Bassler, G. Pensl, and M. Schulz. "Intrinsic $SiC/SiO_2$ Interface States". In: *Phys. Status Solidi (a)* 162.1 (1997), pp. 321–337. DOI: 10.1002/1521-396X(199707)162:1<321::AID-PSSA321>3.0.CO;2-F.

[38] S. E. Tyaginov, M. Jech, G. Rzepa, A. Grill, A.-M. El-Sayed, G. Pobegen, A. Makarov, and T. Grasser. "Border Trap Based Modeling of SiC Transistor Transfer Characteristics". In: *Proc. Intl. Integrated Reliability Workshop (IIRW)*. 2018. DOI: 10.1109/IIRW.2018.8727083.

[39] J. Cottom, G. Gruber, P. Hadley, M. Koch, G. Pobegen, T. Aichinger, and A. Shluger. "Recombination centers in 4H-SiC investigated by electrically detected magnetic resonance and ab initio modeling". In: *J.Appl.Phys.* 119.18 (2016), p. 181507. DOI: 10.1063/1.4948242.

[40] J. Cottom, G. Gruber, G. Pobegen, T. Aichinger, and A. L. Shluger. "Recombination defects at the 4H-$SiC/SiO_2$ interface investigated with electrically detected magnetic resonance and ab initio calculations". In: *J.Appl.Phys.* 124.4 (2018), p. 045302. DOI: 10.1063/1.5024608.

[41] I. Capan, T. Brodar, Z. Pastuovic, R. Siegele, T. Ohshima, S.-i. Sato, T. Makino, L. Snoj, V. Radulovic, J. Coutinho, V. J. B. Torres, and K. Demmouche. "Double negatively charged carbon vacancy at the h- and k-sites in 4H-SiC: Combined Laplace-DLTS and DFT study". In: *J.Appl.Phys.* 123.16 (2018), p. 161597. DOI: 10.1063/1.5011124.

[42] T. Umeda, N. T. Son, J. Isoya, E. Janzén, T. Ohshima, N. Morishita, H. Itoh, A. Gali, and M. Bockstedte. "Identification of the Carbon Antisite-Vacancy Pair in 4*H*-SiC". In: *Physical Review Letters* 96 (14 2006), p. 145501. DOI: 10.1103/PhysRevLett.96.145501.

[43] F. Devynck, A. Alkauskas, P. Broqvist, and A. Pasquarello. "Charge transition levels of carbon-, oxygen-, and hydrogen-related defects at the $SiC/SiO_2$ interface through hybrid functionals". In: *Physical Review B* 84 (23 2011), p. 235320. DOI: 10.1103/PhysRevB.84.235320.

[44] P. Deák, J. Knaup, C. Thill, T. Frauenheim, T. Hornos, and A. Gali. "The mechanism of defect creation and passivation at the $SiC/SiO_2$ interface". In: *J.Phys.D: Appl.Phys* 41.4 (2008), pp. 049801–049801. DOI: 10.1088/0022-3727/41/4/049801.

[45] J. M. Knaup, P. Deák, T. Frauenheim, A. Gali, Z. Hajnal, and W. J. Choyke. "Defects in $SiO_2$ as the possible origin of near interface traps in the $SiC/SiO_2$ system: A systematic theoretical study". In: *Physical Review B* 72 (11 2005), p. 115323. DOI: 10.1103/PhysRevB.72.115323.

[46] A. Gali, P. Deák, E. Rauls, N. T. Son, I. G. Ivanov, F. H. C. Carlsson, E. Janzén, and W. J. Choyke. "Correlation between the antisite pair and the $D_I$ center in SiC". In: *Physical Review B* 67 (15 2003), p. 155203. DOI: 10.1103/PhysRevB.67.155203.

[47] K. Christiansen and R. Helbig. "Anisotropic oxidation of 6H-SiC". In: *J.Appl.Phys.* 79.6 (1996), pp. 3276–3281. DOI: 10.1063/1.361225.

[48] E. A. Ray, J. Rozen, S. Dhar, L. C. Feldman, and J. R. Williams. "Pressure dependence of $SiO_2$ growth kinetics and electrical properties in SiC". In: *J.Appl.Phys.* 103.2 (2008), p. 023522. DOI: 10.1063/1.2832408.

[49] J. E. Crowell, L. L. Tedder, H.-C. Cho, F. M. Cascarano, and M. A. Logan. "The chemical vapor deposition of $SiO_2$ from TEOS". In: *J. of Elec. Spec. and Rel. Phen.* 54-55 (1990), pp. 1097–1104. DOI: 10.1016/0368-2048(90)80299-P.

[50] C. J. Cochrane, P. M. Lenahan, and A. J. Lelis. "An electrically detected magnetic resonance study of performance limiting defects in SiC metal oxide semiconductor field effect transistors". In: *J.Appl.Phys.* 109.1 (2011), p. 014506. DOI: 10.1063/1.3530600.

[51] C. J. Cochrane, P. M. Lenahan, and A. J. Lelis. "Identification of a silicon vacancy as an important defect in 4H SiC metal oxide semiconducting field effect transistor using spin dependent recombination". In: *Appl.Phys.Lett.* 100.2 (2012), p. 023509. DOI: 10.1063/1.3675857.

[52] C. J. Cochrane, P. M. Lenahan, and A. J. Lelis. "The effect of nitric oxide anneals on silicon vacancies at and very near the interface of 4H SiC metal oxide semiconducting field effect transistors using electrically detected magnetic resonance". In: *Appl.Phys.Lett.* 102.19 (2013), p. 193507. DOI: 10.1063/1.4805355.

[53] U. Forsberg, Ö. Danielsson, A. Henry, M. Linnarsson, and E. Janzen. "Nitrogen doping of epitaxial silicon carbide". In: *Journal of Crystal Growth* 236.1 (2002), pp. 101–112. DOI: 10.1016/S0022-0248(01)02198-4.