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Soft error hardening enhancement analysis of NBTI tolerant Schmitt trigger circuit

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ABSTRACT

Bias temperature instability (BTI) and soft errors are major reliability concerns for deep submicron technologies. Negative BTI leads to an increase of the threshold voltage of PMOS transistors and is thus considered a serious challenge for improving circuit performance. In this paper, we concentrate on a design-time solution, i.e., more reliable NMOS only Schmitt Trigger with Voltage Booster (NST-VB). For this we analyzed the impact of BTI on the soft-error susceptibility of different CMOS circuits using HSPICE and performed critical charge simulations considering different supply voltages and stress time. From our results, we conclude that the NST-VB circuit has a higher critical charge when compared to CMOS inverters and Schmitt trigger (ST) based counterparts. NST-VB has improved the sensitivity of 62.48% and 55.10%, as compared to CMOS inverter and ST circuits, respectively, after three years of operation. To better assess soft error resilience, we introduce a soft error rate ratio (SERR) as a performance metric. Our analysis indicates that NST-VB has 12.62%, and 12.39% less SERR compared to ST and CMOS inverters. The effect of process variation on CMOS inverter, ST inverter and NST-VB circuit are analyzed using 5000 Monte Carlo simulations for critical voltages and we observe that the deviation of NST-VB is 6.06× and 6.89× less as compared to the CMOS and ST based inverters, respectively.

1. Introduction

Bias temperature instability (BTI) is one of the most significant reliability issues for new generations of CMOS devices [1]. This device performance degradation mechanism can be classified into negative BTI (NBTI) and positive BTI (PBTI) which affect PMOS and NMOS transistors, respectively. The impact of NBTI in PMOS transistors and PBTI in NMOS transistors is more severe than the NBTI/NMOS and PBTI/PMOS cases and seriously affect the lifetime of single devices and complex circuits [2,3]. As NBTI in PMOS transistors has been observed to be more pronounced than PBTI in NMOS transistors, the former is typically studied [3]. The origin of NBTI and PBTI is due to single defects in the oxide or at the semiconductor interface, which can get charged under normal operating conditions [4,5]. The degradation can become accelerated and more pronounce at raised temperatures [6,7]. The trapped charges in both kinds of devices may increase the transistors' threshold voltage (V_{th}) and degrade the device transconductance and mobility [8]. As a result, NBTI and PBTI cause a degradation of device performance over time [9], which may lead to timing errors, Jitter and reduced noise margins in logic and memories [10].

Along with susceptibility to BTI, aggressive scaled down CMOS devices are increasingly sensitive to radiation-induced errors which also degrade the noise immunity of the circuit [11,12]. For instance, radiation-induced single event effects (SEE) are mainly due to reduced supply voltages and node capacitances [13,14]. Single event upset (SEU) is the typical SEE in storage elements (latches and memory cells) which can lead to a flip of the circuits' logic states. However, a single event transient (SET) is induced in the combinational circuits which may produce voltage glitch that may propagate through the logic blocks and give rise for soft errors [15]. Alpha particles and neutron radiation from cosmic rays can lead to soft errors and affect the circuit performance in the terrestrial and space environment [16,17]. In particular, in recent CMOS technology, it has been proven that alpha particles generation induced by neutron hits significantly contribute to the

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overall soft error rate [18]. Moreover, direct ionization from secondary protons can affect circuits operating at low voltages which exhibit a reduced critical charge (Q_{crit}) [18,19]. The decrease of the critical charge with supply voltage reduction has been studied in detail in [20]. The critical charge is the minimum amount of collected charge at the sensitive node of a circuit during a particle strike which is sufficient to lead to the same input and output state of the circuit [11]. On top of that, NBTI increases the soft error rate (SER), since it causes a reduction of Q_{crit} with the stress time [21]. As a result, for deep submicron technologies, the SER is expected to be significantly increased [22].

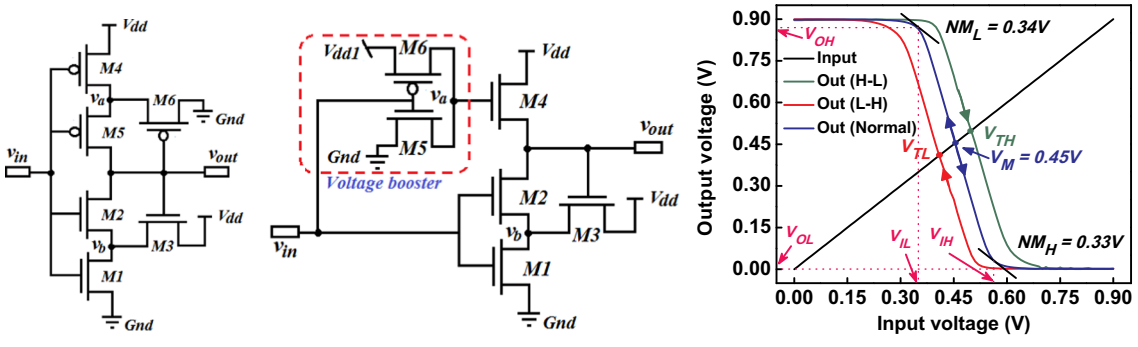
NBTI stress is an aggravating factor for conventional CMOS inverter susceptibility to latch-up during slow high-low (H-L) and low-high (L-H) transitions [23]. The straightforward solution to overcome NBTI induced latch-up is the utilization of NMOS inverters [23], but this approach has many drawbacks, including (i) reduced output voltage ($V_{dd} - V_{thn}$), (ii) small noise margins, and (iii) the direct current path issue when the Pull-Down Network (PDN) is ON, since the Pull-Up Network (PUN) is always ON. Moreover, the threshold voltage of transistors has not scaled as much as the supply voltage in deep submicron technologies, which results in a decreased static noise margin of digital circuits. Therefore, the input signal itself is more vulnerable for the external radiation and noise has become an essential issue for IC designers [24,25]. An alternative solution to tackle slowly varying input signals and enhance the noise margin relies on the use of Schmitt trigger (ST) circuits [26–28]. The switching threshold voltage of the ST depends on the direction of the input signal transition which is given by the hysteresis of the transfer characteristics. Therefore, since the output of the ST does not respond directly to the input when its variation is lower than the switching threshold difference, the noise immunity of the ST circuit increases considerably compared with standard CMOS designs. A ST based SRAM design has been proposed in [29], where the authors highlight its suitability to operate correctly at ultra-low supply voltage considering process variations. Moreover, the effectiveness of ST under PVT variations is discussed in [30], where benefits and drawbacks of ST inverters are addressed in detail.

Besides improving the noise margin and being robust against process variations, ST-based circuits can be effectively used to enhance soft error resilience, as proven by a significant amount of research that has been recently carried out. For example, the hysteresis property of ST is utilized to mask the soft error transient pulses in the circuits [31], whereas, in [13] authors propose a hardened memory cell uses ST design for single-event hardening with the multiple-node upset. Finally, in [32], ST inverter chains are analyzed under subthreshold conditions, proving that ST circuits offer improved soft error hardening and hence better tolerance to single event effects compared to traditional designs. Although previous research results in [25,28,29] have demonstrated that ST-based designs can be very useful for improving noise margin and tackling soft error issues, the impact of NBTI on the ST circuit operation has not been addressed so far. Recently, in [33,34], authors have demonstrated that ST is more sensitive to NBTI than the CMOS inverter, which is mainly due to the use of three PMOS transistors instead of only one for CMOS inverter. To tackle this drawback, they have proposed a more effective circuit to counteract NBTI detrimental effects, namely the NMOS only ST with Voltage Booster (NST-VB). Its rail-to-rail path makes use of only NMOS transistors, which can substantially reduces the impact of NBTI effect on the circuit characteristics. NST-VB exhibits an improved noise margin due to the feedback connections, and is more robust output due to the voltage booster circuit. In [34], the basic concept of the NST-VB circuit was introduced, but its capability to soft error hardening enhancement analysis when BTI aging is accounted for has not been evaluated. Hereafter, conventional CMOS inverter, ST based inverter, and NST-VB based inverter are referred to as CMOS, ST and NST-VB, respectively.

The main goal of this work is to assess NST-VB reliability implications when the soft error radiation hardening enhancement is considered. To this end, we first compare the susceptibility to soft errors with functionally equivalent counterparts, i.e., CMOS inverter and ST, concerning critical charge variations when exposed to different stress time and supply voltages. Particularly, we compute and compare the critical charge sensitivity for all the considered circuits and then conduct a critical charge degradation analysis under various stress and supply voltage values. Our findings indicate that, after three years of stress time, the NST-VB circuit exhibits 62.48% and 55.10% improved sensitivity as compared to CMOS inverter and ST counterparts, respectively. Subsequently, the viability of radiation hardening enhancement of different circuits is measured using soft error rate ratio (SERR). Our evaluations indicate that the NST-VB has 12.62% and 12.39% less SERR when compared to ST, and CMOS based inverters. While soft error susceptibility is the key metric for our analysis to get a better perspective on NST-VB implications, we evaluated the high energy particles dose to flipping margins and found that the NST-VB circuit is more tolerant to high energy than the CMOS inverter. We also analyzed the Monte Carlo simulations on critical input nodes and output voltages of CMOS, ST, and NST-VB circuits and our results demonstrate that the NST-VB is less affected by process variations.

2. NMOS only voltage booster enhanced Schmitt trigger circuit

The schematic for the NST-VB and its VTC are shown in Fig. 1(b) and (c) [33,34]. The main attribute of this circuit is the use of only NMOS transistors in the critical path. This can be achieved by replacing the PMOS transistor from PUN with an NMOS transistor counterpart to obliterate the NBTI induced side effects. The NST-VB circuit has been derived combining an ST and an NMOS inverter. The NMOS inverter is NBTI insensitive but has many issues like small noise margins, reduced maximum output voltage ($V_{dd} - V_{thn}$) and direct current from V_{dd} to ground. The direct current exists in the circuit when PDN is ON since PUN is always ON. The voltage booster in Fig. 1(b) is implemented to



(a) (b) (c)

Fig. 1. Schematic of (a) Schmitt trigger circuit and the (b) NST-VB circuit is shown together with the (c) Voltage transfer characteristics of NST-VB circuit.

address the weaknesses of the NMOS inverter, i.e., to overcome the direct current problem and to increase the output voltage swing, with the trade-off of slightly higher leakage power dissipation. The supply voltage of voltage booster is chosen to be about V_{thn} higher than the primary circuit, i.e. $V_{dd1} = V_{dd} + V_{thn}$. Similarly, the ST improves the noise margin of the circuit, but suffers from NBTI due to three PMOS transistors present in its PUN. To overcome the mentioned issues, the NMOS inverter PUN with a voltage booster and a ST PDN with feedback connection have been added into the NST-VB design. The circuit output is forced into high impedance by enabling the voltage booster, and the noise margin is increased with feedback connected transistors in PDN by adjusting the higher and lower threshold voltages (V_{TH} and V_{TL}) of the circuit.

For the direction of the output transition, transistor M_3 is combined with transistor M_2 and is used to adjust the device transconductance ratio k_R. The V_{TH} and V_{TL} determines the voltage transfer characteristics of the NST-VB circuit as illustrated in Fig. 1(c). In this work we have used the NST-VB circuit as an inverter which follows the same characteristics during H-L and L-H transitions. For this, the transistor sizings are adjusted to get $V_{TH} = V_{TL} = V_M = \frac{V_{dd}}{2}$, as shown in Fig. 1(c). As our purpose is to evaluate the NST-VB structure with respect to radiation hardening enhancement, we discuss theoretical aspects related to critical charge, simulation setup, and simulation flow for soft-error analysis with embedded aging effects.

3. Radiation hardening analysis methodology

As previously mentioned, the presence of hysteresis in the circuit improves the noise margins, and thus the voltage noise at a gate input needs to be higher in order to be propagated to the output. This is reflected by a higher critical charge at the input of the gate, and higher soft error robustness. In order to highlight the effect of NBTI on the critical charge we reduced the hysteresis to zero for the worst case soft error analysis of the circuits with hysteresis. To assess the effectiveness of the NST-VB circuit as an inverter with improved robustness against soft errors compared to standard CMOS inverter and ST based inverters when considering NBTI, we consider the PTM 32 nm CMOS technology [35]. For stress analysis and aging evaluation, we use the HSPICE MOSRA model [36] and performed all simulations considering supply voltage $V_{dd} = 0.9$ V for the circuit and $V_{dd1} = 1.4$ V for voltage booster supply voltage. The operating temperature of the circuit is set to $T = 125$ ° C to increase and accelerate aging effects.

3.1. Simulation setup

The radiation hardening investigation of the three above circuits (CMOS inverter, ST, and NST-VB), is carried out using HSPICE. Fig. 2 summarizes the various steps involved in the critical charge analysis at several stress time for different inverter circuits. All simulations are performed considering the simulation setup defined in Fig. 3. Three cascaded inverters are used and the effect on the circuit under test (CUT) is analyzed by applying logic low to the input of the first inverter. The cascade of three inverter with CUT in centre allows us to account for the loading effect on the CUT, thus leading to more accurate results than a single inverter. The critical charge at a node is affected more by the driving strength of the gate driving the node, rather than on the node capacitance. Therefore, to determine the accurate critical charge, a driver circuit is required [37], which is the first inverter in Fig. 3. The stronger the driver is the higher the critical charge becomes. Similarly, the output inverter is connected to the CUT to measure capability of the CUT to drive subsequent circuits. The driving capability of the CUT is used to find the fanout of the CUT. A single event transient (SET) is injected at the output of the first inverter and then the propagation of the SET to the output of the second inverter is analyzed. The cascade structure is used in the soft error analysis to observe the effect of high energy particle induced glitches at the sensitive node, and to analyze its

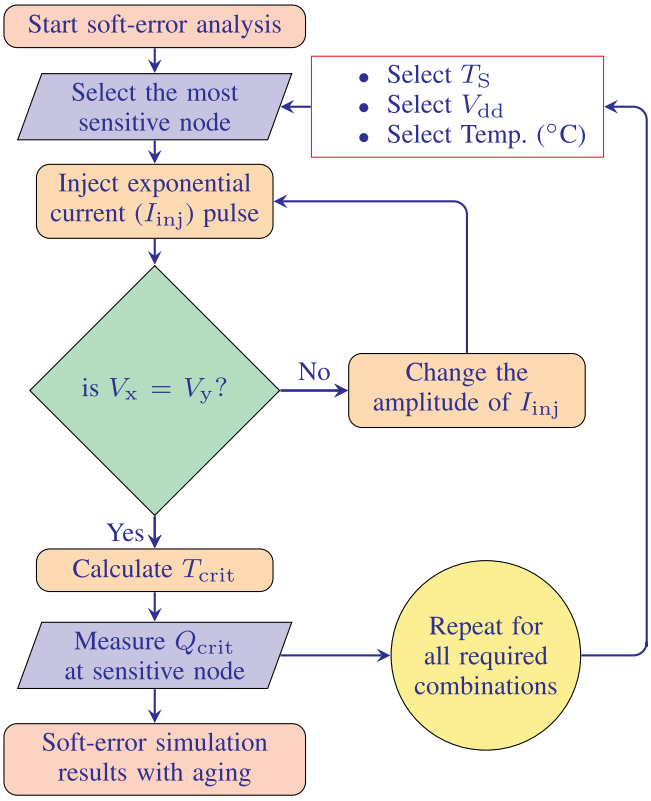


Fig. 2. Simulation flow of soft-error analysis with embedded aging effects.

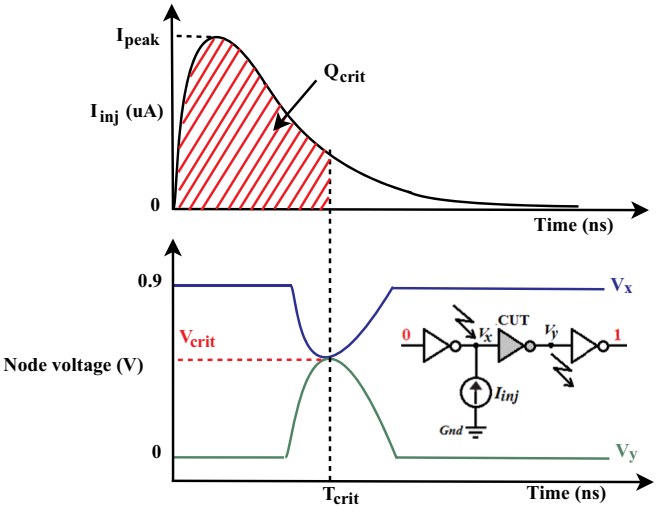


Fig. 3. Graphical representation defining the critical charge. V_x and V_y are the voltages of the input and output nodes of the circuit under test (CUT). The simulation setup for a high energy particle hitting a sensitive node V_x storing 1 of a inverter chain is given in inset.

effect on the output logic of the successive inverter. If the amplitude and duration of the induced glitches are high enough to change the logic of successive inverter, we consider that the energetic particle hit can give rise to a soft error. Therefore, the soft error rate is chosen as a metric to analyze the radiation hardening of the considered circuit for particular operating conditions. A double exponential current pulse is applied to the most sensitive input node of CUT and to extract V_{crit} where V_x and V_y are the same. Subsequently, T_{crit} is extracted as the temperature at which $V_x = V_y$, and the critical charge is calculated using Eq. (3). A detailed graphical illustration for critical charge

calculation is depicted in Fig. 3. The above evaluation is repeated for different stress times at various supply voltages for all inverter circuits.

In order to introduce SEU into the circuits, the current induced by α-particles which hit the CMOS circuit is modeled by a double exponential current source and is specified by [38]

$$I_{inj}(t) = \frac{Q_{inj}}{\tau_f - \tau_r} \times \left(e^{-t/\tau_f} - e^{-t/\tau_r} \right) \quad (1)$$

or

$$I_{inj}(t) = I_{peak} \times (e^{-t/\tau_f} - e^{-t/\tau_r}) \quad (2)$$

where Q_{inj} is the aggregate sum of the charge kept at the sensitive node and I_{peak} is the peak value of the current source. Also, τ_f and τ_r are material dependent time constants. As suggested in [39] typical values are 1 ps and 50 ps for τ_r and τ_f, respectively, and are used for the simulations.

In our experiments, the Q_{crit} is determined by introducing a current pulse at the respective sensitive node of the inverter circuits. This pulse simulates the current induced by the particle strike at the sensitive node. To calculate Q_{crit}, we determine the minimum duration and magnitude of the injected current pulse that is required to lead to $V_x = V_y$. Afterwards Q_{crit} is calculated by integrating the current pulse for the time interval 0 to T_{crit}

$$Q_{crit} = \int_0^{T_{crit}} I_{inj}(t)dt \quad (3)$$

where $I_{inj}(t)$ is the injected current pulse at sensitive nodes for the analysis of SEU.

3.2. Single event transients in the circuits

Single even transients can occur only at sensitive nodes. A sensitive node is basically a pn-junction that is reverse biased. This condition typically occurs in drain junctions of transistors that are in the OFF state. In fact, in this case, the electric field across the junction, which is determined by the voltage drop across the junction is V_{dd}, is at its maximum value.

If we consider a standard CMOS inverter, the following two situations can occur. First, when the input is logic 0, and the output is logic 1, the NMOS transistor is in its OFF state, and its drain junction is then the sensitive one. An energetic particle hitting this region can induce enough charge to cause a negative glitch, i.e. a temporary 1 → 0 transition, at the inverter output. Second, when the input is logic 1, and the output is logic 0, the PMOS transistor is in its OFF state, and its drain junction is the sensitive one. An energetic particle hitting this region can cause a positive glitch, i.e. a temporary 0 → 1 transition, at the inverter output. Similar considerations apply to transistors *M2* and *M5* in the circuit for a standard ST as shown in Fig. 1(a).

If we consider the circuit from Fig. 1(b), the situation is different. Indeed, only NMOS transistors drive the output of the NST-VB circuit. Therefore, the only critical condition that we need to consider is when its input is logic 0 and the output is logic 1. In this case, the only sensitive region is the drain junction of the transistor *M2*. If this junction is hit by an energetic particle, it can induce a negative glitch at the inverter output. When the input is logic 1, and the output is logic 0, transistors *M1* and *M2* are in ON state, whereas transistor *M4* is in its OFF state. Therefore, if a SET occurs at node v_a, the glitch can turn ON transistor *M4* and propagate the glitch to the output of the circuit. But, it requires large amplitude of the SET to generate the glitch at the output, because due to the feedback controlled pull-down network the glitch recovers and the possibility to have a SET at the circuit output is hardly available. In this case, the only potential sensitive region is the drain junction of *M4*. However, there is no electric field in this region which could split the generated electron-hole pairs and produce a net charge that alters the output voltage. The voltage drop across this junction is 0 V (the drain is at 0 V, and also the substrate is biased at 0 V).

The node having logic '1' in CUT is weaker and more susceptible to soft errors than the node having logic '0', since it exhibits a smaller critical charge [40]. The CMOS inverter has only one sensitive node which is responsible for flipping the logic of the output, whereas, ST and NST-VB have two additional internal nodes v_a and v_b which may affect the flipping of output of the circuit. If a high energy particle hits node v_a of the ST circuit, a current pulse with very high magnitude needs to be generated to flip the logic. Indeed, the effect of a SET on node v_a of ST is recovered by feedback transistor *M6*, and a flipping of the output node cannot practically occur. As for an energetic particle hitting node v_a of the NST-VB circuit, the following two situations need to be considered. If $v_x = 0V$ ($v_{in} = 0$ in Fig. 1(b)), then *M6* is in its ON state and $v_a = V_{dd1} = V_{dd} + V_{thn}$. In this case, *M4* is also in the ON state, and thus charges the output v_{out} up to V_{dd}. Moreover, *M1* and *M2* are both in the OFF state. An energetic particle hitting node v_a can induce a temporary discharge of such a node, and thus temporarily switching off transistor *M4*. As a result, node v_{out} turns out to be in high impedance, but its logic value does not change. The temporary glitch on v_a is readily recovered by transistor *M6* that re-established the correct value V_{dd1}. If $V_x = V_{dd}$, *M5* is in the ON state and $v_a = 0V$. In addition, both transistors *M1* and *M2* are ON and v_{out} is discharged to ground. If an energetic particle hitting node v_a induces a high enough positive glitch, this can temporarily turn ON transistor *M4*, thus propagating the glitch to the output node. This positive glitch can be further confirmed by the feedback transistor *M3*. However, when the proper low voltage value of node v_a is recovered by the action of transistor *M5*, the correct output value is re-established.

Let us now consider node v_b of the NST-VB circuit. If $V_x = 0V$, the transistors *M1* and *M2* are in the OFF state, whereas *M3* is the ON state and drives node v_b to $V_{dd} - V_{th}$. The effect of a particle hit temporarily discharging node v_b cannot propagate to the output, since transistor *M2* is in the OFF state, and is readily recovered by the action of transistor *M3*. If $V_x = V_{dd}$, instead, the transistors *M1* and *M2* are in the ON state, and $v_b = v_{out} = 0V$. It is worth noting that no SET can be induced on v_b, since there is no electric field across its junction that can split the electron-hole couples generated by a possible particle strike. Similarly, the ST circuit has feedback network in both pull-up and pull-down networks. The SET at node v_a and v_b can generate a glitch at the output but it is recovered by the feedback networks and no logic flipping [41]. Table I shows the critical charge of different sensitive nodes of CMOS, ST, and NST-VB based inverter circuits. Here, *Z* indicates the high impedance state and NA indicates the no critical charge. For some sensitive nodes of the circuits, the critical chage can not be calculated because there is no logic flipping at the output of SET occurs at the respective sensitive nodes. From results, it is observed that the input node V_x (v_{in} in the Table I) of the CUT has the lower critical charge compared to all other sensitive nodes. Hence, for the further soft-error analysis, node V_x of all the circuits have been considered. The critical charge for the NST-VB circuit is 78.09% and 47.8% higher as compared to the CMOS and ST circuits, respectively. Further, we will show the

Table I
Critical charge at sensitive nodes of different logic circuits considering NBTI.

Logic circuits	Sensitive nodes	Temporary logic flipping	Critical charge (fC)	
			$V_x = 0$	$V_x = 1$
CMOS	v_{in}	Yes	0.857	0.776
ST	v_{in}	Yes	2.605	0.935
	v_a	No	NA	NA
	v_b	No	NA	NA
NST-VB	v_{in}	Yes	2.628	1.382
	v_a	No	Z	NA
	v_b	No	NA	NA

impact of PBTI in all the considered circuits in subsequent sections.

3.3. Soft error rate

Soft errors in any digital circuit arise when a high energy particle from chip packaging materials or cosmic radiation induces enough charge that, if collected by a sensitive node it can change the logic value of the hitted circuit node. Here, the soft error rate on circuits is analyzed without considering memory cells or latches. As already discussed, the basic building blocks like inverters must be resilient to NBTI and soft errors for designing NBTI tolerant, robust, and reliable SRAM cells. To do this, SER of inverter circuits must be analyzed carefully to get a better perspective while designing latches and memory elements. Circuits designed using advanced technology are extremely susceptible to soft errors because of lower critical charge assigned to the lower supply voltages and smaller node capacitances. The soft error resilience of any circuit can be evaluated from its Q_{crit}. The soft error rate (SER) is exponentially dependent on Q_{crit} and found that the SER is inversely proportional to Q_{crit} [42]. SER can be express by.

$$SER \propto N_{flux} A e^{-\frac{Q_{crit}}{Q_S}} \tag{4}$$

with N_{flux} is the neutron flux intensity, Q_S is the device charge collection efficiency (in *fC*), and A is the sensitive node cross section area. The above equation describes that a small change in Q_{crit} will significantly reduce the SER.

For the validation of soft error hardening enhancement on NST-VB and other circuits, the approximate soft error rate ratio (SERR) with and without stress is introduced. The SERR can be calculated by assuming all other parameters are unaffected except Q_{crit} for particular stress conditions

$$SERR = \left.\frac{SER_3}{SER_0}\right|_{@V_{dd}} \tag{5}$$

or

$$SERR \approx antilog_e[Q_{crit}^{@0year} - Q_{crit}^{@3years}]|_{@V_{dd}} \tag{6}$$

where SER_0 and SER_3 are the soft error rates, and $Q_{crit}^{@0year}$ and $Q_{crit}^{@3years}$ are the critical charges at no stress and after three years of stress, respectively. A lower the SERR means better radiation hardening enhancement of the design and vice versa.

4. Simulation results and discussions

This section presents the simulation results obtained considering the setup described in Section 3.1. Fig. 4 presents the results concerning the NBTI induced delay degradation extracted from the three inverters after different stress times. The circuit delay is calculated for both DC stress and AC stress. The DC stress means that the input is constant for the whole stress time whereas, while for AC stress, both stress and recovery phases occur. The AC stress effect depends on the input duty cycle, where we considered a duty cycle of $\beta = 0.75$, 0.5, and 0.25 for the analysis. One can observe from Fig. 4 that the NST-VB circuit exhibits the minimal delay increment for both AC and DC stress when compared to CMOS and ST counterparts. When changing the AC stress between the two extreme duty cycle cases ($\beta = 0.75$ and $\beta = 0.25$) the CMOS, ST, and NST-VB implementations exhibit a change of the delay of approximately 25.2 ps, 122 ps, and 11.7 ps, respectively, after three years of device stress. This suggests that the NST-VB design does not only provide the least delay increase of the considered candidates but also is less sensitive to duty cycle changes. The delay degradations due to DC stress is also shown in Fig. 4 and shows that the DC stress effect is more severe when compared to the one induced by AC stress which is consistend with [43,44]. The results further indicate that after three years of stress the NST-VB circuit exhibits the smallest delay shift of 0.47%, while ST and CMOS counterparts experience 7.2% and 5.32% delay

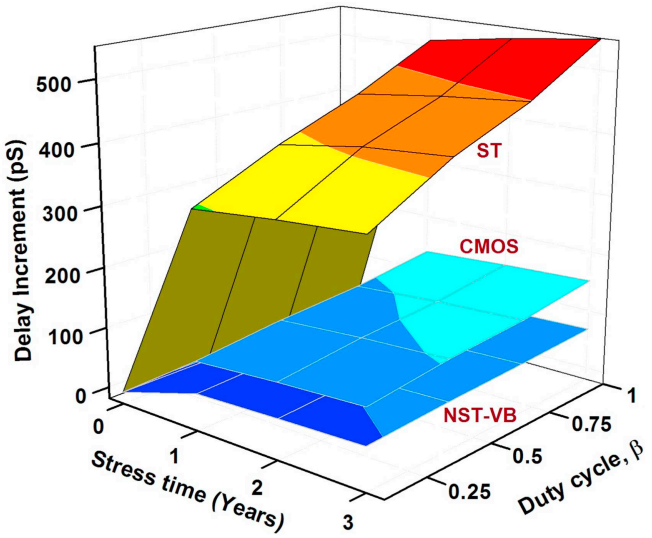


Fig. 4. Delay increment of different inverters for various duty cycles (β) and stress times.

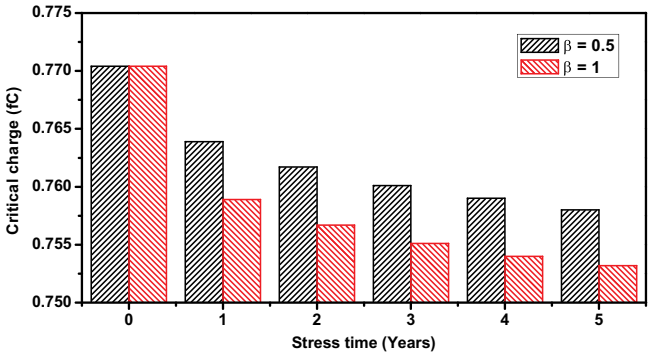
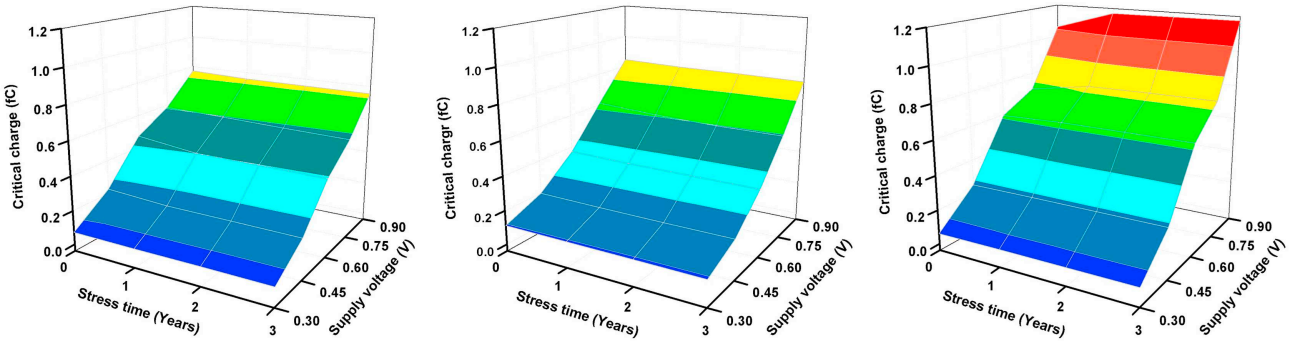


Fig. 5. Critical charge variation of CMOS inverter with different NBTI stress time and duty cycles.

shifts, respectively. The fact that the ST circuit is more affected by NBTI can be related to the three PMOS transistors in the PUN network hence the stress probability is higher than the CMOS inverter.

In Fig. 5, the Q_{crit} values at the CMOS inverter input node for different stress times considering stress ratio (duty cycle) of 0.5 and 1 are shown. It illustrates that the output node is temporarily discharging due to hitting particles when it is handled by the NBTI affected PUN. At the stress time $t_s = 0$ years, the critical charge exhibits is maximum and as the circuit ages, Q_{crit} of the circuit decreases too. The decrement in critical charge is 1.61% and 2.23% after the stress time of five years for stress ratio 0.5 and 1, respectively. The value of Q_{crit} decreases with a higher rate during the initial phase of stress than during remaining stress period.

The effect of supply voltage variations at different stress time for CMOS, ST, and NST-VB based inverter circuits is captured in Fig. 6. The figure indicates that the critical charge of CMOS and ST inverter decreases with the increasing stress time, whereas the critical charge increment for the NST-VB circuit is diminishing when increasing the stress time. It is obvious that the critical charge of all the topologies increases with the increasing supply voltage [20,37]. From Fig. 6, however, we can observe that the rate of critical charge increment for NST-VB circuit with the supply voltage is higher compared to ST and CMOS inverter. Therefore, our approach is more effective than ST and CMOS inverters in improving the soft error robustness by increasing the supply voltage. This is confirmed by the results reported in Table II. This is remarkable as it suggests that the reliability and radiation



(a) (b) (c)

Fig. 6. Critical charge varitation at different supply voltages and at different stress times for (a) CMOS inverter (b) Schmitt trigger (c) NST-VB circuit.

Table II
Sensitivity of the critical charge to the supply voltage (*fC/V*) of logic circuits for different stress times.

t_S (years)	Logic circuits ↓		
	CMOS	ST	NST-VB
0	1.162	1.222	1.664
1	1.146	1.207	1.846
2	1.143	1.202	1.849
3	1.140	1.195	1.853

hardening of NST-VB based designs benefit from the voltage scaling, while the other ones experience reliability degradation and are affected by radiation.

For the static power reduction in memories and logic circuits, two techniques namely dynamic voltage scaling (DVS) [45] and power gating [46] are used. Results demonstrate that the NST-VB has better radiation hardening for supply voltage change, and thus it is useful to implement the drowsy cache memories [47] having DVS to lower the static power consumption of the circuit. The NST-VB circuit has a higher critical charge compared to CMOS and ST circuit even at lower V_{dd} which makes the design more resilient to soft-errors. Results also show that the use of DVS on NST-VB also increases the SER over time due to aging [48]. The results in Fig. 6 and Table II show that NST-VB provides a higher soft error resilience improvement when the supply voltage is increased with DVS, in comparison with alternative CMOS and ST based solutions.

As our purpose is to evaluate NST-VB regarding soft error resilience, we first need to discuss theoretical aspects related to critical charge sensitivity analysis of the considered circuits.

4.1. Critical charge sensitivity analysis

The critical charge sensitivity of any circuit can be defined as the critical charge variation concerning the change in different stress conditions. Critical charge sensitivity is the function of various parameters such as stress time t_S, supply voltage V_{dd}, threshold voltage V_{th}, and input signal probability $P(v_{in})$ which defined as

$$\Delta Q_{crit} = f\{t_S, V_{dd}, V_{th}, P(v_{in})\}. \tag{7}$$

For understanding the sensitivity of Q_{crit} on NBTI, the stress time t_S and the supply voltage V_{dd} are helpful as intermediary parameters. Furthermore Q_{crit} of any CMOS circuit affects $P(v_{in})$. The threshold voltage V_{th} is the major parameter of PMOS transistor and is used as an important parameter to evaluate the critical charge sensitivity to NBTI [49]. Thus, Q_{crit} sensitivity to NBTI is a combination of all these sensitivities and can be expressed by

$$\frac{\partial Q_{crit}}{\partial V_{th}} \approx \left(\frac{\partial Q_{crit}}{\partial V_{dd}} \times \frac{\partial Q_{crit}}{\partial P(v_{in})}\right) \Big/ \frac{\partial Q_{crit}}{\partial t_S} \tag{8}$$

The dominating components for the critical charge sensitivity analysis due to NBTI of circuits are the critical charge sensitivity to supply voltage $\frac{\partial Q_{crit}}{\partial V_{dd}}$, and the critical charge sensitivity to stress time $\frac{\partial Q_{crit}}{\partial t_S}$. For particular operating conditions, assuming equal input probability [$P(v_{in}=0) = P(v_{in}=1) = 0.5$], $\frac{\partial Q_{crit}}{\partial P(v_{in})}$ is less effective. Whereas, V_{dd} change and t_S are the major variable due to NBTI, the following approximation can be considered to simplify the analysis

$$\frac{\partial Q_{crit}}{\partial V_{th}} \approx \frac{\partial Q_{crit}}{\partial V_{dd}} \Big/ \frac{\partial Q_{crit}}{\partial t_S} \tag{9}$$

The critical charge increment for unstressed CMOS, ST, and NST-VB when supply voltage changes from 0.3 V to 0.9 V are 0.6975fC, 0.7334fC, and 0.9985fC, respectively. On the other hand, critical charge for CMOS, ST, and NST-VB, after stressing the device for three years increase by 0.6843fC, 0.7168fC, and 1.112fC, respectively, when supply voltage raises from 0.3 V to 0.9 V. The critical charge sensitivity to supply voltage of various inverter circuit for different stress time can be expressed as

$$\text{Sensitivity}|_{t_S} = \frac{Q_{crit}\,|_{V_{dd}^H} - Q_{crit}\,|_{V_{dd}^L}}{V_{dd}^H - V_{dd}^L} \tag{10}$$

where $V_{dd}{}^H$ and $V_{dd}{}^L$ are the higher and lower supply voltages, respectively. From Eq. (10) we can observe that the sensitivity of the circuit increases if the change in critical charge is large. From Table II, it is perceived that the NST-VB circuit has the higher critical charge w.r.t. the supply voltage sensitivity when compared with the CMOS and ST based counterparts for different stress times. Also, the sensitivity for NST-VB increases with stress time, whereas it decreases with the stress time for CMOS and ST circuits. The sensitivity of CMOS and ST is decreased by 1.93% and 2.32%, whereas the sensitivity of NST-VB is increased by 10.19% after the three years of device stress. From the above analysis we can conclude that as NST-VB circuit performs well concerning critical charge to supply voltage sensitivity and increments with increasing stress time. The NST-VB circuit has improved sensitivity when compared with ST and CMOS by 36.15% and 43.16%, respectively, without NBTI stress whereas NST-VB has improved sensitivity when compared with ST and CMOS by 55.10% and 62.48%, respectively, after three years of device stress.

From the above discussion it is perceived that the $\partial Q_{crit}/\partial t_S$ for NST-VB is positive, which decreases the effective $\partial Q_{crit}/\partial V_{th}$, meaning that the effect of NBTI is less on NST-VB circuit critical charge variations. The NST-VB behaves differently because it only consists of NMOS transistors in the critical path. The PMOS transistor is present in the secondary circuit (voltage booster), but the effect of NBTI occuring in the voltage booster does not affect the circuit performance with time due to aging.

Table III
Soft error rate ratio (SERR) of different logic circuit after three years of stress.

V_{dd}	Logic circuits ↓		
	CMOS	ST	NST-VB
0.3 V	1.0021	1.0013	0.9963
0.9 V	1.0154	1.0181	0.8896

The viability of radiation hardening enhancement by increasing V_{dd} is measured for different circuits using the SERR as defined in Eq. (6). The SERR at two supply voltages 0.3 V and 0.9 V for all the considered circuits after three years of device stress time is given in Table III. Results demonstrate that the NST-VB has better SERR than the CMOS and ST based inverter for both the supply voltages. From the results it is also observed that the NST-VB has 12.62%, and 12.39% less SERR when compared with the ST and CMOS based inverters. Thus the NST-VB is best suited for the implementation of reliable and radiation hardened circuit applications. Further, for the analysis for radiation hardening enhancement, we need to analyze the flipping margin of all considered circuits.

4.2. Flipping margin analysis

Fig. 7 exhibits the margin and overlap voltages for the NST-VB circuit and the CMOS inverter for different amplitudes of high energy particle dose equivalent to the exponential current pulse. Results show that the NST-VB circuit is more tolerant to the high energy particle compared to CMOS inverter without stress and after five years of stress. From the result, it is observed that the CMOS inverter tends to flip even at a low current amplitudes depending on the stress time, whereas NST-VB flipping energy is unaffected by the stress. Results also show that, if the dose amplitude for CMOS is high, the overlap voltage magnitude is more than the V_{dd}. The rate of margin decrement is less for NST-VB circuit whereas the CMOS inverter has the high rate of margin decrement at around their critical peak current. The rate of margin decrement for CMOS inverter and NST-VB circuit are 96.43 $mV/\mu A$ and 17.83 $mV/\mu A$, respectively. From the above discussion, we can observe that the NST-VB is less sensitive to the applied high energy particle energy.

Fig. 8 presents the simulation results obtained when α-particles with the different energy (low is equivalent to CMOS critical charge and high is equivalent to NST-VB critical charge) hit the sensitive node within two NOT chains using NST-VB circuit and CMOS inverter, respectively, at two phases of circuit life time (the prestine circuit and the circuit after five years of stress) [21]. The worst case situation has been considered when the sensitive node is driven by a Pull-Up network (PUN). Fig. 8 reveals the glitches induced at V_x and V_y due to two hitting particle with the same energy at the V_x of the CMOS and NST-VB

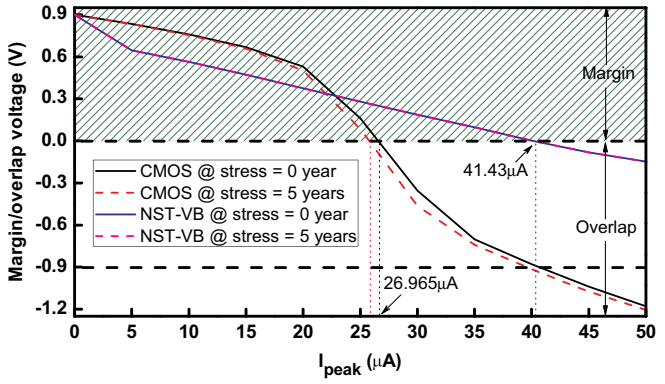


Fig. 7. Energy to flipping margin/overlap investigation of CMOS inverter and NST-VB circuit without stress and after five years of device stress.

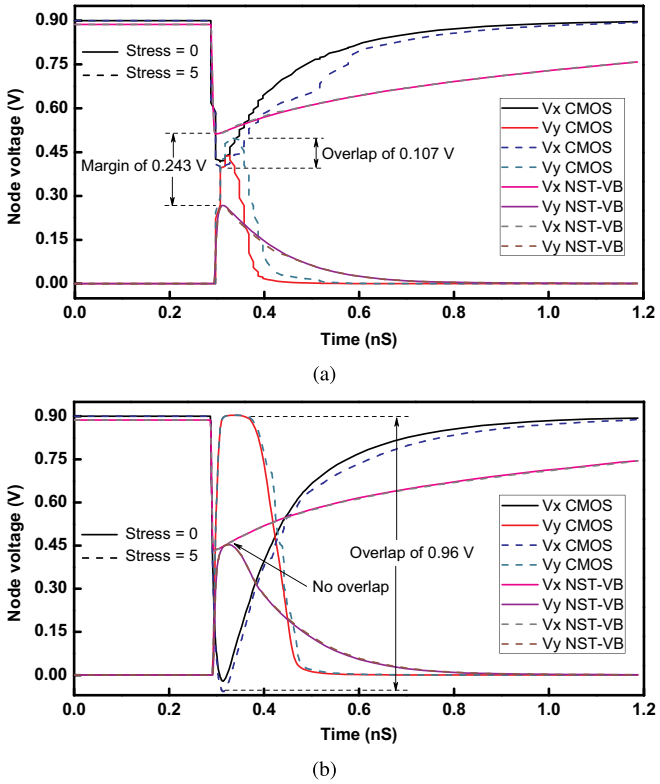


Fig. 8. Simulation results for two high energy particles (equivalent to current pulse) with different amplitudes for hitting a node of a CMOS and NST-VB inverter chain without stress and after five years of stress (a) $I_{peak} = 26.965\mu A$ (b) $I_{peak} = 41.43\mu A$.

circuit. As can be seen from above figures, even for two hitting particles with the same energy the amplitude of the induced glitch is higher for CMOS inverter after five years of stress than for the prestine circuit. It can also be observed that at low and high energy of hitting particles the amplitude of the glitch is less for NST-VB as compared to CMOS inverter, and is unaffected after five years of stress. At higher energy, the flipping overlap for CMOS inverter is more as compared to lower energy. The various overlaps and margins for CMOS and NST-VB inverter at different stress time and energy are summarized in Table IV. From results, it is observed that the NST-VB circuit is less affected by NBTI stress time and has a higher critical charge when compared with the CMOS inverter. Further, we have also analyzed the effect of PBTI in NMOS transitors with NBTI in PMOS transistors in subsequent section.

4.3. Effect of NBTI and PBTI on the circuits

To analyze the circuit in the presence of both NBTI and PBTI, we evaluated the critical charge by means of HSPICE simulations with and without BTI stress at the most sensitive node V_x (as shown in Fig. 3) of the considered circuits. We evaluated the critical charge for the input

Table IV
Flipping margin of CMOS and NST-VB based inverter for different amplitudes of high energy particles (equivalent to current pulse).

I_{peak}	t_S (years)	Logic circuits ↓	
		CMOS	NST-VB
26.965 μA	0	0	Margin 0.243 V
	5	Overlap 0.107 V	Margin 0.243 V
41.43 μA	0	Overlap 0.93 V	0
	5	Overlap 0.96 V	0

Table V
Critical charge at the sensitive node V_x for the input combination without and after three years of BTI stress considering NBTI only and combinational NBTI + PBTI stress.

Logic circuits	Stress	Critical charge (*fC*)	
		$V_x = 0$	$V_x = 1$
CMOS	Fresh	0.857	0.777
	NBTI	0.855	0.766
	NBTI + PBTI	0.851	0.763
ST	Fresh	2.605	0.935
	NBTI	2.582	0.917
	NBTI + PBTI	2.557	0.915
NST-VB	Fresh	2.628	1.382
	NBTI	2.594	1.350
	NBTI + PBTI	2.502	1.327

combinations at the sensitive node for all three considered circuits. From Table V, it is observed that the critical charge is lower at the sensitive node for all the considered circuits if the sensitive node dwells in its logic high state. Thus logic high at the sensitive node is considered as the critical input combination for further analysis. Results also demonestrate that the critcal charge difference for the input combinations are high for the circuits having the feedback arrangement (ST and NST-VN) compared to CMOS inverters. This indicates that the critical charge can be enhanced by using the feedback topology of the circuits. By considering only NBTI stress, and both NBTI and PBTI stress after three years of device stress, the critical charge decreases for all the considered circuits. The less pronounced effect of PBTI is observed in CMOS inverters for the critical input case because the CUT is driven by the PMOS of input inverter. The effect of PBTI is very weak in the circuits because the CUT is driven by input inverter and load inverter and these two inverters are deciding the critical charge of the sensitive node of CUT. This proves that the effect of BTI depends on the degradation of the circuit. Results show that, even though the effect of BTI presents in all the circuits, the critical charge is high for the proposed NST-VB circuit. Thus, the NST-VB circuit is more robust for radiation hardening with the presence of temporal degradations.

It is worth noting that, although the values of the critical charge will change for different, more scaled technologies, since it depends on the electrical parameters of the circuit (mainly V_{dd}, V_{th}, driver strength and node capacitance), we expect analogous results from the qualitative point of view. In addition, as for FinFET technology, it is more robust against BTI than planar MOSFET, and therefore its soft error robustness is less affected by BTI [50].

4.4. Power and area analysis

We also analyze the power dissipation and area for all the considered circuits, as given in Table VI. As we can see, the Schmitt trigger has higher power consumption as compared to standard CMOS inverter. As NST-VB is the modified version of the conventional Schmitt trigger, the power dissipation for NST-VB is also higher than the standard CMOS inverter. The dynamic power for NST-VB is less as compared to a conventional ST circuit because the NST-VB circuit uses only NMOS transistors in the critical path. The higher mobility of electrons leads to faster transition, and hence less switching power is dissipated, which further decreases the overall dynamic power dissipation. As the supply voltage of voltage booster is threshold voltage higher than the main supply voltage, the static power dissipation is higher in the NST-VB circuit as compared to the CMOS inverter and ST based inverter.

Table VI
Performance parameters for different logic circuits.

Parameters	Logic circuits		
	CMOS	ST	NST-VB
Static power (nW)	6.757	5.832	25.165
Dynamic power (μW)	0.077	2.644	2.462
Area (μm^2)	3.584	12.288	9.216

The area of the NST-VB circuit is lower than the ST circuit. Even though the number of transistors is six for both ST and NST-VB, the area is less because of the use of only NMOS transistors for the conduction. The lower sized NMOS transistor provides the same voltage swing when compared with the higher sized PMOS used in the ST circuit.

4.5. Process variation analysis

For the analysis of soft error resilience and process variations on CMOS, ST, and NST-VB inverter, we performed 5000 Monte Carlo simulations for the critical input and output voltages as depicted in Fig. 9. The simulation results show that the mean value μ for critical input and output voltages of CMOS and ST are lower than at the NST-VB circuit. The standard deviation (σ) from the mean value for CMOS inverter has 168.68% and 13.8% more for input and output critical voltages, respectively, as compared to NST-VB circuit. Similarly, The standard deviation σ from the mean value for ST inverter has 12.12× and 6.89× more deviation for input and output critical voltages, respectively, as compared to NST-VB circuit. Further, we also evaluated the process variability as a figure of merit for the critical voltages of all the considered circuits. The process variability is the ratio of the standard deviation and the mean value of the critical voltages. For the better tolerance to the process variations, the variability should be as small as possible [51]. Fig. 10 shows the variability for the critical voltages for all the considered circuits and we observe that the NST-VB has less variability compared to the CMOS and ST based inverter circuits. Furthermore, our results demonstrate that the variability at node V_x for NST-VB is 2.79× and 43.86× lower than the CMOS and ST based inverters, respectively. Similarly, the variability at node V_y for NST-VB is 1.18× and 5.28× lower than for the CMOS and ST based inverters, respectively. The variability at the V_x is higher because the SET occurs at the input side of the CUT and is transfered to the node V_y. From the above discussions, we can conclude that the most sensitive input node of NST-VB circuit has less effect of process variations as compared to CMOS inverter sensitive node. As the NST-VB circuit has less variability issues, hence it is useful for reliable and stable circuit applications.

5. Conclusion

In this paper, we analyze the potential impact of replacing CMOS inverters and Schmitt Trigger (ST) by more reliable components, i.e., NST-VB, as reliability enhancement design-time solution. The comparison concerning delay variation of the three candidates, all implemented in 32 nm CMOS technology, revealed that after three years of NBTI stress, NST-VB exhibits an almost negligible delay shift of 0.47%, while ST and CMOS inverter experiences a significant delay shift of 7.2% and 5.32%, respectively. Moreover, our evaluations indicated NST-VB have improved sensitivity of 62.48% and 55.10%, against CMOS inverter and ST, respectively, after the three years of stress time. To better assess soft error resilience, we introduced a soft-error rate ratio (SERR) as the performance metric. Our analysis indicates that NST-VB has 12.62%, and 12.39% less SERR as compared to ST and CMOS based inverters, respectively, which shows that the NST-VB is more tolerant to soft error than the alternative circuits. Finally, soft-error impact and process variation analysis on NST-VB circuit and CMOS inverter are performed using 5000 Monte Carlo simulations for critical voltages and we observe that the standard deviation of NST-VB is 168.68% less as compared to CMOS inverters. This demonstrates that NST-VB logic circuits constitute a viable approach which provides the best radiation hardening enhancement and effective resilience against NBTI effects.

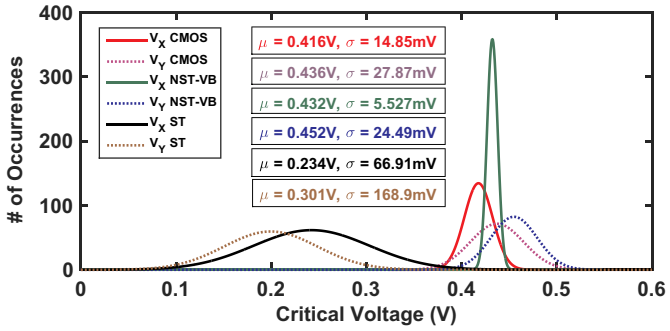


Fig. 9. 5000 Monte Carlo simulations of V_x and V_y critical voltages (V_{crit}) for CMOS, ST and NST-VB based inverters.

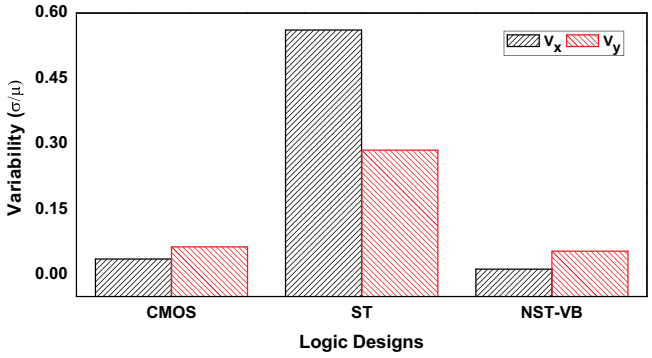


Fig. 10. Process variability (σ/μ) of V_x and V_y critical voltages (V_{crit}) for CMOS, ST and NST-VB based inverters.

Author statement

Ambika Prasad Shah: Conceptualization; Data curation; Formal analysis; Funding acquisition; Investigation; Methodology; Validation; Visualization; Roles/Writing – original draft.

Daniele Rossi: Visualization; Investigation; Validation; Roles/Writing – original draft.

Vishal Sharma: Methodology; Software.

Santosh Kumar Vishvakarma: Resources; Software; Supervision; Project administration.

Michael Waltl: Resources; Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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