Extraction of Statistical Gate Oxide Parameters From Large MOSFET Arrays

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***Abstract*—In modern MOS technologies continuous scaling of the geometry of transistors has led to an increase of the variability between nominally identical devices. To study the variability and reliability of such devices, a statistically significant number of samples needs to be tested. In this work we present a characterization study of defects causing BTI and RTN, performed on custom built arrays consisting of thousands of nanoscale devices. In such nanoscale devices, variability and reliability issues are typically analyzed for individual defects. However, the large number of measurements needed to extract statistically meaningful results make this approach infeasible. To analyze the large set of measurement data, we employ statistical distributions of the threshold voltage shifts arising from defects that capture and emit charge. This allows us to extract defect statistics using a defect-centric approach. Defect distributions are characterized for various gate, drain and bulk biases, and for two geometries to verify the methodology and to obtain statistics suitable for TCAD modeling and lifetime estimation. With the TCAD models we extrapolate the observed degradation of the devices. Finally, we investigate the influence of bulk and drain stress biases on the defects and observe that the impact of bulk bias on the device degradation is similar to that of the gate bias. In contrast, drain stress with drain biases up to $-0.45\,\mathrm{V}$ appears to be negligible for the investigated technology. Our measurements also clearly reveal that the overall BTI degradation is heavily dependent on the gate-bulk stress bias, while the extracted number of RTN defects seems to be independent on stress.**

***Index Terms*—BTI, RTN, reliability, defect-centric, array, TCAD, NMP.**

I. Introduction

MINITATURIZATION of MOSFETs has led to an increase in variability among individual devices. The performance of such devices is strongly affected by atomistic defects, located at the channel/insulator interface or within the gate oxide. Characterizing their behavior as well as their prevalence in a technology is a necessity for understanding the reliability of modern FETs [1]–[3]. In this work, we characterize defects present in pMOS transistors which have been fabricated in dedicated array structures. The degradation mechanisms we focus on in our study are the bias temperature instabilities (BTI) [4], and random telegraph noise (RTN) [5]. These effects are often studied on individual devices, which allows to study the trapping kinetics of the involved defects in detail by analyzing recovery traces for discrete steps, which correspond to charge transitions of single defects. Here, we focus on statistical characterization of these effects by analyzing a significant number of devices. The observed degradation is then not analyzed at the single device/single defect level, but over a large set of devices in a probabilistic manner. This is done by drawing distributions of the degradation of ΔV_{th} over the set of devices and explaining them using the defect centric approach [6].

In Section II, we will discuss the test structures, and describe the details of the measurements performed. In Section III, the defect centric approach to defect characterization will be outlined. Finally, in Section IV, the results obtained will be presented and discussed. The discussion will be aided by numerical simulations of the measurements. To extend our understanding of charge trapping for this particular technology, we extend our previous study [7] on the same arrays by lifetime extrapolation and the investigation of stress bias applied to the bulk and drain terminals.

II. Devices and Measurements

The devices used in this work are fabricated in a commercial technology, and comprise high-k/metal gate, planar pMOS FETs with a gate width of $W = 100\,\mathrm{nm}$ and length of $L = 30\,\mathrm{nm}$ (henceforth called *short devices*) and $L = 150\,\mathrm{nm}$ (*long devices*). The FETs are organized in array structures consisting of more than 3000 individually addressable devices. The devices can be selected using electrically controlled double transmission gates which allow to switch the external gate and drain connections to individual rows and columns of the array using on-chip logic. The source and bulk contacts are shared among all devices, as shown in Figure 1. Secondary gate and drain lines exist to keep devices not selected at a defined bias. These gate and drain lines were supplied with $V_{\mathrm{G}} = 0.15\,\mathrm{V}$ and $V_{\mathrm{D}} = 0.0\,\mathrm{V}$ respectively. Further details about the array chips can be found in [8].

Manuscript received March 23, 2020; accepted March 27, 2020. Date of publication April 2, 2020; date of current version June 5, 2020. This work was supported by the Take-Off Program of the Austrian Research Promotion Agency FFG under Project 861022 and Project 867414. *(Corresponding author: Bernhard Stampfer.)*

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Digital Object Identifier 10.1109/TDMR.2020.2985109

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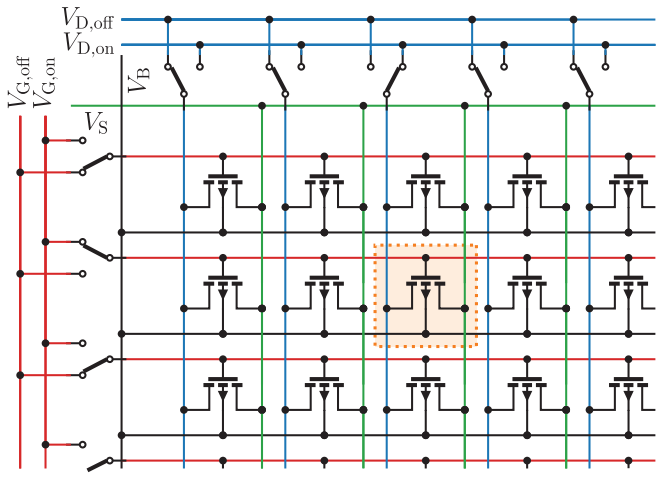

Fig. 1. Electrical layout of the gate, drain, source and bulk lines of the array chip used for characterization. The $V_{G,on}$ and $V_{D,on}$ connections form the rows and columns of the array and allow selecting a device. Devices in other rows and columns are supplied with $V_{G,off}$ and $V_{D,off}$, respectively. The source and bulk connections are shared among all devices.

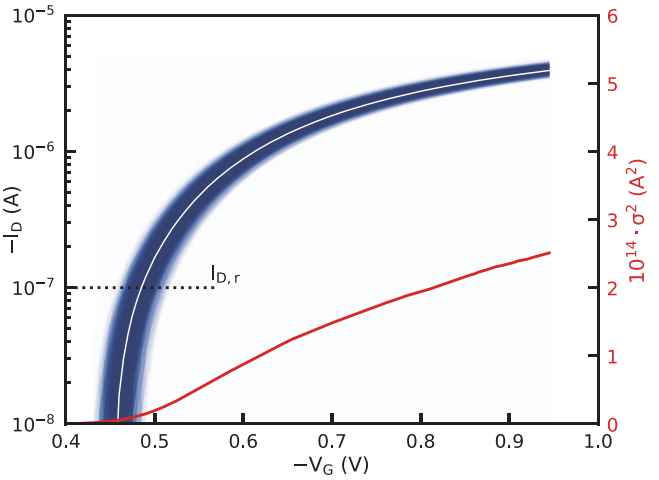

Fig. 2. Transfer characteristics for the array of long devices (blue), their mean (white), and variance (red). The dashed black line indicates the drain current used to set the relaxation voltages for the MSM sequences.

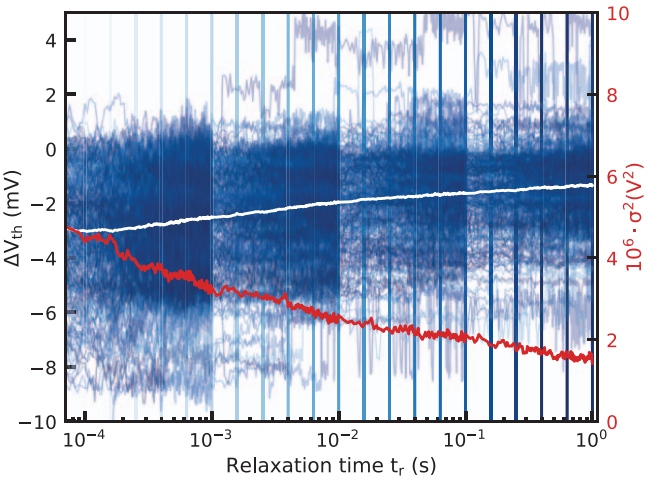

Fig. 3. Threshold voltage shifts (ΔV_{th}) after stress for one set of measurements (blue), their mean (white), and variance (red). The curves are obtained by mapping the measured drain current (I_D) to ΔV_{th} using the virgin $I_D(V_G)$ curves for each device. The vertical lines indicate points in time at which distributions of ΔV_{th} are drawn for the statistical characterization. Note that the visible change in measurement noise between decades in t_r is a consequence of increasing the sampling time with each decade.

For the characterization our custom-designed TDDS measurement instrument is used [9], which also controls the device selection logic of the device. The measurements are performed in 39 sets, at short and long devices and various stress biases. Each set consists of a number of measurements performed sequentially on all devices of the corresponding array. The gates of all devices arranged in a row are electrically connected. Thus, the devices which are connected to the same gate line as the selected device will be subjected to the same gate stress. To prevent this from affecting characterization, the scheme for sequential selection of the devices steps the rows in the inner loop and the columns in the outer loop. This gives the device in the next column sufficient time to recover until it is selected for measurement. The measurement sequence consists of an initial $I_D(V_G)$ followed by extended measure-stress-measure (eMSM) sequences with stress phases of $t_s = \{2, 10, 100, 1000, 10000\}$ms, and relaxation phases of $t_{r,max} = 1$ s during which the drain current is recorded. The recordings are started with a measurement delay of 100 µs after stress release, with 200 sampling points per decade in time at $V_{G,rec}$ corresponding to $I_{D,r} = 10\,\mu$A, which is determined from the initial $I_D(V_G)$. During the measurements, the chip is kept at a constant temperature of 35 °C. An exemplary set of $I_D(V_G)$ curves is shown in Figure 2. It should be noted that due to the devices being part of a large array with shared drain lines, all devices in the selected column will contribute to the measured drain current. Thus, the off-currents of a number of devices will add to the current of the selected device. This makes it difficult to obtain the true off-current of the single selected device.

After the measurements, the recorded relaxation currents are mapped to an equivalent ΔV_{th} using the initial $I_D(V_G)$ curves. A set of ΔV_{th} traces is shown in Figure 3. The characterization of the threshold voltage shift is not affected by the spurious off-currents, as the additional current is present in both the initial $I_D(V_G)$ and in the relaxation measurements, and thus does not affect the mapped ΔV_{th}. From these data, a distribution of ΔV_{th} over all measured devices—as will be evaluated in the next section—can be drawn for any moment in relaxation time.

To check if all devices behave similarly over the area of the array, Figure 4 shows the variability of ΔV_{th} over the transistor array after stress at $V_G = -1.45$ V. Neither the fine-grained nor the coarse representations show any unusual clusters or drift of ΔV_{th} over the array area.

III. Defect Characterization

From the relaxation measurement data we extract cumulative density functions of ΔV_{th} as shown in Figure 5.

The shape of these distributions is governed by three main contributions.

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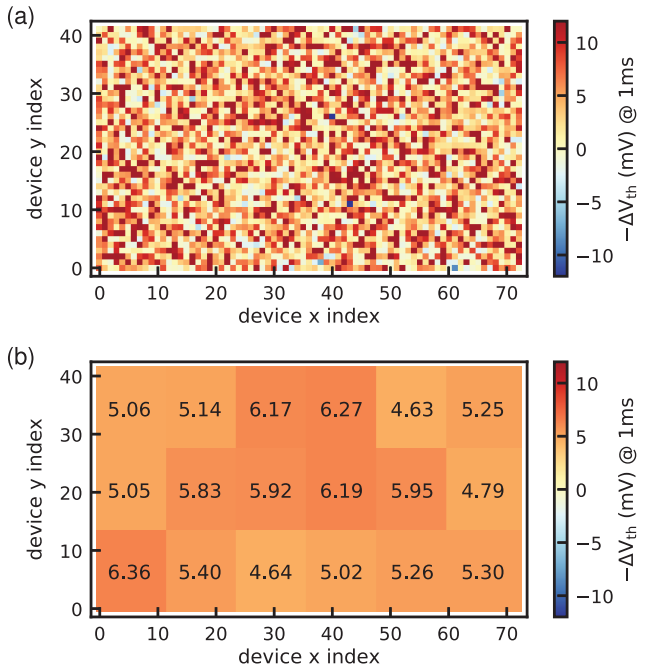

Fig. 4. Threshold voltage shift (ΔV_{th}) evaluated at $t_{\text{r}} = 1$ ms after $t_{\text{s}} = 10$ s of stress at $V_{\text{G}} = -1.45$ V, measured on the short devices. Shown per device as positioned on the array (top), and clustered into larger blocks (bottom). The bottom plot underlines the homogeneous degradation of the devices over the area of the array.

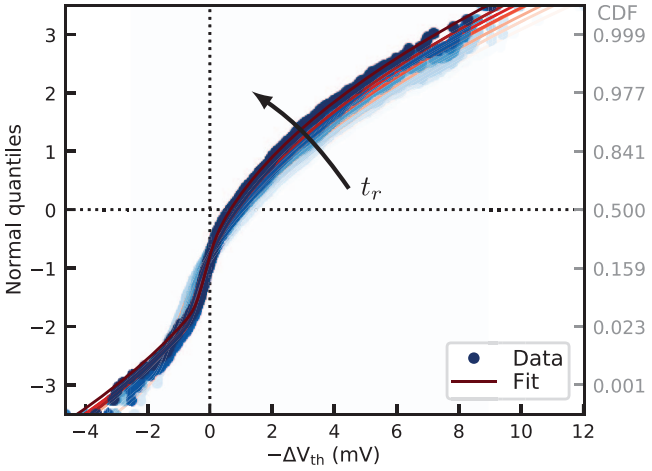

Fig. 5. Cumulative density functions of the threshold voltage shift during relaxation. Blue: Extracted from a measurement on the long devices after 10 ms of stress at −1.45 V. Red: Fitted theoretical distribution. The theoretical model shows good agreement with the observed distributions.

- Defects which show BTI behavior, i.e., capturing charge during stress and emitting it during relaxation, thereby causing a degradation of the threshold voltage (increased $-\Delta V_{\text{th}}$) up to a certain relaxation time
- Defects which show RTN behavior, i.e., randomly capturing or emitting charge between the initial $I_{\text{D}}(V_{\text{G}})$ and the measurements, thereby causing either a positive or negative shift in ΔV_{th}
- Gaussian noise, adding normally distributed shifts to the data.

By describing each of these effects statistically, the CDFs observed in the measurements can be reproduced. While this generally requires a numerical approach, analytical expressions which directly give the number of charged defects (N) and their average step height (η) are available, given the data is dominated by BTI [6]:

$$N = \frac{\langle \Delta V_{\text{th}} \rangle}{\eta} \tag{1}$$

$$\eta = \frac{\sigma^2}{2\langle \Delta V_{\text{th}} \rangle} \tag{2}$$

Here, $\langle \Delta V_{\text{th}} \rangle$ and σ^2 are the mean and the variance of the measured distribution, respectively.

To characterize both the BTI and RTN contribution, however, we use a numerical approach here. For this, the PDF of ΔV_{th} is calculated as the convolution of the contributions due to BTI, RTN and noise [10]:

$$\begin{aligned} p(\Delta V_{\text{th}}) = {} & p_{\text{Discharge}}(\Delta V_{\text{th}}|N, \eta) \\ & \times p_{\text{RTN}}(\Delta V_{\text{th}}|N_{RTN}, \eta) \\ & \times p_{\text{Noise}}(\Delta V_{\text{th}}|m, \sigma) \end{aligned} \tag{3}$$

For the defect contributions $p_{\text{Discharge}}$ and p_{RTN}, it is assumed that the number of defects is Poisson distributed throughout the devices, with the mean values N and N_{RTN}. The impact of each individual defect on ΔV_{th} is assumed to be exponentially distributed with mean η. The probability of the sum of k exponential distributions is described by the Gamma distribution (γ). For the BTI defects, which shift the observed ΔV_{th} in one direction only, this results in a sum of Poisson weighted gamma distributions:

$$p_{\text{Discharge}}(\Delta V_{\text{th}}|N, \eta) = \sum_{k=0}^{\infty} \mathcal{P}_N(k)\gamma(k, \Delta V_{\text{th}}/\eta) \tag{4}$$

While for RTN defects, which cause both negative and positive shifts in ΔV_{th}, both contributions have to be accounted for:

$$\begin{aligned} p_{\text{RTN}}(\Delta V_{\text{th}}|N_{\text{RTN}}, \eta) = {} & \sum_{k=0}^{\infty} \mathcal{P}_{N_{\text{RTN}}/2}(k)\gamma(k, \Delta V_{\text{th}}/\eta) \\ & \times \sum_{k=0}^{\infty} \mathcal{P}_{N_{\text{RTN}}/2}(k)\gamma(k, -\Delta V_{\text{th}}/\eta) \end{aligned} \tag{5}$$

Notice that the same parameter η is used for the step height in BTI and RTN, as both are thought to be caused by the same kind of defects [11], [12].

For the measurement noise, a normal distribution with parameters for mean (m) and variance (σ) is used:

$$p_{\text{Noise}}(\Delta V_{\text{th}}|m, \sigma) = \mathcal{N}\left(m, \sigma^2\right) \tag{6}$$

Equation (3) yields the final PDF, which can be integrated to obtain the CDF. Alternatively, one of the terms of the convolution may be integrated prior to convolving. The set of parameters describing the CDF ($\{N, N_{\text{RTN}}, \eta, m, \sigma\}$) can then be numerically optimized to match the CDFs obtained from the ΔV_{th} measurements.

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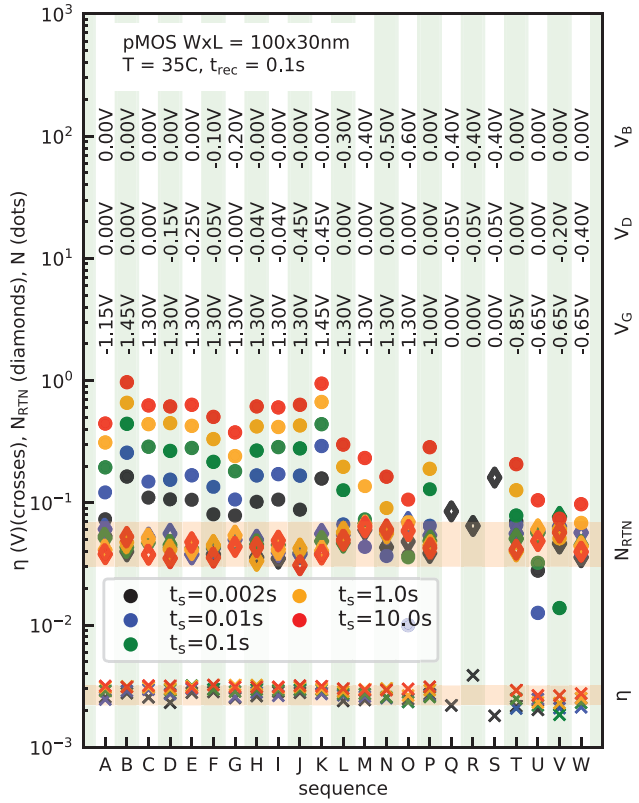

Fig. 6. Parameters extracted at a relaxation time of $t_r = 0.1$ s for all sequences on the short devices. While the number of charged defects (N) varies with the applied stress parameters, the number of RTN active defect (N_{RTN}) stays relatively constant at 4×10^{-2}. The average step height caused by the defects (η) is around 3 mV for all sets. Extraction for measurement sets Q, R, and S was not successful. This is a consequence of the low gate biases applied during these sets, which results in almost negligible degradation.

IV. Results

Extraction results for all sets measured on the short devices are given in Figure 6. The parameters shown are extracted at a relaxation time of $t_r = 100$ ms after stress, the bias parameters are given in the figure. As expected, both the step height, as well as the number of RTN active defects remains constant over all sets. The number of charged BTI defects increases with stress time, gate bias and (negative) body bias.

The importance of characterizing a large number of devices is clearly evident here, as there is on average often less than one active defect per device. This is a consequence of the small gate area of the devices, as well as the relatively short stress times, the low stress biases and moderate temperature the devices were subjected to.

A. Device Degradation

The dependence of the degradation on stress gate bias, stress time and relaxation time is given in Figures 7 and 8. In Figure 7 the extracted number of charged BTI defects is shown in dependence of stress gate bias and stress time, shortly ($t_r = 2$ ms) after stress. As expected, the degradation depends strongly on both stress bias and time.

By performing the extraction at various points in relaxation time, the dependence of the average number of charged defects

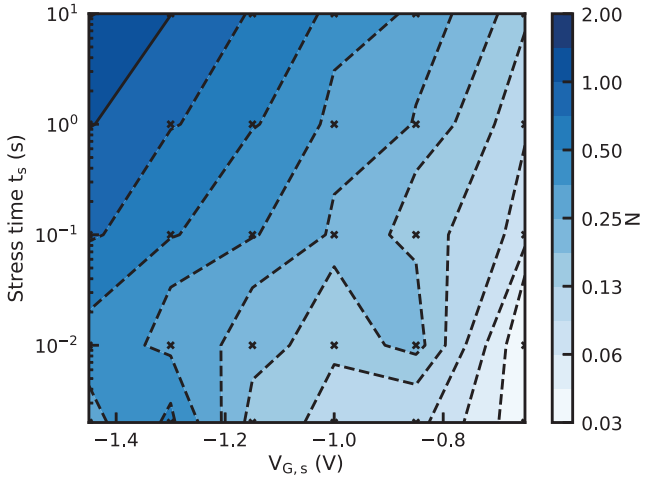

Fig. 7. Gate bias and stress time dependence of the average number of charged BTI defects (N), $t_r = 2$ ms after stress, measured on the short devices. The dashed lines are contour lines while the crosses indicate measurement points.

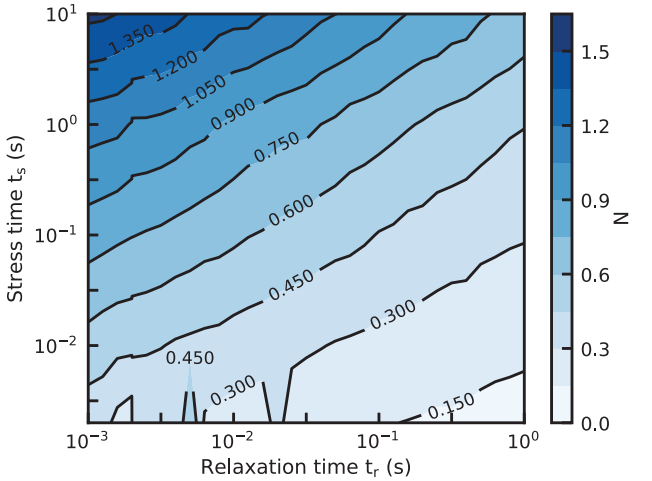

Fig. 8. Extracted average number of captured defects (N) after stress and successive relaxation for a stress bias of -1.45 V, measured on the short devices. Measurement points at t_s= {2, 10, 100, 1000, 10000}ms at various t_r.

over both stress and relaxation time can be extracted, as shown in Figure 8 for the most severe stress case ($V_G = -1.45$ V). At this stress bias, only for very low stress times the defects are able to recover almost completely during the following relaxation period.

B. Simulations

To verify the obtained results, the average values obtained from the measurements were replicated using TCAD simulations. For the simulations, the open-source compact simulator *Comphy* [13] is used. This simulator uses an effective two-state NMP model to calculate charge trapping (see Figure 9). In the model, each defect is modeled by a Markov chain with a neutral and a charged state. Transition rates between the states are calculated from parabolas which represent the potential energy surfaces of the system in the charged and neutral states. Their shape is determined by the ratio of their curvatures R, and a relaxation energy $S\hbar\omega$. Their offset is given by the energy

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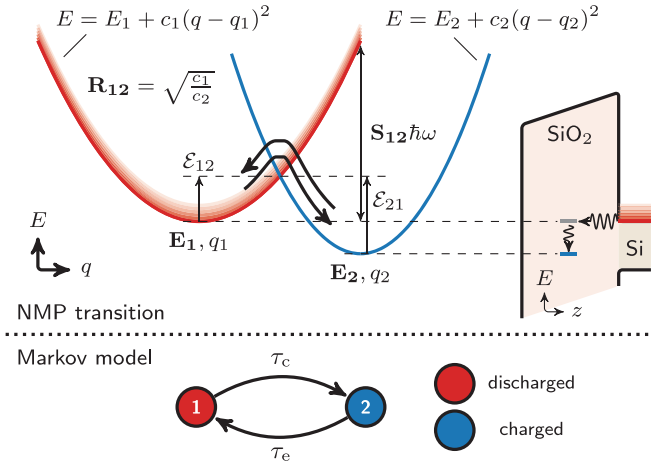

Fig. 9. Two-state NMP model as used for the defect simulations. The defect can exist in a neutral and a charged state. To change states, a carrier has to tunnel through the oxide and the defect has to overcome an energetic barrier. The barrier is calculated in the model by an intersection of two parabolas, which shift in energy with the gate bias.

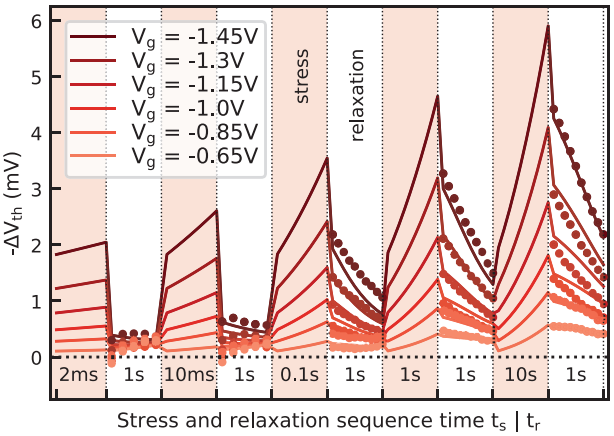

Fig. 10. Measured (dots) and simulated (lines) average degradation for the short devices for all measurements with $V_B = V_D = 0$ V. The simulations are performed using the SiO_2 and HfO_2 defect bands extracted in [13]. The agreement between measurement and simulation is reasonable, although some deviation can be observed after the shortest stress times which might be switching related.

of the reservoir—the channel or the gate—and the energy of the defect. The intersection point of the parabolas gives an energy barrier which has to be overcome thermally. The offset between the parabolas, and in consequence the energy barrier for charge transition, changes with the applied gate bias. In addition, a WKB factor accounts for tunneling between the reservoir and the defect. The simulator places a number of such defects in the oxide, with their parameters and their weights based on the defect bands provided to the simulator. The SiO_2 and HfO_2 defect bands used in this work are from an earlier study on devices of the same technology, but larger in gate area [13]. For each time-step, the simulator calculates the transition rates for each defect, and updates their charge and impact on ΔV_{th} accordingly.

Results showing both the measured degradation averaged over all short devices, as well as the simulated degradation are given in Figure 10. The simulations show good agreement with

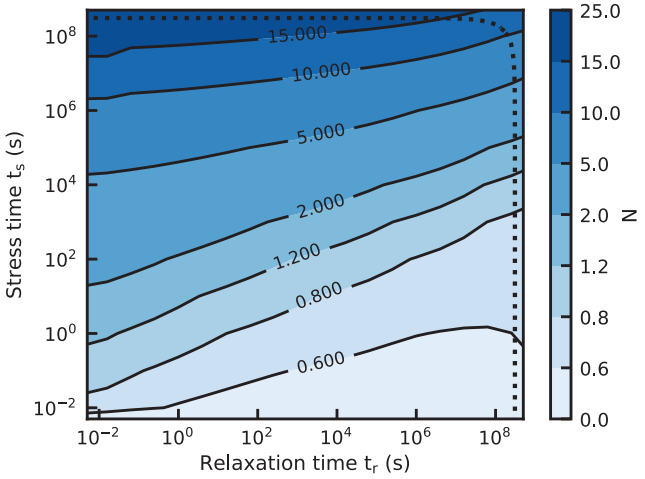

Fig. 11. Simulated average number of charged defects after stress and successive relaxation for a stress bias of −1.45 V for up to 10 years (dotted line). The simulation is performed with the defect data from [13], calibrated to long term measurements performed on large area devices of the same technology.

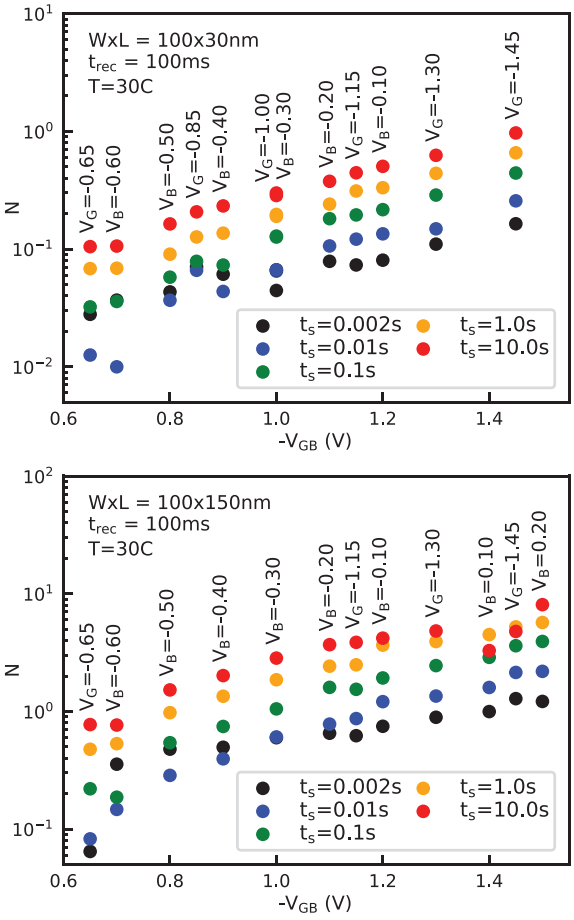

Fig. 12. Average number of charged defects after 0.1 s of relaxation as a function of stress time for different gate-bulk voltages, for both the short and long devices. The points where a gate bias is given were measured at $V_B = 0$ V, the points where a bulk bias is given at $V_G = -1.3$ V. Both sets show a similar trend, indicating that the severity of stress depends only on V_{GB}, regardless whether the stress bias is applied to gate or bulk.

the measured data, with minor deviations in early recovery after the shortest stress times. Using this simulation setup, the expected number of defects charged as a function of stress and

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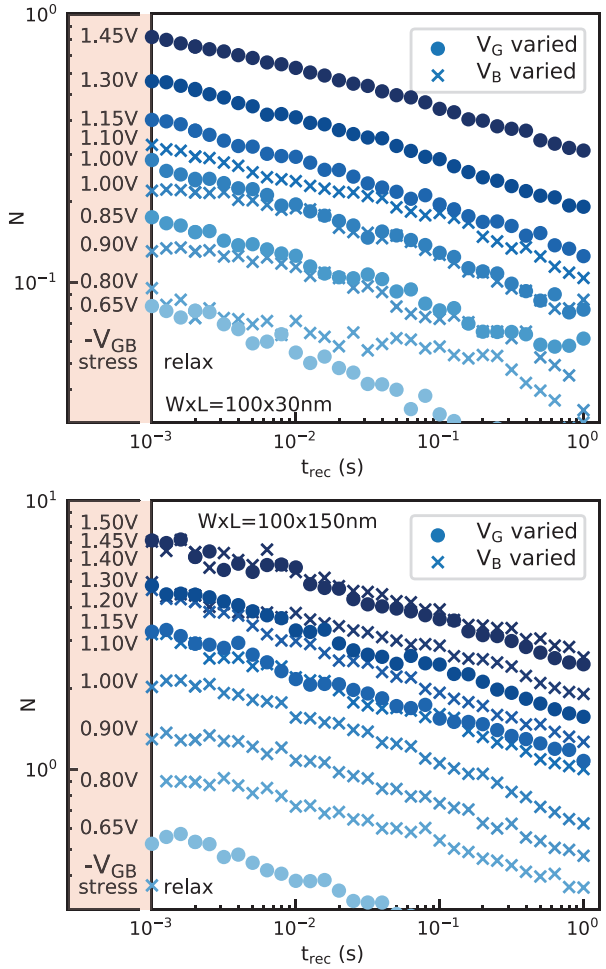

Fig. 13. Relaxation of the average number of charged defects after 0.1 s of stress at varying gate-bulk voltages, for both (top) the short and (bottom) the long devices. The measurements represented by circles are measured at $V_B = 0$ V, while for the measurements represented by crosses, the gate bias $V_G = -1.3$ V is applied and the body bias V_B is varied. Relaxation shows similar behavior independent on which terminal stress was applied, with slight variations at short recovery times. This may be caused by a longer transient behavior when swithcing from stress to recovery due to the larger capacitance of the bulk.

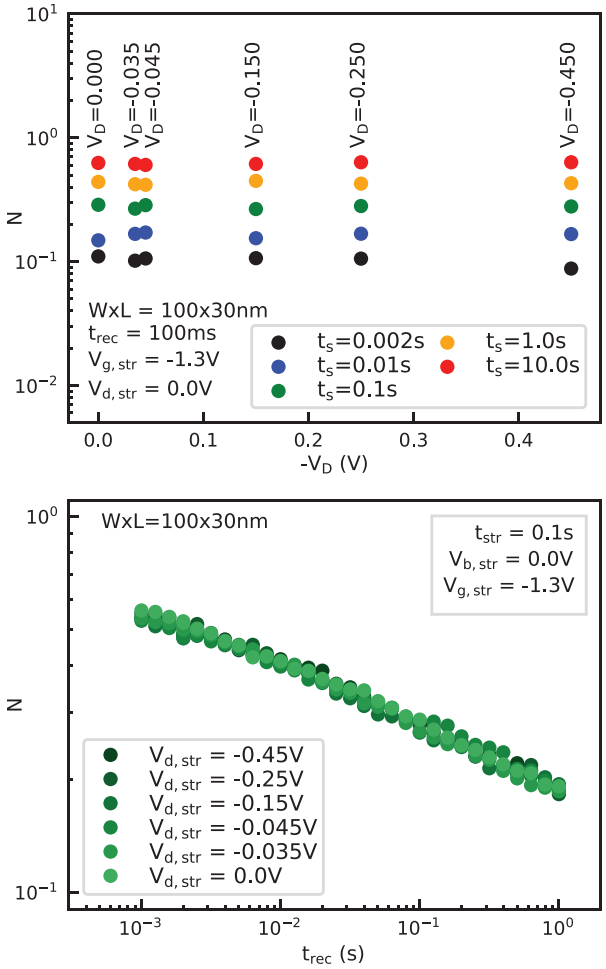

Fig. 14. Average number of charged defects for various drain biases applied during stress for the short devices. (top) Extracted for all stress times after $t_r = 100$ ms of relaxation. (bottom) Extracted during relaxation after $t_s = 100$ ms of stress. The low drain biases applied during stress seem to have no significant impact on the measurements.

relaxation time as plotted for the measurement data in Figure 8 are extrapolated for a ten-year timeframe using simulation data in Figure 11.

C. Bulk Bias Dependence

To investigate the influence of the bulk bias for this technology, a number of measurements are performed at a constant gate bias of $V_G = -1.3$ V while varying the bulk bias. The results are shown in Figures 12 and 13 for the short and long devices, and compared to measurements at $V_B = 0.0$ V. It can be seen in Figure 12 that the number of charged defects in the investigated pMOS transistors increases with increased (negative) gate bias and decreases with increased (negative) bulk bias. Both gate and bulk bias show the same influence on the extracted number of defects charged, which appears to depend only on V_{GB}. Figure 13 reveals that relaxation on the log(N) axis shows a similar slope independent of whether the stress bias is applied to the gate terminal only, or divided between the bulk and gate terminals. This seems counterintuitive at first glance, as charge trapping is dependent on the oxide electric field F_{ox}, which is mainly determined by the gate voltage once the channel is present. The observed dependence on both the gate and bulk bias may be caused by altering of the carrier density or their distribution in the channel by the bulk bias, or by insufficient control of the channel during bulk stress.

A comparison of the geometries shows that the short and long devices exhibit a similar dependence on the applied gate stress bias. While the device area between the two device structures differs by a factor of 5, the number of defects encountered can be observed to scale by a factor of 10 at same values of V_{GB}. A possible explanation for this might be edge effects, which decrease the effective length of the channels and thus lead to a larger ratio of the effective areas of the short and long devices.

In addition to the measurements shown in Figures 12 and 13 for bulk bias dependence, the influence of drain-source stress is evaluated as well. For this, measurement sets are performed with drain stress biases up to $V_D \leq 0.45$ V, which is still well below the hot-carrier regime. The results for the short devices

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are shown in Figure 14. No significant influence is found on the degradation either shortly after stress or during relaxation. This observation seems reasonable, considering the low $V_{DS} \leq 0.35V_{GS}$, and is fully consistent with earlier observations on non-homogenous BTI stress [14].

V. Conclusion

Measurements on dedicated array structures allow for the efficient characterization of defects in thousands of individual nanoscale transistors. Using a defect-centric approach large amounts of measurement data as obtained from such experiments can be processed efficiently to find the statistical behavior of these defects. Measurements taken at varying bias conditions and stress times allow to compare the influence of these parameters on the defects BTI contribution during stress and relaxation phases. Consistent with [15], the BTI behavior in such devices is severely affected by gate and bulk stress, while RTN activity and step height is largely independent on the applied stress parameters. TCAD simulations based on an effective two-state NMP model allow lifetime extrapolation of the extracted degradation. Degradation in the investigated devices is found to depend mainly on the gate-bulk voltage, and is found largely independent of the applied drain bias.

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