Ultra-Low Noise Defect Probing Instrument for Defect Spectroscopy of MOS Transistors

Michael Waltl, *Member, IEEE*

***Abstract*—It is commonly accepted that the performance and time-to-failure of modern semiconductor transistors are seriously affected by single defects located in the insulator or at the insulator/semiconductor interface. The impact of such single defects on the device current ranges from several pico-ampere up to hundreds of nano-ampere and their characterization poses a major challenge for measurement instruments. However, for an accurate description of the device behavior under operation, the understanding of the physical mechanism behind single-charge trapping is inevitable. For this a large variety of defects and devices with different geometries have to be studied. However, the impact of single defects on the device current rapidly decreases with increasing effective gate area. Thus, suitable measurement instruments have to provide a high current measurement resolution at a large signal-to-noise ratio (SNR) for monitoring single charge transitions. To enable defect spectroscopy at a very detailed level an ultra-low noise defect probing instrument (DPI) is invented. The compact implementation and optional usage of a lead battery supply unit for the DPI guarantees highest SNR and also long-term stability over more than two years, which is typically hard to achieve when instruments of different manufacturers are connected. Utilizing the DPI a measurement resolution of a few micro-volts in terms of threshold voltage shift can be achieved, which fairly outweighs the results obtained with general-purpose instruments.**

***Index Terms*—Reliability, transistor, defect spectroscopy, single defects, bias temperature instabilities, 1/f noise, time-dependent defect spectroscopy.**

I. Introduction

SINCE several decades the performance and also the geometry of integrated metal-oxide-semiconductor (MOS) transistors have been continuously improved. This successful development has led to the fact that electronic devices based on the complementary MOS (CMOS) technology have become indispensable in our everyday life. Despite these improvements, however, all MOS transistors suffer from imperfections at the atomic level which can emerge as electrically active sites, so-called defects [1], [2], [3]. These defects are unavoidably introduced during device fabrication and occur at interfaces between materials with different lattice constants, i.e., at the interface between the substrate and the insulator (Si/SiO_2). Especially disadvantageous in MOS transistors is the fact that these defects can become charged and uncharged during device operation at nominal bias conditions and so perturb the surface potential along the conducting channel. This behavior gives rise to *(i)* a drift of threshold voltage ΔV_{th} of the MOS transistors, *(ii)* reduction of the sub-threshold slope, *(iii)* change of the carrier mobility, *(iv)* and also the on-resistance can increase. These observations are in summary commonly referred to as bias temperature instabilities (BTI). However, not only BTI, but also stress induced leakage currents [4], [5] where an increase of the gate current is observed, and hot-carrier-degradation [6], [7] which seriously lowers the channel mobility due to creation of interface defects affect the MOS transistor's performance.

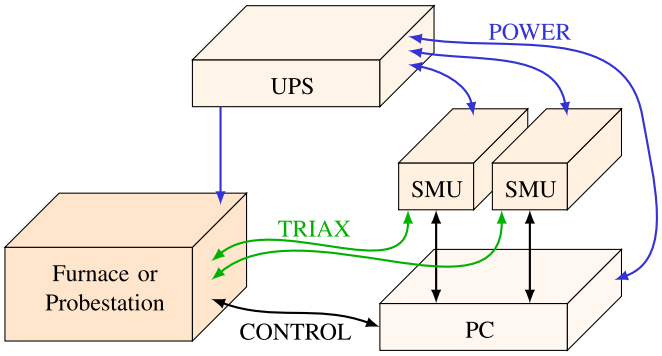


Fig. 1. A schematic showing a typical measurement facility for the *defect spectroscopy*. To contact the devices and to provide a stable temperature, commercial probe stations but also special custom-designed furnaces can be used. The measurements are performed using source-measure-units (SMUs) which are controlled by a personal computer (PC). An online uninterruptible power supply (UPS) is highly recommended, especially to guarantee failure-safe long term measurements, and also to stabilize the frequency of the main power connection, which can improve measurement noise and makes the system more reliable in harsh environments.

A. General Measurement Considerations

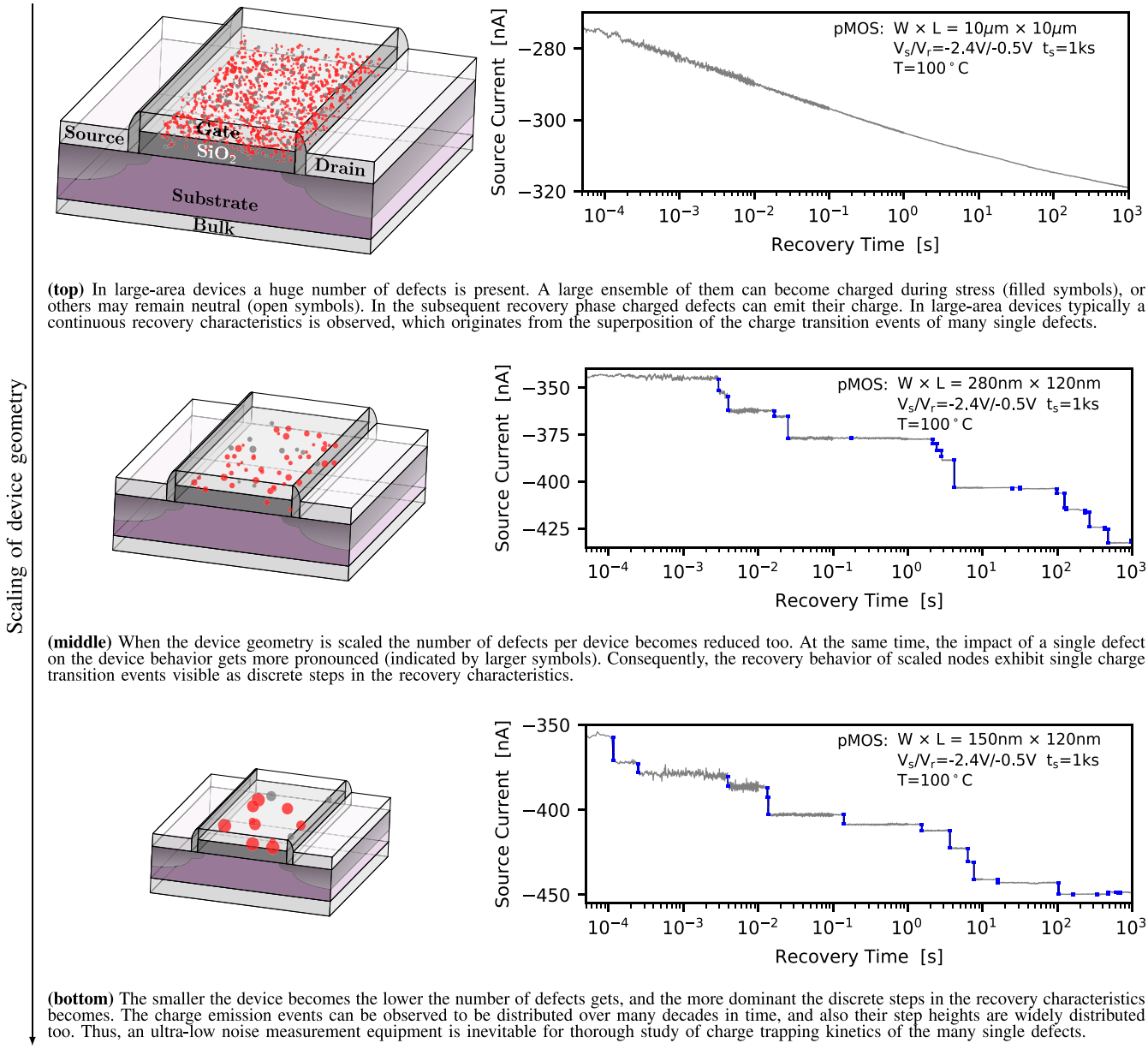
To study the impact of charge trapping on the overall device behavior dedicated semiconductor device test stations, as visible in Figure 1, are used and several measurement techniques are applied for device characterization. In addition to classical $I_D(V_G)$ and $C(V)$ experiments, DCIV [8], [9], [10], measure-stress-measure (MSM) [11], extended MSM [12], [13] and charge pumping [14] measurements have been extensively used in the past. Lots of efforts have also been put into the development of new methods like an on-the-fly technique [15],

Manuscript received January 30, 2020; revised March 18, 2020; accepted April 15, 2020. Date of publication April 20, 2020; date of current version June 5, 2020. This work was supported in part by the Austrian Research Promotion Agency FFG (Take-Off Program) under Project 861022 and Project 867414.

The author is with the Christian Doppler Laboratory for Single-Defect Spectroscopy in Semiconductor Devices, Institute for Microelectronics, TU Wien, 1040 Vienna, Austria (e-mail: waltl@iue.tuwien.ac.at).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TDMR.2020.2988650



(top) In large-area devices a huge number of defects is present. A large ensemble of them can become charged during stress (filled symbols), or others may remain neutral (open symbols). In the subsequent recovery phase charged defects can emit their charge. In large-area devices typically a continuous recovery characteristics is observed, which originates from the superposition of the charge transition events of many single defects.

(middle) When the device geometry is scaled the number of defects per device becomes reduced too. At the same time, the impact of a single defect on the device behavior gets more pronounced (indicated by larger symbols). Consequently, the recovery behavior of scaled nodes exhibit single charge transition events visible as discrete steps in the recovery characteristics.

(bottom) The smaller the device becomes the lower the number of defects gets, and the more dominant the discrete steps in the recovery characteristics becomes. The charge emission events can be observed to be distributed over many decades in time, and also their step heights are widely distributed too. Thus, an ultra-low noise measurement equipment is inevitable for thorough study of charge trapping kinetics of the many single defects.

Fig. 2. When the geometry of MOS transistors becomes reduced towards nanoscale devices the number of active defects is also significantly reduced, but at the same time the impact of a single defect on the device behavior gets more pronounced. This trend and the consequences for the transient recovery behavior after NBTI stress has been applied is shown for pMOS devices with three different geometries, **(top)** W × L = 10μm × 10μm, **(middle)** W × L = 280nm × 120nm and **(bottom)** W × L = 150nm × 120nm. Although nanoscale devices exhibit significantly large discrete steps arising from charge transitions of single defects available highly optimized measurement tools are inevitable to study the wealth of defects determining the device behavior.

an analog gate bias control circuit [16], [17], but also into the development of the time-dependent defect spectroscopy (TDDS) [18], [19]. As the clock frequencies of circuits used in central processing units or in radio frequency applications are in the range of several gigahertz, special attention has been recently put into the development of ultra-fast $I_D(V_G)$ techniques [20] but also high-speed $C(V)$ measurements [21] and the implementation of dedicated ring-oscillator based test structures [22], [23] in order to study the impact of charge trapping down to the nanosecond regime.

In general, as long as well-established measurement sequences are applied, general-purpose instruments (GPIs) [24], [25], [26], [27] can be used. However, to compensate for missing features and circumvent various limitations of commercial setups custom-made solutions mostly extended with GPIs (digital storage oscilloscopes, programmable pulse units, lock-in amplifiers, etc.) are more often used [15], [17], [20], [28], [29], [30], [31], [32].

B. Requirements for Defect Spectroscopy

The requirements for the measurement tools and methods change with ongoing enhancement of MOS transistors, and especially with scaling of the device geometries. While in large-area transistors the cumulative response of many defects can be observed as continuous drift of the device threshold

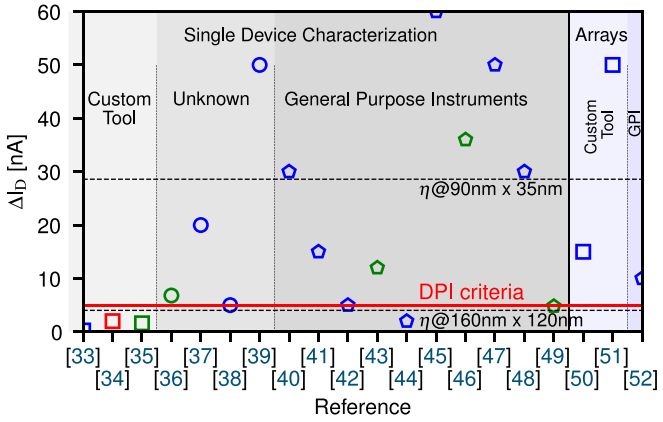


Fig. 3. The limit of the measurement resolution ΔI_D for discrete transitions in the drain current, i.e., single charge capture and emission events, extracted from single defect studies is shown. For the studies single devices, but also dedicated array structures, have been used. To record the current either custom-designed solutions (squares) or general-purpose instruments (GPIs, diamonds) have been used. In the literature either the value for ΔI_D is available directly (blue symbols), or has been converted from a given equivalent threshold voltage shift ΔV_{th} (green symbols), or has been given in terms of $\Delta I_D/I_D$ (red symbols). It has to be mentioned that ΔI_D depends on the current range of the SMU and also on the sampling rate, i.e., signal bandwidth. Thus, a general comparison is difficult, but the trend clearly shows that highest resolutions are obtained from custom-based solutions. Also highlighted is the measurement limit of ΔI_D=5 nA which is a reasonable approximation for the limit of GPIs and is used to benchmark the DPI presented in this work.

voltage ΔV_{th}, discrete steps in the drain current are observed in scaled transistors, which are a consequence of single charge transitions, see Figure 2. Thus, by using nanoscale devices the charge trapping kinetics of individual defects can be studied, which is essential for physical modeling of their bias and temperature dependence. But the characterization of such discrete transitions poses a formidable challenge for the experimental tools in terms of measurement resolution and also measurement noise.

In the recent past several groups investigated charge trapping at the single defect level using nMOS and pMOS devices employing SiO_2, SiON or high-k gate stacks, see Figure 3. For their studies custom-made measurement setups or GPIs have been used. The achievable measurement resolution for discrete transitions in the drain current ΔI_D, as shown in Figure 3, reveals that the highest resolution can be typically achieved when dedicated custom-based solutions are used. It has to be noted that the minimum ΔI_D for a specified measurement series from Figure 3 strongly depends on the overall noise in the drain current, which is determined by the sampling rate and bandwidth of the source-measure-unit (SMU), but also by the trap density of the investigated devices. Furthermore, the mean of the device current determines the required current range of the SMU, and thus also affects the achieved measurement precision of ΔI_D.

As the impact of a certain defect scales inversely with the effective gate area, an ultra-high ΔI_D resolution would enable to characterize single charge trapping for a large variety of device geometries for different technologies. For this purpose, a new defect probing instrument (DPI) is invented and applied for defect spectroscopy in MOS transistors.

II. Defect Characterization in Transistors

The defects prevalent in semiconductor transistors can be generally grouped into interface states and oxide defects, depending whether they are directly at the Si/SiO_2 interface or in the insulator (SiO_2, SiON or high-k). Each of the defects can become repeatedly charged and uncharged during device operation. For the purpose of defect spectroscopy employing MSM sequences defects are deliberately charged during the stress phase, i.e., phase at high gate bias, and can emit their charge during the subsequent recovery phase, when typically a low gate bias is applied. Each of the charge transitions occurring for each of the single defects perturbs the surface potential along the conducting channel, and can so modulate the drain-source current I_{DS} through the device. As large-area devices exhibit high defect densities many of such defects will change their charge state during a single MSM sequence. However, in large-area devices the impact of each single defect on the overall current flux is very low, and thus only the average response of many defects can be measured, as visible in Figure 2 (top). A groundbreaking progress in understanding the intricate behavior of the charge trapping kinetics of each of the defects has been made by investigating random telegraph noise (RTN) [53] and later TDDS [17], [54] employing nanoscale devices. Both methods take advantage of the scaling of MOS structures. With lowering of the device feature size, the impact of a single defect on the device behavior becomes more and more pronounced, see Figure 2 (middle) and (bottom). In such nanoscale devices the single charge transitions are visible as discrete steps in the drain-source current, which can be analyzed. Detailed single defect studies have revealed that the underlying defect physics is anything but trivial, as the defects can show intricate and surprising bias dependencies (switching traps versus fixed traps), can transform from one configuration into another (neutral, stable or meta-stable), and can even be randomly deactivated and reactivated over time [18], [55], [56]. Also the impact of each single defect on the device current is not always the same, but strongly depends on the location of the defect with respect to the conducting channel. As a consequence, the accurate description of the defects' impact on device performance requires physical based trapping models, like the non-radiative multiphonon model [19], in combination with statistical models describing distributions of defects, as for instance the cumulative distribution function (CDF) of step heights [49]

$$\frac{1-\mathrm{CDF}}{\#devices} = \sum\nolimits_i N_{T_i} \exp\left(-\frac{\Delta I_{DS}}{\eta_i}\right) \tag{1}$$

with N_{T_i} the average number of defects producing an average shift η_i of the drain-source current by a single charge transition. To create the complementary CDF the step height of the single charge transitions from Figure 2 (bottom) are expressed either directly in terms of currents shifts, or in terms of by equivalent shifts of the threshold voltage using $I_D(V_G)$ characteristics of pristine devices, see Figure 4 [57], given by $\Delta V_{th} = \Delta I_{DS}/g_m(V_G^r)$ with V_G^r being the recovery bias applied at the gate terminal of the transistor. With regard to the CDF, a very high measurement resolution is important in order to extract the step height distribution as accurately as possible for

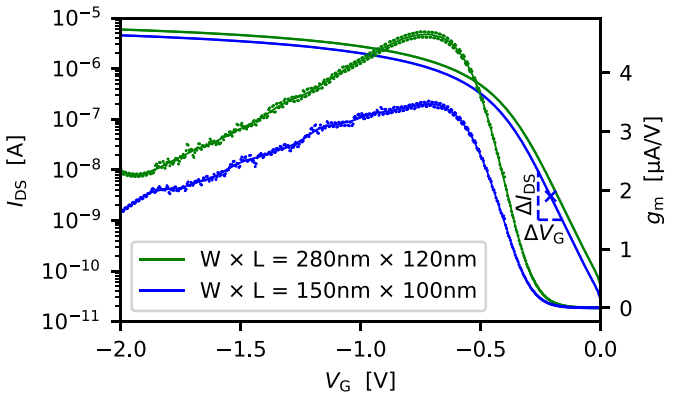


Fig. 4. The drift of the drain current ΔI_D over time is regularly considered as equivalent shift of the threshold voltage ΔV_{th}. To convert the current values into an equivalent threshold voltage ΔV_{th} the $I_D(V_G)$ characteristics of virgin devices is typically used. The transconductance g_m provides the conversion factor between ΔV_{th} and I_{DS}. As g_m is not constant, the obtained values for ΔV_{th} also strongly depend on the applied gate bias during the measurement.

a large variety of technologies. The high measurement resolution is especially relevant for transistors with dimensions of several hundreds of nanometers. Furthermore, due to the fact that the step heights are exponentially distributed, a too coarse measurement resolution would only enable to study a minority of defects in detail, and thus many intricate features of their charge trapping kinetics could not be resolved. However, the latter is essential for verification and development of advanced charge trapping models. To enable single-defect spectroscopy with highest step height resolution at reasonable sampling rates, the *defect probing instrument* (DPI) is proposed, and its concept and features are discussed in the following.

III. Defect Probing Instrument

In order to provide a measurement instrument which enables full controllability of the experimental parameters, that are *(i)* the output voltages and the corresponding switching behavior between different voltage levels as well as *(ii)* different data acquisition schemes for current monitoring and *(iii)* additional control outputs, all at lowest noise levels, the *defect probing instrument* (DPI) has been invented. Initially designed and optimized for single-defect spectroscopy in Si and wide band-gap MOS transistors [58], [59], [60] the DPI also allows characterization of large-area transistors using MSM schemes [58], [61], [62], [63], [64] and $C(V)$ characteristics [65]. Furthermore, the DPI enables automated characterization of array structures [66], and also devices based on 2D materials like MoS_2 [67].

To ensure a high degree of flexibility for constantly evolving requirements, the DPI is based on a modular design concept, see Figure 5. The main configuration of the DPI consists of a three-channel pattern generator unit (PGU) to provide programmable bias signals, one device connector unit (DCU) which converts the device currents into an equivalent voltage, and up to two data acquisition units (DAU) which record the voltage signals provided by the DCU. All units are synchronized employing a backpanel bus system, and can be individually configured via USB connection. It has to be

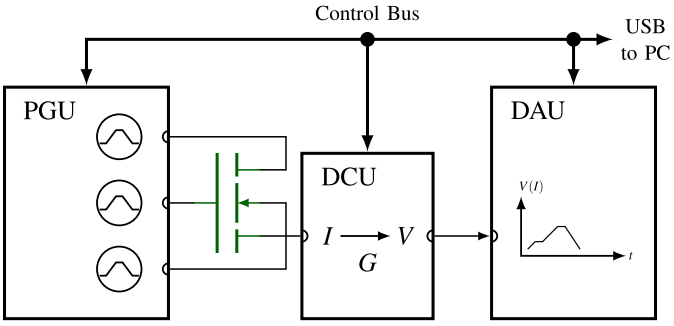


Fig. 5. The defect probing instrument (DPI) is based on a modular design concept and comprises pattern generator units (PGUs) which provide programmable output voltage signals, device connector units (DCUs) which convert the device currents into an equivalent voltage signal and data acquisition units (DAUs) to record voltage signals. All units are synchronized via a shared parallel bus and can be further controlled directly by a measurement host via USB interface.

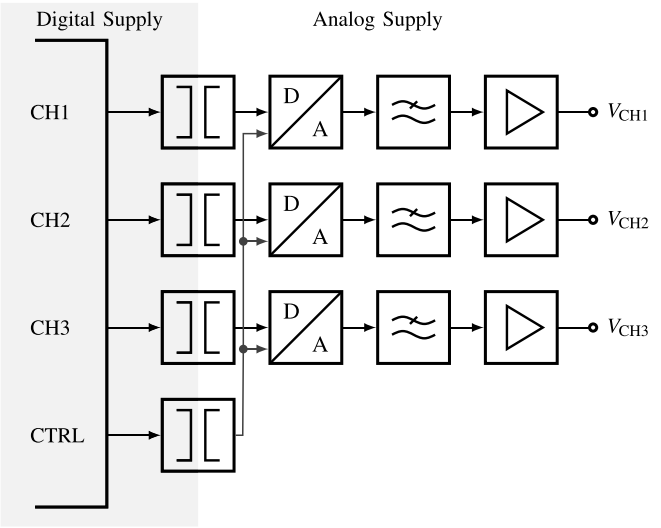


Fig. 6. The schematic of the pattern generator unit (PGU) shows the three parallel digital to analog converter (DAC) stages together with the corresponding output filters and amplifiers. The digital control lines of the processor are decoupled from the analog area. The processor itself is connected to a backbone bus system for data exchange with other modules and synchronization purposes.

mentioned that a major advantage of the selected design concept is that the individual units can be continuously improved independently of each other to further improve the SNR and measurement resolution. Also features like fast $I_D(V_G)$ or fast $C(V)$ methods can be added to the system at reasonable efforts.

A. Pattern Generator Unit

The schematic of the pattern generator unit (PGU) is shown in Figure 6. As indicated in the schematic, a fundamental design strategy for the entire DPI is that the digital and analog components are strictly electrically isolated from each other in order to guarantee lowest noise in the analog signal paths.

The output signals of the PGU are controlled by an ARM processor, which also provides the USB interface for communication with the measurement host. Furthermore, the processor is connected to an internal bus system to exchange control information with other modules and to provide an exactly synchronized timing behavior. When switching between defined

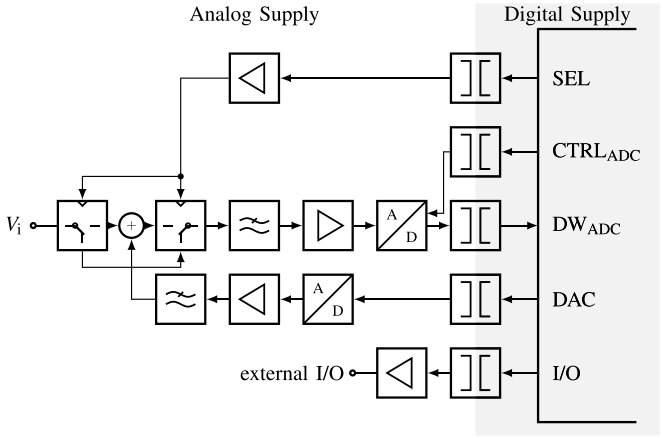


Fig. 7. The analog input signal is passed to the input filter with or without subtraction of a programmable offset voltage. A high precision analog to digital converter stage converts the analog signal to a digital word and is controlled by an electrically decoupled processor. Furthermore, the processor unit provides programmable external digital control lines to control and synchronize operations with external general-purpose instruments. Similar to the PGU, for the communication with the measurement host a USB interface is provided.

voltage levels the output voltage characteristics are of particular interest. On the one hand the switching transient has to be as short as possible, while on the other hand any voltage overshoot has to be avoided, because the steeper the switching transient becomes, the larger the corresponding voltage overshoot might be. To compensate for the detrimental voltage overshoot, several techniques such as pole compensation, gain compensation, lead and lead-lag compensation are typically used in OPAMP circuits [68]. The compensated switching transient of the PGU exhibits a smooth transition between distinct bias levels with a rise time and fall time of $t_r = t_f \approx 200\,]$ns enabling a maximum output frequency of $f_{max} = 1$MHz. To extend the applicability of the defect spectroscopy employing the DPI to wide band-gap technologies like SiC and GaN the output bias range of the PGU can be configured up to $\pm 48\,V$.

B. Data Acquisition Unit

The data acquisition unit (DAU) records an analog input voltage at a high sampling rate of up to $f_{s,max} = 1$MHz with a resolution of $V_{res} \approx 75\mu$V. Before the analog input signal is converted into a digital word it is filtered and pre-amplified, as shown in Figure 7.

Both, the filter and the pre-amplifier stage, are carefully calibrated to the input bandwidth of the analog to digital converter stage in order to guarantee lowest noise and at the same time take advantage of the high sampling frequency. Another important feature of the DAU is the analog voltage level shifter which can be directly applied to the input signal. This significantly extends the measurement range without any loss in accuracy as it allows to shift the mean value of the input signal in order to remain within the bias ranges of the analog to digital converter stage. This is particularly important for single-defect spectroscopy where the currents during recovery phase of the MSM sequences needs to be recorded at highest accuracy over a wide gate bias range.

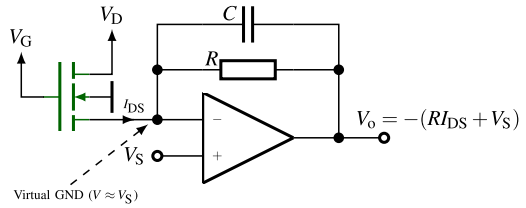


Fig. 8. The schematic of a typical transimpedance amplifier (TIA) circuit is shown with capability to operate as source and measure unit when a bias at V_S is applied.

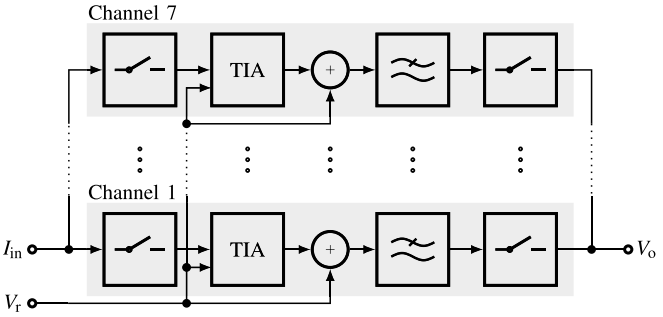


Fig. 9. The current converter unit (CCU) provides seven input current ranges selectable using synchronized switches. Again, the analog and digital components are electrically isolated.

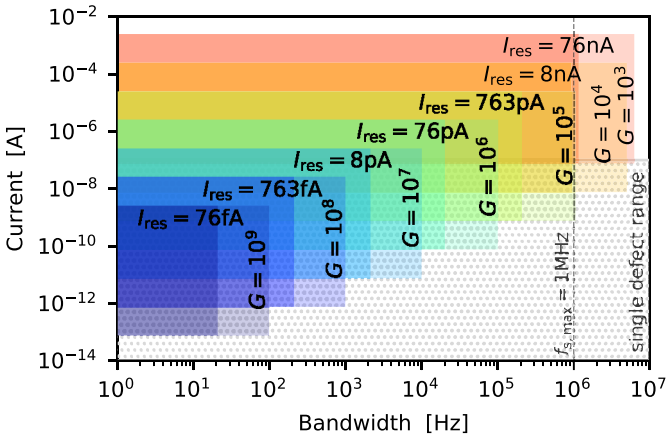


Fig. 10. The current ranges of the current converter unit (CCU) are shown together with the bandwidth of each channel. Towards smaller current resolution the bandwidth of the TIA also decreases. The light areas show the theoretical bandwidth, i.e., 3dB bandwidth, while the dark areas provide the bandwidth when 99.9% of the transient process when a current step function is applied at the input has decayed. Also the typical single defect range for pMOS transistors (W × L = 150nm × 120nm) from Figure 11 is shown.

C. Current Converter Unit

The current converter unit (CCU) is built around the transimpedance amplifier (TIA), as shown in Figure 8. When considering an ideal operational amplifier (OPAMP), i.e., the input bias currents and offset voltage of the OPAMP is neglected, the absolute value of the current through the selected feedback resistor is given by V_o/R. Thus, the OPAMP adjusts its output voltage in order that the current through the feedback loop equals the current through the transistor. A source and measure unit can be obtained when a bias V_S is applied at the positive input of the OPAMP. Due to the virtual ground pin, the same potential is then available at the source

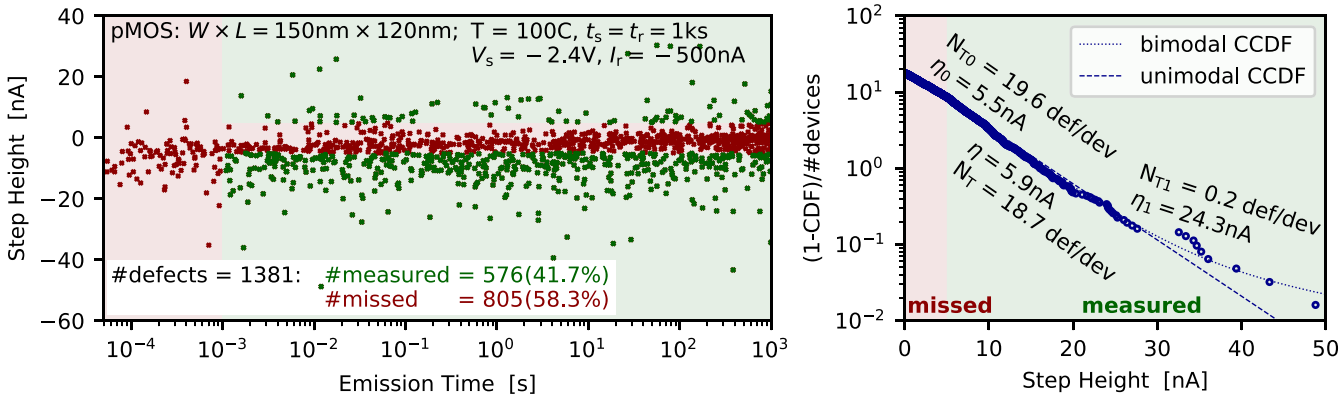


Fig. 11. **(left)** The emission events of 65 pMOS transistors (W × L = 150nm × 120nm) have been extracted from the recovery traces recorded after each device has been stressed for $t_s = 1$ks at $V_G^s = -2.4$V. To account for device-to-device variations of the V_{th} between seemingly identical transistors and to ensure that each device recovers at the same oxide field, the recovery bias is selected according to the constant current criteria, i.e., $V_G^r = V_G(I_{DS} = -500\text{nA})$. The single defect detection limit considered with $\Delta I_{lim} \approx 5$nA at a bandwidth of at least 1kHz is highlighted in red. **(right)** The complementary CDF of step heights follows an exponential characteristics. Using GPIs approximately only around 40% of defects can be measured compared to the presented DPI.

terminal of the transistor. The parallel capacitor placed in the feedback loop determines the bandwidth of the TIA and is used to increase the phase margin of the OPAMP.

As for the defect spectroscopy highest current measurement resolution is required in order to resolve discrete current transitions in the sub-pico-ampere regime the input leakage currents and offset biases of the OPAMP are crucial parameters. To suppress leakage currents at its best OPAMPs with FET inputs are preferably used within the CCU. To cover a large current range several different gains, i.e., feedback resistors, of the TIA are required. Each single gain defines one of the seven single channels of the CCU, see Figure 9, and are selected using mechanical relays. These are preferred to integrated switches as the latter typically exhibit too large leakage currents. Additional hardware components are required to remove the source bias V_S from the output voltage signal of the TIA, before a filter stage limits the signal bandwidth to the maximum sampling frequency of the DAU. The corresponding current ranges and the achieved maximum signal bandwidth is shown in Figure 10.

IV. Results

At the beginning the cumulative CDF of step heights of mid-scaled transistors is measured employing the DPI. Then the charge transitions are extracted from each recovery trace and their distribution is evaluated. As will be demonstrated, the single-defect spectroscopy requires high current measurement resolution at reasonable bandwidth as otherwise only a small fraction of the full distribution of step heights can be measured. An important parameter of high-resolution measurement instruments is the intrinsic noise of the system, which is discussed next for the DPI. Finally the distribution functions of different device geometries are discussed.

A. Extraction of Step Height Distribution Function

The charge transition events extracted from 65 nanoscale pMOS transistors are shown in Figure 11 together with the corresponding CDF. As can be seen the current measurement resolution of the instruments is a crucial parameter as it determines the number of defects which can be accessed during the measurement. The average detection limit for single charge transitions using GPIs from Figure 3 is around $\Delta I_{lim} \approx 5$nA at a sampling rate of at least 1kHz. Considering this limit one can see that approximately two times more defects can be clearly resolved with the new DPI compared to existing instruments. The main drawbacks of the limited measurement resolution are that

(i) In order verify defect models and to improve the accuracy of simulations and device lifetime calculations the charge trapping kinetics of a large number single defects have to be studied.

(ii) Furthermore, the individual defects reveal interesting physical properties which are important for physical modeling which one would otherwise not be able to explore, and

(iii) As the step heights of the defects become smaller with increasing channel area, the defect spectroscopy applied with available instruments is limited to devices with W × L < 200nm × 200nm only.

B. Intrinsic Noise of the Defect Probing Instrument

To analyze the intrinsic noise of the DPI the root-mean-square (RMS) value of the measured current of each channel is evaluated at different sampling rates. Therefore, a reference resistor which equals the value of the gain of the TIA has been connected to the input of the DCU and the bias is provided by the PGU. As can be seen in Figure 12, the measurement resolution gets significantly better with increasing integration time. Thus, a trade-off between signal bandwidth and current resolution has to be found. It has to be noted, that the observed ultra-low intrinsic measurement noise allows to record the data at higher sampling rates, which significantly reduces the overall measurement time. For instance, to record the complementary CDF of step heights from Figure 11 the recovery traces of 65 devices have been recorded for $t_r = 1$ks after each of the devices has been stressed for $t_s = 1$ks. One solution to compensate a possible poor SNR could be to increase the

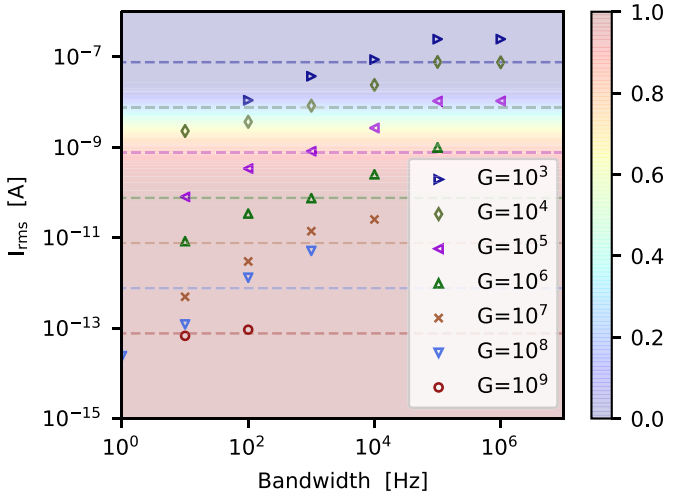


Fig. 12. The high current resolution for the single channels of the DCU is shown at different sampling rates. Each data point is the root-mean-square (RMS) value of the current which has been measured by applying the voltage signal provided by the PGU to a test resistor. The dashed lines provide the resolution of the least significant bit of the ADC of the DAU. As can be seen, with decreasing sampling rate, i.e., increasing integration time, smaller steps can be resolved. In the background the complementary CDF of step heights measured from pMOS transistors (W × L = 150nm × 120nm) from Figure 11 is given.

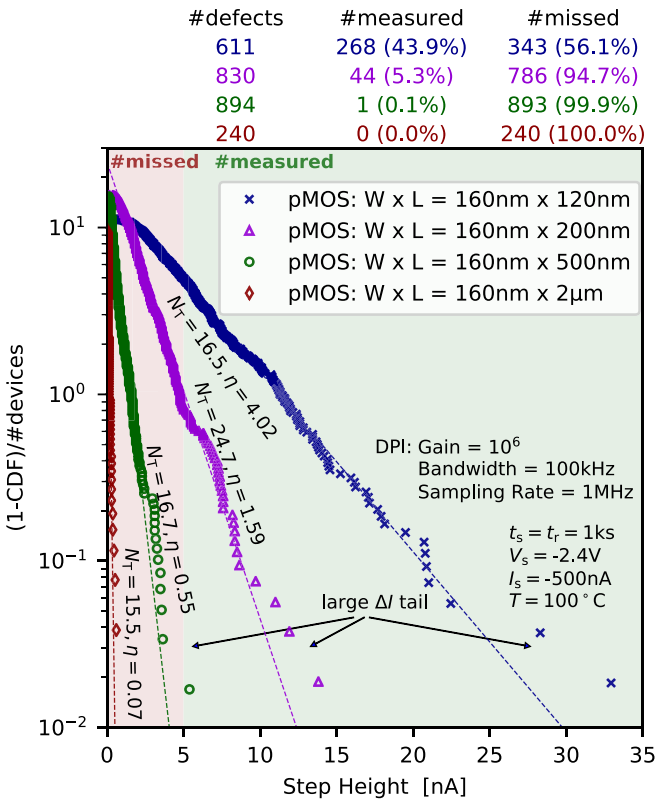


Fig. 13. The cumulative CDF of step heights is shown for pMOS transistors of the same technology but with different geometries. As visible, the distribution functions follow approximately an uniform distribution with a tail at large step heights for each device geometry. The step height resolution achieved with GPIs is highlighted in red. For the smaller geometries the observed step heights cannot be resolved with existing instruments anymore.

gain of the current-to-voltage converter, which would inherently lead to a decrease of the signal bandwidth. In order to record the recovery traces for same number of decades in time at lower bandwidth, the recovery time t_r has to be increased. An increase of the recovery time from t_r = 1ks to t_r = 10ks would lead to a massive increase of the measurement time. In this case the recording of a single complementary CDF would take 65 · 9ks ≈ 7 days longer compared to the previous case. Such an increase of the recovery time would make the TDDS inapplicable as typically 100 stress/recovery sequences have to be recorded to extract a single charge emission point at a given stress/recovery bias and temperature.

The complementary CDF from Figure 11 is also shown in the background Figure 12. As can be seen, for the selected technology the DCU with gain G = 10^6 at a sampling frequency of 100kHz enables to characterize more than 70% of the defects for this kind of pMOS transistor. More accurate measurement resolution is obtained by either reducing the sampling frequency, i.e., increase the integration time for a single data point, or select another channel of the DCU with a larger gain. Alternatively, the DAU provides logarithmic sampling of the input signals. Thus the integration time successively increases during the recording of a single recovery trace. This enables on one hand to measure the fast charge transition events in the microsecond range, but also enables to measure at highest resolution at larger emission times.

C. Single-Defect Spectroscopy of Scaled Transistors

As mentioned before, the understanding of the charge trapping kinetics and the physical influence of single defects on the overall behavior of transistors is essential for accurate performance analysis and time-to-failure predictions. However, the average influence of a single defect on the current flow η decreases very strongly with increasing gate area, see Figure 13. Thus, the characterization of single defects in pMOS devices with a gate area exceeding $A > 8 \times 10^{-2} (\mu m)^2$ is typically very difficult to achieve with existing measurement solutions, as large integration times are required leading to excessively long measurement times. However, the high resolution of the DPI makes it possible to measure single defects up to structures with at least $A > 1.2(\mu)^2$ (≈ 15 times larger gate area) at sampling rates up to 1kHz. Even more outstanding is the improvement in single defect characterization which can be achieved for nMOS transistors. As the nMOS technology exhibits an approximately ten times lower defect density as its pMOS counterparts [69] only a few lucky defects would be accessible with GPIs, as visible in Figure 13. This can inevitably lead to a massive overestimation of the defect distribution when a uni-modal complementary CDF is considered for statistical description. The large deviation between the distribution measured due to limited measurement resolution and the one obtained with the DPI is very large, and thus the step distribution would be approximated too pessimistic. Furthermore, the step distribution measured with the DPI no longer appears as uni-modal distribution, but follows a bi-modal trend. Furthermore, similar to the pMOS cases, the larger nMOS structures can not be analyzed with GPIs on a microscopic single defect level, a serious limitation which can be overcome with the DPI.

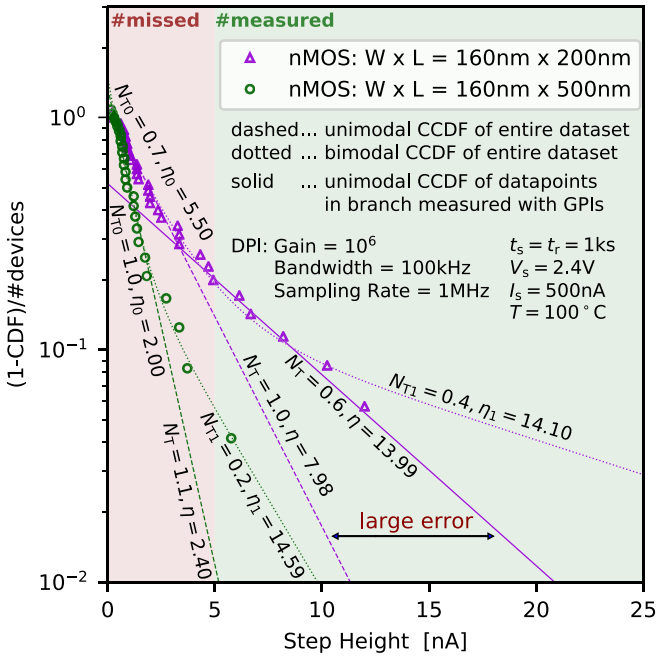


Fig. 14. For nMOS transistors the single-defect spectroscopy becomes more challenging than for pMOS devices. As can be seen from the complementary CDF the number of defects is way smaller compared to the pMOS technology. Thus, a high measurement resolution is inevitable for proper defect characterization. A too coarse step resolution immediately leads to an overestimation of step height distribution. Furthermore, the bi-modal characteristics of the complementary CDF becomes evident with the high resolution provided by the DPI. Also, the larger nMOS transistors could not be studied at the single defect level without the DPI.

V. Conclusion

The characterization of defects in semiconductor devices at high current resolution represents a major challenge for measurement instruments. However, in order to investigate the physical roots and the impact of single defects on the device characteristics in detail, the defect characterization is unavoidable. In this work a newly developed *defect probing instrument* (DPI) is discussed which enables to seize single defects much more exactly than it has been possible with available systems so far. This enables the single-defect spectroscopy also for comparatively large pMOS and nMOS transistors. The new advancement in instrumentation is especially advantageous for correct statistical modeling of defects in semiconductor devices and for further device simulations and performance and lifetime estimations for a large variety of technologies, i.e., Si devices, SiC based high-power devices, but also for future technologies employing 2D materials.

Acknowledgment

This work would not have been possible without the support of A. Grill, B. Stampfer, P.-J. Wagner and T. Grasser (TU Wien), as well as H. Reisinger (Infineon Munich). Furthermore, inspiring discussions with B. Kaczer (imec), G. Pobegen (Infineon Villach), F. Schanovsky, W. Goes, G. Rzepa, B. Ullmann and C. Schleich (TU Wien) are gratefully acknowledged.

References

[1] Y. Miura and Y. Matukura, "Investigation of silicon-silicon dioxide interface using MOS structure," *Jpn. J. Appl. Phys.*, vol. 5, no. 2, p. 180, 1966.

[2] B. E. Deal, "Standardized terminology for oxide charges associated with thermally oxidized silicon," *IEEE Trans. Electron Devices*, vol. 27, no. 3, pp. 606–608, Mar. 1980.

[3] D. M. Fleetwood, "Border traps' in MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 39, no. 2, pp. 269–271, Apr. 1992.

[4] J. Maserjian and N. Zamani, "Behavior of the Si/SiO_2 interface observed by Fowler-Nordheim tunneling," *J. Appl. Phys.*, vol. 53, no. 1, pp. 559–567, 1982.

[5] D. DiMaria and E. Cartier, "Mechanism for stress-induced leakage currents in thin silicon dioxide films," *J. Appl. Phys.*, vol. 78, no. 6, pp. 3883–3894, 1995.

[6] E. Takeda, N. Suzuki, and T. Hagiwara, "Device performance degradation to hot-carrier injection at energies below the Si/SiO_2 energy barrier," in *Proc. Int. Electron Devices Meeting*, vol. 29, 1983, pp. 396–399.

[7] A. Bravaix *et al.*, "Off state incorporation into the 3 energy mode device lifetime modeling for advanced 40nm CMOS node," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2010, pp. 55–64.

[8] A. Neugroschel *et al.*, "Direct-current measurements of oxide and interface traps on oxidized silicon," *IEEE Trans. Electron Devices*, vol. 42, no. 9, pp. 1657–1662, Sep. 1995.

[9] J. Cai and C.-T. Sah, "Monitoring interface traps by DCIV method," *IEEE Electron Device Lett.*, vol. 20, no. 1, pp. 60–63, Jan. 1999.

[10] J. Cai and C.-T. Sah, "Interfacial electronic traps in surface controlled transistors," *IEEE Trans. Electron Devices*, vol. 47, no. 3, pp. 576–583, Mar. 2000.

[11] M. Ershov *et al.*, "Transient effects and characterization methodology of negative bias temperature instability in pMOS transistors," in *Proc. 41st Annu. IEEE Int. Rel. Phys. Symp.*, 2003, pp. 606–607.

[12] B. Kaczer *et al.*, "Ubiquitous relaxation in BTI stressing—New evaluation and insights," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2008, pp. 20–27.

[13] B. Kaczer *et al.*, "NBTI from the perspective of defect states with widely distributed time scales," *Proc. IEEE Int. Rel. Phys. Symp.*, 2009, pp. 55–60.

[14] P. Heremans, J. Witters, G. Groeseneken, and H. E. Maes, "Analysis of the charge pumping technique and its application for the evaluation of MOSFET degradation," *IEEE Trans. Electron Devices*, vol. 36, no. 7, pp. 1318–1335, Jul. 1989.

[15] M. Denais *et al.*, "On-the-fly characterization of NBTI in ultra-thin gate oxide pMOSFET's," in *IEEE Int. Electron Devices Meeting (IEDM) Tech. Dig.*, Dec. 2004, pp. 109–112.

[16] H. Reisinger, O. Blank, W. Heinrigs, A. Muhlhoff, W. Gustin, and C. Schlunder, "Analysis of NBTI degradation- and recovery-behavior based on ultra fast VT-measurements," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2006, pp. 448–453.

[17] H. Reisinger, U. Brunner, W. Heinrigs, W. Gustin, and C. Schlunder, "A comparison of fast methods for measuring NBTI degradation," *IEEE Trans. Device Mater. Rel.*, vol. 7, no. 4, pp. 531–539, Dec. 2007.

[18] T. Grasser, H. Reisinger, P.-J. Wagner, W. Goes, F. Schanovsky, and B. Kaczer, "The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability," in *Proc. IEEE Int. Rel. Phys. Symp.*, May 2010, pp. 16–25.

[19] T. Grasser, "Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities," *Microelectron. Rel.*, vol. 52, no. 1, pp. 39–70, 2012.

[20] Z. Ji, J. F. Zhang, and W. Zhang, "A new mobility extraction technique based on simultaneous ultrafast I_d-V_g and C_{cg}-V_g measurements in MOSFETs," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1906–1914, Jul. 2012.

[21] R. W. Herfst, P. G. Steeneken, M. P. J. Tiggelman, J. Stulemeijer, and J. Schmitz, "Fast RF-CV characterization through high-speed 1-port S-parameter measurements," in *Proc. Int. Conf. Microelectron. Test Struct. (ICMTS)*, 2010, pp. 170–173.

[22] J.-J. Kim *et al.*, "Reliability monitoring ring oscillator structures for isolated/combined NBTI and PBTI measurement in high-k metal gate technologies," in *Proc. Int. Rel. Phys. Symp.*, 2011, pp. 1–4.

[23] A. Kerber, S. Cimino, F. Guarin, and T. Nigam, "Assessing device reliability margin in scaled CMOS technologies using ring oscillator circuits," in *Proc. IEEE Electron Devices Technol. Manuf. Conf. (EDTM)*, 2017, pp. 28–30.

[24] *B1530A (B1500A-A30, B1500AU-030) Waveform Generator/Fast Measurement Unit (WGFMU)*, Keysight Technologies, Santa Rosa, CA, USA, 2019.

[25] *Keithley 4200A-SCS Parameter Analyzer*, Keithley Instruments, Cleveland, OH, USA, 2019.

[26] *Source-Measure-Unit 2636A/B*, Keithley Instruments, Cleveland, OH, USA, 2007.

[27] *HF2LI Lock-In Amplifier With HF2TA Current Amplifier*, Zurich Instruments, Zürich, Switzerland, 2019.

[28] A. Kerber and M. Kerber, "Fast wafer level data acquisition for reliability characterization of sub-100 nm CMOS technologies," in *Proc. IEEE Int. Integr. Rel. Workshop Final Rep.*, Oct. 2004, pp. 41–45.

[29] E. N. Kumar *et al.*, "Material dependence of NBTI physical mechanism in silicon oxynitride (SiON) p-MOSFETs: A comprehensive study by ultra-fast on-the-fly (UF-OTF) IDLIN technique," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2007, pp. 809–812.

[30] J. F. Zhang, Z. Ji, M. H. Chang, B. Kaczer, and G. Groeseneken, "Real Vth instability of pMOSFETs under practical operation conditions," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2007, pp. 817–820.

[31] G. A. Du, D. S. Ang, Z. Q. Teo, and Y. Z. Hu, "Ultrafast measurement on NBTI," *IEEE Electron Device Lett.*, vol. 30, no. 3, pp. 275–277, Mar. 2009.

[32] D. S. Ang, Z. Q. Teo, T. J. J. Ho, and C. M. Ng, "Reassessing the mechanisms of negative-bias temperature instability by repetitive stress/relaxation experiments," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 1, pp. 19–34, Mar. 2011.

[33] Z. Shi, J.-P. Mieville, and M. Dutoit, "Random telegraph signals in deep submicron n-MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, no. 7, pp. 1161–1168, Jul. 1994, doi: 10.1109/16.293343.

[34] J. P. Campbell *et al.*, "Random telegraph noise in highly scaled nMOSFETs," in *Proc. Int. Rel. Phys. Symp. (IRPS)*, 2009, pp. 382–388, doi: 10.1109/IRPS.2009.5173283.

[35] H. Reisinger, T. Grasser, W. Gustin, and C. Schlunder, "The statistical analysis of individual defects constituting NBTI and its implications for modeling DC- and AC-stress," in *Proc. Int. Rel. Phys. Symp. (IRPS)*, 2010, pp. 7–15, doi: 10.1109/IRPS.2010.5488858.

[36] K. Abe, A. Teramoto, S. Sugawa, and T. Ohmi, "Understanding of traps causing random telegraph noise based on experimentally extracted time constants and amplitude," in *Proc. Int. Rel. Phys. Symp. (IRPS)*, 2011, pp. 1–6, doi: 10.1109/IRPS.2011.5784503.

[37] H. Miki *et al.*, "Statistical measurement of random telegraph noise and its impact in scaled-down high-k/metalgate MOSFETs," in *Proc. Int. Electron Devices Meeting (IEDM)*, 2012, pp. 1–4, doi: 10.1109/IEDM.2012.6479071.

[38] D. Veksler *et al.*, "Random telegraph noise (RTN) in scaled RRAM devices," in *Proc. Int. Rel. Phys. Symp. (IRPS)*, 2013, pp. 1–4, doi: 10.1109/IRPS.2013.6532101.

[39] N. Ayala, J. Martin-Martinez, R. Rodriguez, M. Nafria, and X. Aymerich, "Unified characterization of RTN and BTI for circuit performance and variability simulation," in *Proc. Eur. Solid-State Device Res. Conf. (ESSDERC)*, 2012, pp. 266–269, doi: 10.1109/ESSDERC.2012.6343384.

[40] R. Wang, S. Guo, Z. Zhang, J. Zou, D. Mao, and R. Huang, "Complex random telegraph noise (RTN): What do we understand?" in *Proc. Int. Symp. Phys. Failure Anal. Integr. Circuits*, 2018, pp. 1–7, doi: 10.1109/IPFA.2018.8452514.

[41] P. Saraza-Canflanca *et al.*, "A detailed study of the gate/drain voltage dependence of RTN in bulk pMOS transistors," *Microelectron. Eng.*, vol. 215, Jul. 2019, Art. no. 111004, doi: 10.1016/j.mee.2019.111004.

[42] G. Pedreira *et al.*, "A new time efficient methodology for the massive characterization of RTN in CMOS devices," in *Proc. Int. Rel. Phys. Symp. (IRPS)*, 2019, pp. 1–5, doi: 10.1109/IRPS.2019.8720582.

[43] M. Simicic, P. Weckx, B. Parvais, P. Roussel, B. Kaczer, and G. Gielen, "Understanding the impact of time-dependent random variability on analog ICs: From single transistor measurements to circuit simulations," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 3, pp. 601–610, Mar. 2019, doi: 10.1109/TVLSI.2018.2878841.

[44] Y. F. Lim *et al.*, "Random telegraph signal noise in gate-all-around Si-FinFET with ultranarrow body," *IEEE Electron Device Lett.*, vol. 27, no. 9, pp. 765–768, Sep. 2006, doi: 10.1109/LED.2006.880640.

[45] T. Nagumo, K. Takeuchi, S. Yokogawa, K. Imai, and Y. Hayashi, "New analysis methods for comprehensive understanding of random telegraph noise," in *Proc. Int. Electron Devices Meeting (IEDM)*, 2009, pp. 1–4, doi: 10.1109/IEDM.2009.5424230.

[46] N. Tega *et al.*, "Increasing threshold voltage variation due to random telegraph noise in FETs as gate lengths scale to 20 nm," in *Proc. IEEE Symp. VLSI Technol.*, 2009, pp. 50–51.

[47] X. Zhan *et al.*, "A dual-point technique for the entire I_D-V_G characterization into subthreshold region under random telegraph noise condition," *IEEE Electron Device Lett.*, vol. 40, no. 5, pp. 674–677, May 2019, doi: 10.1109/LED.2019.2903516.

[48] L. V. Brandt, B. K. Esfeh, V. Kilchytska, and D. Flandre, "Robust methodology for low-frequency noise power analyses in advanced MOS transistors," in *Proc. Int. EUROSOI Workshop Int. Conf. Ultimate Integr. Silicon (EUROSOI-ULIS)*, 2019, pp. 1–4.

[49] M. Toledano-Luque *et al.*, "Temperature and voltage dependences of the capture and emission times of individual traps in high-k dielectrics," *Microelectron. Eng.*, vol. 88, no. 7, pp. 1243–1246, Jul. 2011.

[50] S. Realov and K. L. Shepard, "Random telegraph noise in 45-nm CMOS: Analysis using an on-chip test and measurement system," in *Proc. Int. Electron Devices Meeting (IEDM)*, 2010, pp. 1–4, doi: 10.1109/IEDM.2010.5703436.

[51] S. Realov and K. L. Shepard, "Analysis of random telegraph noise in 45-nm CMOS using on-chip characterization system," *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1716–1722, May 2013, doi: 10.1109/TED.2013.2254118.

[52] P. Saraza-Canflanca *et al.*, "Automated massive RTN characterization using a transistor array chip," in *Proc. Int. Conf. Synth. Model. Anal. Simulat. Methods Appl. Circuit Design (SMACD)*, 2018, pp. 29–32, doi: 10.1109/SMACD.2018.8434914.

[53] K. S. Ralls *et al.*, "Discrete resistance switching in submicrometer silicon inversion layers: Individual interface traps and low-frequency ($\frac{1}{f}$?) noise," vol. 52, pp. 228–231, Jan. 1984. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRevLett.52.228

[54] T. Grasser, H. Reisinger, P.-J. Wagner, and B. Kaczer, "Time-dependent defect spectroscopy for the characterization of border traps in metal-oxide-semiconductor transistors," *Phys. Rev. B, Condens. Matter*, vol. 82, no. 24, 2010, Art. no. 245318.

[55] Y. Wimmer, A.-M. El-Sayed, W. Gös, T. Grasser, and A. L. Shluger, "Role of hydrogen in volatile behaviour of defects in SiO_2-based electronic devices," *Proc. Roy. Soc. A, Math. Phys. Eng. Sci.*, vol. 472, no. 2190, pp. 1–23, 2016.

[56] T. Grasser *et al.*, "Hydrogen-related volatile defects as the possible cause for the recoverable component of NBTI," in *Proc. IEEE Int. Electron Devices Meeting*, 2013, pp. 1–4.

[57] B. Ullmann *et al.*, "Impact of mixed negative bias temperature instability and hot carrier stress on MOSFET characteristics—Part I: Experimental," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 232–240, Jan. 2019.

[58] M. Waltl *et al.*, "Superior NBTI in high-*k* SiGe transistors-part I: Experimental," *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2092–2098, May 2017.

[59] A. Grill *et al.*, "Characterization and modeling of single defects in GaN/AlGaN Fin-MIS-HEMTs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2017, pp. 1–5.

[60] B. Ullmann *et al.*, "The impact of mixed negative bias temperature instability and hot carrier stress on single oxide defects," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2017, pp. 1–6.

[61] G. Rzepa *et al.*, "Efficient physical defect model applied to PBTI in high-k stacks," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2017, pp. 1–6.

[62] A. Grill *et al.*, "Electrostatic coupling and identification of single-defects in GaN/AlGaN Fin-MIS-HEMTs," *Solid-State Electron.*, vol. 156, pp. 41–47, Jun. 2019.

[63] G. Rzepa *et al.*, "Complete extraction of defect bands responsible for instabilities in n and pFinFETs," in *Proc. IEEE Symp. VLSI Technol.*, 2016, pp. 1–2.

[64] C. Schleich *et al.*, "Physical modeling of bias temperature instabilities in SiC MOSFETs," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2019, pp. 20.5.1–20.5.4.

[65] T. Grasser *et al.*, "Characterization and physical modeling of the temporal evolution of near-interfacial states resulting from NBTI/PBTI stress in nMOS/pMOS transistors," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2018, pp. 1–10.

[66] B. Stampfer *et al.*, "Statistical characterization of BTI and RTN using integrated pMOS arrays," in *Proc. IEEE Int. Integr. Rel. Workshop (IIRW)*, 2019, pp. 1–5.

[67] B. Stampfer *et al.*, "Characterization of single defects in ultrascaled MoS_2 field-effect transistors," *ACS Nano*, vol. 12, no. 6, pp. 5368–5375, 2018.

[68] R. Mancini and B. Carter, *Op Amps For Everyone*. Dallas, TX, USA: Texas Instruments, 2002.

[69] M. Waltl, W. Goes, K. Rott, H. Reisinger, and T. Grasser, "A single-trap study of PBTI in SiON nMOS transistors: Similarities and differences to the NBTI/pMOS case," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2014, pp. 1–5.