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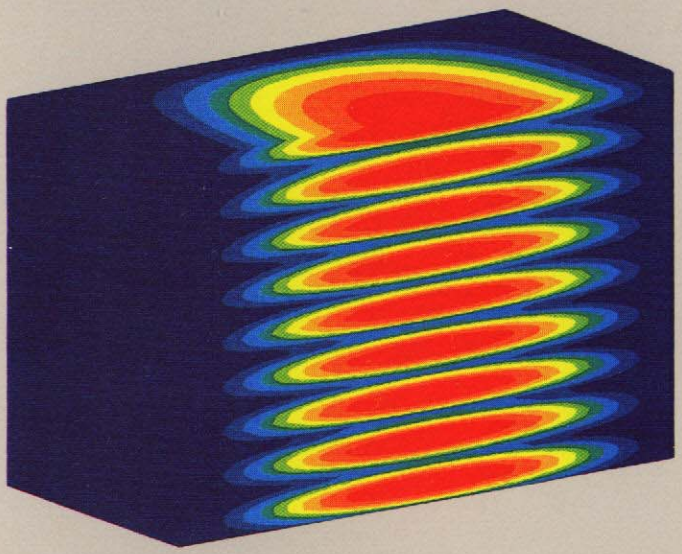

Annual Review
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Preface

Siegfried Selberherr

This brochure is the eighth annual research review of the Institute for Microelectronics. The staff financed by the Austrian Ministry of Science, Transportation and Arts consists of nine full time employees: the head of the institute, five scientists, a secretary and two technical assistants. However, due to the 'Sparpaket', an initiative of the Austrian government to consolidate the budget of our country, only three scientists are presently funded, much to our regret and frustration. Twenty additional scientists are funded through scientific projects supported by our industrial partners.

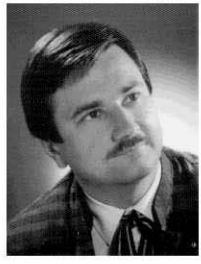
This year we can report participation in a new ESPRIT project directly funded by the European Union, namely ADEQUAT+[1]. The 'Christian Doppler Forschungsgesellschaft' set up the 'Christian Doppler Laboratorium für Integrierte Bauelemente' at our institute, which serves as a considerable source of funding for industrially relevant research. We are also glad to report that all our industrial partners from last year's review have continued to support our institute.

The projects of the institute are, in a continuation of our previous work, focused on microelectronics modeling issues. We are quite satisfied with our academic and scientific output. Particularly pleasing is the number of contributions and participations in international conferences. We are looking forward to a successful next year!

[1] Advanced Developments for CMOS for $0.25\mu m$ and below

Siegfried Selberherr was born in Klosterneuburg, Austria, in 1955. He received the degree of 'Diplomingenieur' in electrical engineering and the doctoral degree in technical sciences from the Technical University of Vienna in 1978 and 1981, respectively. Since that time he has been with the Technical University of Vienna as professor. Dr. Selberherr has been holding the 'venia docendi' on 'Computer-Aided Design' since 1984. He has been the head of the 'Institut für Mikroelektronik' since 1988. His current topics are modeling and simulation of problems for microelectronics engineering.

Renate Winkler was born in Vienna, Austria, in 1960. She joined the 'Institut für Mikroelektronik' in November 1993. Since that time she has been in charge of the organizational and administrative work of the institute.



Ewald Haslinger was born in Vienna, Austria, in 1959. He joined the 'Institut für Mikroelektronik' in December 1991. Since that time he has been in charge of the organizational, administrative and technical work of the institute.

Manfred Katterbauer was born in Schwarzach St.Veit, Austria, in 1965. He joined the 'Institut für Mikroelektronik' in February 1995. Since that time he has been in charge of all technical hardware and software work of the institute.

Monte Carlo Simulation of Silicon Amorphization during Ion Implantation

Walter Bohmayr

When a sufficiently high dose of energetic ions is implanted into a silicon crystal, irradiated zones of the crystal are transformed into an amorphous state. The thickness and spatial location of the amorphous layers determine the type of the secondary defects and the number of point defects remaining in the silicon crystal after a recrystallization step. Primary and secondary defects exhibit a totally different annealing behavior, and sophisticated characterization techniques are required because point defect diffusion from the S/D region of a MOSFET to the area under the gate is a possible source of the inverse short channel effect. Furthermore, amorphous regions are easier to re-grow into damage-free films ("epitaxial recrystallization").

As a first step towards a simulation of these important phenomena we present an accurate multi-dimensional model to predict the range of amorphous layers within ion implanted single-crystal silicon. The critical parameters ruling the amorphization process are the implantation dose, the ion mass, the ion energy, and the substrate temperature T which are all taken into account by our simulation method. The approach is based on a critical damage energy model which assumes that the transformation into the amorphous state happens when the accumulated damage energy generated by ion beams exceeds a critical threshold E_C. The main problem is that E_C is a function of T, ion energy and spatial location. Only at very low temperatures ($T \leq 82$K) one can assume that almost no mi-

gration of point defects occurs and hence E_C is constant. Our task was to develop an amorphization model which predicts the remaining stable damage as a function of T. The fundamental idea of our approach is the assumption that temperature dependent parameters are local functions of the deposited damage energy density E_D. In fact, E_D is a measure for the cascade density and areas with a lower density are assumed to anneal easier at a certain temperature compared to regions damaged more strongly. Therefore, we use an analytical out-diffusion model to determine the temperature dependence and we apply power laws of E_D to model the depth dependence.

Combining these equations we get E_C as a function of depth at a certain temperature and hence it follows that we can also determine the necessary implantation dose to obtain amorphization at a given point and substrate temperature. Our simulation results are in very good agreement with the experimental data and almost no additional CPU time is required.

Walter Bohmayr was born in Steyr, Austria, in 1969. He studied electrical engineering and computer science at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in Industrial Electronics and Control Theory in 1993. During his studies, he was employed with 'Austrian Industries' as a software engineer. He joined the 'Institut für Mikroelektronik' in November 1993, where he is currently working for his doctoral degree. His work is focused on physical and mathematical models and algorithms for three-dimensional process simulation in integrated circuit fabrication. In 1995, the SUSTAIN Coordination Board agreed with awarding him the SUSTAIN fellowship at 'Fraunhofer Institut für Integrierte Schaltungen-Bauelementetechnologie', Erlangen, and he held a visiting research position at SONY, Atsugi, Japan. Part of his work was carried out within the JESSI project PROMPT.

Aspects of Three-Dimensional Mesh Generation

Peter Fleischmann

With the growing importance of three-dimensional simulation, mesh generation has become a critical factor. The amount of data in three dimensions requires efficient and more sophisticated algorithms and data structures. Meshing algorithms which have worked well for two dimensions are often not feasible for higher dimensions. Also, the increasing topographical complexity of the devices and simulation domain poses a greater challenge for automatic meshing schemes. During the development of a fully unstructured Delaunay algorithm suitable for such demands of three-dimensional mesh generation we have experienced various important aspects. One can distinguish the following basic tasks which a more universal three-dimensional mesh generator has to carry out:

- Surface modeling involves all necessary steps to process the given input geometry and to incorporate the given surface into the grid.
- Volume decomposition describes the tesselation of the simulation domain into a set of grid elements such as tetrahedra or hexaedral elements.
- Grid adaptation includes coarsening, refining or generally regridding issues to improve the discretization of the simulated quantities. The accuracy of a first approximative simulation run can be increased, or the grid can be adapted in transient simulations.

Among the more important aspects of the first task is the degree of automation in which the mesh generator deals with the input geometry. Can the algorithm automatically and rigorously process any complex surface with entirely no human interaction? Such a capability plays a critical role especially in Technology Computer-Aided Design (TCAD) where the topography of the geometry itself is subject to simulation. Another issue of surface modeling is special surface triangulation. Our research focuses on Delaunay surface triangulation for the purpose of generating Delaunay meshes which are necessary for the commonly used Box Integration method.

Concerning volume decomposition one of the major issues is the balance between the number, the size, and the quality of the elements. The number should be minimized while the size should satisfy local grid density criteria. Rapid changes of the element sizes throughout the domain avoid too coarse or too fine elements in some areas. At the same time a minimum element quality has to be maintained. Our research includes the insertion of Steiner points to improve the element quality and to avoid typical Delaunay slivers. A fully unstructured meshing algorithm is under development which allows arbitrary changes of the grid densities throughout the simulation domain.

Peter Fleischmann was born in Kabul, Afghanistan, in 1969. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in December 1994. He is currently working for his doctoral degree. His research interests include mesh generation as well as algorithms and data structures in computational geometry.

Mixed-Mode Simulation with MINIMOS-NT

Tibor Grasser

The development of semiconductor devices tends towards a further reduction of device geometry to allow a higher packing density and thus resulting in lower prices. For devices ranging in the submicron region conventional compact models as supported by SPICE loose their validity under certain biasing conditions. Simulation of circuits containing such devices requires a different approach to achieve good accuracy. Due to its object-oriented equation management the simulator MINIMOS-NT is well suited for the extensions required for handling mixed mode simulation. The equations describing the circuit behavior are added to the matrix assembled by the device simulator, resulting in one complete linear system to be solved.

To manage the enormous amount of data associated with device simulation, several libraries have been implemented to simplify the programmers work with basic data structures. One of the modules developed to meet the demands of MINIMOS-NT is the geometry attribute support (GAS) library. This library provides a set of functions for handling attributes which are defined on two-dimensional geometries. For most of the attributes meaningful default values are defined in the VISTA material-database. These default values can be accessed by defining a material type attribute for each segment. To allow for greater flexibility, especially concerning the demands for mixed-mode simulation, a name can be

selected for each segment. This segment name is added to the basic data structure managed by the GAS-library and can be used as a reference to its belonging segment instead of the hitherto used segment index. This feature is essential for the development of an user-interface. It allows the grouping of devices containing the same standardized segment names, e.g., *drain*, *source*, *gate*, *insulator*, and *semiconductor* in the case of FETs.

In the design of the user-interface (input deck) special attention has been payed to flexibility. Every device must have its unique symbolic name referring either to a SPICE-like compact model or to a structure obtained by process simulation. With this uniform description, the user can simply select device models with appropriate accuracy. The physical models used by the device simulator can be selected at different hierarchical levels in the input deck: Either for all devices (top level), for one device class, for one special instance of a device class, or for a special segment of a class/instance (lowest level). If no specification is given, default values will be used.

Tibor Grasser was born in Vienna, Austria, in 1970. He studied communications engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1995. He joined the 'Institut für Mikroelektronik' in April 1996, where he is currently working for his doctoral degree. His scientific interests include circuit and device simulation, device modeling and physical aspects in general.

Physical Modeling of Carrier Transport in Semiconductor Devices

Goran Kaiblinger-Grujin

For much of the past 40 years, during which semiconductors technology has advanced from point-contact transistors to megabit memories, drift-diffusion equations have served as the backbone of device analysis. Simple approaches based on the gradual channel approximation and analytical drift mobility and diffusion coefficients were used to treat carrier transport. As devices continue to decrease in size and increase in sophistication, however, this simple picture of carrier transport is beginning to lose validity.

In modeling carrier transport on a microscopic level one faces a variety of different scattering processes which have to be described by the means of quantum mechanics. The way how these processes are modeled (in how far physics is included) limitates the validity of each transport model. However, the more sophisticated the scattering processes are described, the more computer resources are spent. A numerical method for solving the transport problem is the Monte Carlo method which, in many cases, is the most accurate technique available for analyzing carrier transport in devices; it is frequently the standard against which the validity of simpler approaches is gauged, but even the validity of the MC method depends on the way one models the scattering processes and bandstructure.

In modern devices, the carrier concentration is so high that

carrier-carrier interactions play a dominant role. Screening effects and plasma oscillations of the electron gas have to be considered properly. Screening is the response of the intrinsic electrons and the lattice to an external charge. The motion of electrons in the field produced by their own Coulomb potentials causes collective coherent oscillations of the electron (or hole) gas. In general, charged carriers are scattered at more than one impurity atom simultaneously, so that interference effects have to be considered. Moreover, electrons moving through the channel of n-MOSFETs are scattered at the rough interface. From a miscroscopic point of view, this process is not fully understood yet and further research is necessary.

A sophisticated physical scattering model was developed and implemented in MINIMOS 6. This model includes scattering rates of pairs of charged impurities taking into account dynamical screening in a self-consistent way and of electron-plasmon interactions. As plasmons are collective excitations of the electron gas, it is not yet clear how to model energy dissipation and relaxation of charged carriers interacting with plasmons. The comparison of the simulation results with low field mobility measurements over 10^{14} cm^{-3} to 10^{21} cm^{-3} is excellent.

Goran Kaiblinger-Grujin was born in former Yugoslavia, in 1967. He began to study physics at the Technical University of Vienna in 1988, where he received the degree of 'Diplomingenieur' in June 1993. From July 1993 to Feb. 1994 he worked as a technical consultant with an oil company. After his civil service he joined the 'Institut für Mikroelektronik' in January 1995. He is currently working for his doctoral degree. His scientific interests include semiconductor physics and device simulation.

Rigorous Three-Dimensional Photolithography Simulation

Heinrich Kirchauer

Among all technologies photolithography in today's semiconductor industry holds a leading position in pattern transfer. The large costs and time necessary for experiments make simulation an important tool for further improvements. However, the reduction of the lithographic feature size towards or even beyond the used wavelength places considerable demands onto physical modeling. An efficient calculation of the bulk image, i.e. the light intensity within the optical nonlinear photoresist, is the crucial point of the applicability of any model.

Our simulation method is based on a numerical solution of the Maxwell equations for the electromagnetic field and is thus the physically most rigorous approach. The model is not restricted to a planar photoresist layer. Consequently, light scattering effects caused by a nonplanar substrate topography can be simulated. Furthermore, the method accounts for partial coherent illumination and is linked to the etch tool of PROMIS to simulate the development process of the photoresist.

The simulation model is briefly summarized as follows: According to Dill's exposure/bleaching model the electromagnetic field and its relation to the chemical state of the photoresist is described by coupled nonlinear partial differential equations. The quasi-static approximation assumes a steady-state field distribution within a time step. The time-harmonic electromagnetic field obeys a linear version of the Maxwell equa-

tions with an inhomogeneous permittivity. These equations are solved within a rectangular simulation domain and for laterally periodic boundary conditions. Hence, the field as well as the permittivity can be expanded into two-dimensional Fourier series. Insertion and truncation of these expansions transforms the partial differential equations into a set of linear ordinary differential equations of first order in the vertical coordinate. Half of the boundary conditions are given on top of as well as at the bottom of the simulation domain representing the incident, reflected and outgoing light. Hence, we have to solve a complexly valued two-point boundary value problem for the unknown Fourier coefficients of the electromagnetic field. Due to the high memory requirements for three-dimensional simulations we use a "shooting method" such as an algorithm which has the great advantage that the vertical mesh size does not influence the storage consumption. The algorithm algebraically relates to the two-boundary points of the differential equations. In case of partial coherent illumination the algebraic system has to be solved for several different right-hand sides but with the same system matrix.

Heinrich Kirchauer was born in Vienna, Austria, in 1969. He studied communications engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in March 1994. After his studies he worked on a research project about statistical signal processing at the 'Institut für Nachrichtentechnik' for six months. In December 1994 he joined the 'Institut für Mikroelektronik', where he is currently working for his doctoral degree. His scientific interests include three-dimensional process simulation with special emphasis on lithography simulation.

Device Modeling with MINIMOS-NT

Martin Knaipp

Sophisticated device simulators like MINIMOS-NT are capable of simulating devices with arbitrary geometries and materials using different physical models such as drift-diffusion or hydrodynamic models.

When simulating devices with the typical dimensions of several microns, a simple drift-diffusion model can be used to describe the important physical properties of the structure. In this model the unknowns of each grid point are the potential and the electron and hole concentrations. When describing physical effects such as velocity saturation, recombination or impact ionization, we have to consider that only the evaluated quantities of these unknowns and their derivatives can be used as paramaters. This means for example that the impact ionization rate is calculated from the electric field and the current density.

On the other hand, when simulating small devices with typical dimensions lower than one micron, the so-called 'non-local effects' affect the device characteristics. In this case a hydrodynamic model can be used, in which the carrier temperatures as additional unknowns are accounted for. The electrons and holes heated up by the electric field need some time to give their energy to the lattice. In space charge regions, carrier temperatures of several 1000 K can occur. This thermal energy might be transferred to locations outside the high field region. On the other hand ballistic effects such as velocity overshoot can occur when carriers enter high field regions. A

hydrodynamic impact ionisation model must use these temperatures instead of the electric field to describe the generation rate due to impact ionization in a proper way.

Operation in the avalanche region or simulations using strong inversion with convex space charge regions may cause instabilities in the hydrodynamic model when the equation system is solved. Several numerical algorithms have been investigated to find a way to enable device simulations in such cases. These algorithms control the structure of the Jacobian, the damping strategy and the iteration history.

MINIMOS-NT is able to simulate devices for temperatures up to 500 K. Therefore all models have been modified according to the required lattice temperature. A model is a material-specific description of a physical parameter. Usually a model depends on several input quantities. Besides other parameters most models depend on the lattice temperature. Examples for typical models are the mobility, the energy relaxation time or the thermal conductivity. When simulating heterostructures together with frequently used effects such as recombination or avalanche breakdown, the total number of required models of the considered materials can easily be several dozens. All these models will be implemented into an object-oriented library which is called 'model server'. A well defined interface connects the model server with MINIMOS-NT.

Martin Knaipp was born in Vienna, Austria, in 1966. He studied technical physics at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1994. In August 1994 he joined the 'Institut für Mikroelektronik', where he is working for his doctoral degree. His work is focused on device simulation, especially on high temperature effects.

Effects of Strain on Electronic Properties of Semiconductors

Christian Köpf

Modern growth techniques have enabled crystal growth with the highest accuracy both regarding the composition and surface topology. MBE allows the construction of heterojunction devices of semiconductor alloys with monoatomically sharp interfaces. Both transistors (HFET, HBT) and light emitters (LD) fabricated of III-V compounds on GaAs or InP substrates are the heart of today's fastest circuits gaining importance also in the mass market. Apart from the formation of alloys with different properties due to the bulk band structure modification another degree of freedom arises from the strain effects.

When an epilayer is grown on top of another material having a different lattice constant biaxial in-plane stress arises. In case of thin layers on thick substrates the resulting strain distortion only affects the epilayer. Below a certain critical thickness the growth remains completely commensurate leading to pseudomorphic heterostructures. Otherwise misfit dislocations are generated which partially relax the stress. The determination of the resulting strain state and hence the critical thickness is rather difficult since coherent growth can be retained beyond the equilibrium critical value. High annealing temperatures and/or times would be required to completely perform the transformation from elastic to plastic deformation.

The biaxial strain distorts the cubic symmetry of the crystal. It changes the band edge energies and effective masses. This can

be described by deformation potential and $k \cdot p$ theory. In case of the direct Γ gap, which normally has a spherical symmetry, the effective mass becomes different for in-plane and perpendicular directions, hence the mobility is anisotropic. Compression causes the band gap to increase, and both mobility values are lower than in the unstrained case. Under tension the situation is reverted.

The energetic degeneration of the L and X valleys is partially lifted by the strain situation. Strained to (001) substrate the threefold degenerate X minimum is split into a doublet and a single valley, for (111) interfaces the fourfold L minimum reduces to a threefold and a singlet. This change of the valley minima affects the high-field transport properties since intervalley scattering of the electrons significantly depends on the energetic separation of the individual valleys. The anisotropy which occurs through this shift is much stronger than the effects related to the mass changes. Based on Monte Carlo calculations of the anisotropic mobilities, analytical models have been formulated as functions of composition and strain.

Christian Köpf was born in Vienna, Austria, in 1968. He studied Communications and Radio-Frequency Engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1993. He joined the 'Institut für Mikroelektronik' in November 1993, where he is currently working for his doctoral degree. His scientific interests include heterostructure devices, device modeling and solid state physics in general.

Improved Models for Monte Carlo Device Simulation

Hans Kosina

Predictive simulation of semiconductor devices by means of the Monte Carlo method requires an accurate representation of the dominant physical mechanisms. Three mechanisms have been investigated that play an important role for silicon MOSFET operation.

First, channel doping has increased steadily with decaying channel lengths for technological reasons. The drain current is strongly affected by scattering on charged dopants in the channel. The Brooks Herring treatment of charged impurity scattering significantly overestimates the low-field mobility. A refined model including dynamic screening and a two-ion correction has been developed and evaluated. With the new model and with plasmon scattering as an additional concentration-dependent process very good agreement with empirical mobility data has been achieved.

Second, due to the high lateral field in the channel mobility is reduced by surface scattering. For application in device simulation we are developing a more phenomenological approach to surface roughness scattering which neglects quantization effects. On the other hand, in a basic research project we investigate non-linear transport in the subband system formed in inversion layers. A formalism to solve the Schrödinger equation for a non-parabolic band structure has been developed and implemented in a numerical Schrödinger-Poisson solver. The

subband energies and the subband effective masses have been calculated as a function of non-parabolicity. One consequence of non-parabolicity is that the wave functions and related quantities such as matrix elements become dependent on the in-plane wave vector. Compared to the parabolic case the two-dimensional scattering rates are higher due to increased effective mass, energy-dependent density of states and k-dependent overlap integrals.

Third, for p-channel devices an accurate valence band model is needed. To represent the valence bands of cubic semiconductors a coordinate transformation is proposed such that the hole energy becomes an independent variable. This choice considerably simplifies the evaluation of the integrated scattering probability and the choice of the state after scattering in a Monte Carlo procedure. A numerically calculated band structure is expanded into a series of spherical harmonics. This series describes equi-energy surfaces in k-space. Details of the band structure at the Brillouin zone boundary can be resolved and hence energies up to several electron-volts can be treated.

Hans Kosina was born in Haidershofen, Austria, in 1961. He received the 'Diplomingenieur' degree in electrical engineering and the Ph.D. degree from the Vienna Technical University in 1987 and 1992, respectively. For one year he was with the 'Institut für flexible Automation', and in 1988 he joined the 'Institut für Mikroelektronik' at the Technical University of Vienna. In summer 1993 he held a visiting research position at the Advanced Research and Development Laboratory at Motorola, Austin. Currently he is employed as an assistant professor in the device modeling group. His current interests include modeling of hot carrier phenomena in semiconductor devices, quantum effects and computer aided engineering in VLSI technology.

Parallelization of Program Packages for the Simulation of Semiconductor Processes and Devices

Erasmus Langer

The simulation of realistic semiconductor devices and their technological fabrication processes imply high demands on computer resources, especially concerning the needed computing power, but also the memory requirements. In order to intensify the research capability of the simulation tools, an increase of the throughput and, therefore, an acceleration of the programs are an absolute necessity. This project is planned to be part of an interuniversitary project, the 'Spezialforschungsbereich' AURORA — Advanced Models, Applications, and Software Systems for High Performance Computing. Eleven institutes of the University of Vienna and the Technical University of Vienna are participating in the project AURORA which actually is in the state of preparing the final proposal to be funded by the Austrian 'Fonds zur Förderung der wissenschaftlichen Forschung (FWF)'.

The Monte Carlo method is rapidly gaining acceptance as a means for the simulation of ion implantation — the most important process step for incorporating doping ions into semiconductors — because it accounts well for the physical reality. The Monte Carlo method plays an important role within the device simulation, too. MINIMOS uses different transport models — depending on the geometry, the bias conditions, and the desired accuracy – one of which is the Monte Carlo transport model.

A well-known drawback of the Monte Carlo approach is its considerable demand for computer resources to obtain results with satisfying statistical accuracy. Therefore, the time characteristics have to be optimized in order to utilize the Monte Carlo-based solution method for practical investigations, e.g., investigation of the influence of the doping profile on the electrical behavior of the device where a loop over process and device simulation must be performed several times. Particle-based simulation is well suited for parallelization. Although that kind of acceleration seems to be trivial, the question of load distribution arises since the time needed for the calculation of a single particle varies over all particles by about a factor of ten. One main goal will be the development of parallel, Monte-Carlo-based algorithms running on heterogeneous workstation networks or on distributed memory architectures. In the long term, these parallelized algorithms shall be implemented within the corresponding modules (MINIMOS and PROMIS) of the framework VISTA.

Erasmus Langer was born in Vienna, Austria, in 1951. After having received the degree of 'Diplomingenieur' from the Technical University of Vienna in 1980 he was employed at the 'Institut für Allgemeine Elektrotechnik und Elektronik', first as a research assistant and then as assistant professor. In the beginning his research field was the numerical simulation of semiconductor devices and later the excitation and propagation of electro-acoustic waves in anisotropic piezoelectric materials where he also received his doctoral degree in 1986. In 1988 he joined the newly founded 'Institut für Mikroelektronik'. Currently he is mainly working in the field of simulation and analysis of micro-structures with a focus on ultra large scaled integrated semiconductor devices and acoustic wave devices.

Using Layout Data in the VISTA Framework

Rui Martins

The VISTA framework is able to read layout data from external sources and display it within the PIF Editor (PED). The two formats used most often, namely the Caltech Intermediate Format (CIF) and Calma GDSII, are supported. To enhance the display quality of layout in PED, special parameters like mask colors and textures are technology dependent according to their specification in the technology file.

VISTA is not intended to have all the layout handling features that are found in general purpose ECAD frameworks, nevertheless the necessity to be able to realize some basic operations does exist. Apart from the purely geometric functions (eg. creating, moving, deleting points, lines...) that already existed in PED (in the so-called material-mode to differentiate from the new layout-mode), we have added some more high-level layout handling possibilities, such as selection of area(s) of interest, boolean operations with masks and hide/show particular mask-names.

As two-dimensional simulators are widely used in Technology CAD frameworks and in order to use layout data with them, there is a need to define a cut-line, which specifies the domain of the simulation to be performed. This task is now done interactively in a user-friendly manner, where possible misuses (as specification of cut-lines in a piece of layout with large changes in the orthogonal direction) are detected and reported

in warnings. The resulting one-dimensional masks are stored in a LISP-like format file that is understood by the VISTA Simulation Flow Control Module (SFC). In this way it is possible to perform a sequence of process (and consequently device) simulations without the need of expressly specifying absolute etch coordinates. This means that at a certain stage of the process flow, apart from the technology-related parameters, one only needs to choose the mask name or a combination of masks that are involved at that particular step.

The use of mask information with three-dimensional simulators like the Smart Capacitance Analysis Program (SCAP), its thermal counterpart (STAP) and the lithography simulator, is demanding new requirements in how layout is represented in VISTA. As an example, we would like to mention the need to support phase-shift masks and an efficient interface with the solid modeler. Research is being carried out on these issues, with special emphasis on the metalization steps, as interconnections are becoming more and more a limiting factor in IC technology.

Rui Martins was born in Porto, Portugal, in 1968. He studied electronic and telecommunications engineering at the University of Aveiro - Portugal, where he received the degree of 'Licenciado' in 1991 and 'Mestre' in 1994. In 1993 he was with INESC (Institute for Systems and Computers) where he worked on biomedical instrumentation. He joined the 'Institut für Mikroelektronik' in October 1994 and is currently working for his doctoral degree. His scientific interests include very low power analog and digital integrated circuit design, digital signal processing and TCAD framework aspects.

An Object-Oriented Model Database and Description Language

Robert Mlekus

The continuous development of new processes and devices in combination with the increasing number of devices on a single chip requires a permanent improvement of simulators by way of implementing new or enhanced models and algorithms. In traditional simulators the integration of such new models requires changes in the source code of the simulator and therefore deep knowledge of implementation details. For that reason a new library has been developed, which provides an object-oriented approach to the implementation, parameterization and selection of models, without any changes in the source code of the simulator. The development of models is decoupled from the rest of the simulator, whereby simulators have easy access to a selection of different models and models can easily be interchanged between several simulators.

Any model is represented by an object which encapsulates instructions, private variables, parameters, documentation of the model and the information about the type of the model in a single unit. Models inherit their basic functionality from a generic C++ model class and an arbitrary number of previously defined further model classes. In analogy to other object-oriented programming languages, a hierarchy of model classes is originated. New models can either be defined by coding them in C++ or C, or by using the *Model Description Language*. The latter allows the definition and use of new models in *Model Definition Files* and on an input deck, without re-

compiling the simulator. Some predefined parameter types for standard C++ and C data types can be supplied by additional types deduced from any variable type. A database of models is formed by combining several libraries containing object code and *Model Definition Files.*

The *Model Description Language* allows the specification of the actual type of a specifically required model instance, the declaration of default values for its parameters , and last but not least the definition of new models. New model types are defined by combining any number of previously defined models in a new type and specifying the evaluation rules and parameters of the interface. Furthermore default values for the parameters as well as documentation can be provided.

Models are integrated into the simulator during run time by requesting a model instance with a unique instance name and a required model type from the *Library Manager.* Their parameters are linked to interfaces which have to be provided by the simulator. Any model can be accessed for evaluation, specification of parameter values, acquiring documentation and other tasks by using unified methods.

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Process Flow Representation and Design Automation

Christoph Pichler

The Simulation Flow Control Module (SFC) has matured over the last year to form a robust and reliable basis for various kinds of task-level analysis tasks. The iterative submission of flow experiments is supported by an improved run scheduler to minimize the required computation time. A *make*-like mechanism prevents identical operations from being submitted; working on an asynchronous basis, multiple attempts to build a file are detected, with callbacks being attached to the file descriptor to notify the clients of the completion of the desired operation. Automatic purging of intermediate results that are no longer needed minimizes the amount of disk space required for large-scale experiments. Special emphasis has been given to the providing of full batch mode and interactive mode capabilities without the need for a visual user interface, thus allowing convenient operation on ASCII terminals or across phone lines.

Flexible programming on the task level is supported by a layer of dedicated objects for the representation of complete process flow simulation tasks and agents for the communication with external design-of-experiments (DoE), response-surface-modeling (RSM), and optimizer modules. *Evaluable Entities* encapsulate all kinds of evaluation tasks, providing a uniform interface for parameter passing and response extraction. A layout interface has been implemented and allows cutlines for process simulation to be defined in the layout editor, thus con-

siderably enhancing the versatility of the TCAD environment. An improved flow editor is being developed, which will also address the definition of a uniform representation of all kinds of resources on all framework levels and will allow for flexible data-entry forms.

Successful endeavors to simulate complete semiconductor fabrication sequences without the necessity of skipping or faking certain process steps have had an invaluable impact on the quality and stability of framework gridding services and other auxiliary services, which have reached a satisfactory level by now and pave the way towards a PIF wafer processor which encapsulates simulation tools and auxiliary framework tools to form the core module for high level analysis tasks. Moreover, these "real-life" situations have led to the identification of several flaws in existing simulation tools and to considerable improvements in many areas then uncharted.

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Process Optimization in Technology CAD

Richard Plasun

The large number of integrated simulators in the VISTA TCAD framework makes it a flexible and powerful environment for the design of semiconductor devices, especially for MOSFETS. For the optimization of new devices one has to find the best process parameters for a given process flow, layout mask information and electrical properties of the simulated device. Because of the large number of simulator executions it is very important that these tasks can be run in batch mode without terminal or user interaction.

For these optimizations several facilities are available in the VISTA framework. A Design of Experiments (DOE) Module for automatic generation of experiments is used to generate a set of experiments in the specified input parameter subspace. The module provides a number of experiment designs — like Central Composite Circumscribed design (CCC) — or sensitivity analyses. The framework submits the experiments and extracts the responses with internal or external tools after termination.

A mathematical model can be fitted to a given set of input parameters and simulated responses. This technique — known as Response Surface Methodology (RSM) — is used to get a fast model of the trend of responses by varying input parameters. It is also needed for approximations to decrease the calculation time. Additional transformations for the parameters can

be evaluated automatically or are supplied by the user. They are important for the quality of the fitted surface and can be added to the description of the DOEstep for a better set of experiments.

A nonlinear constrained optimizer and a Levenberg–Marquardt nonlinear least square fit algorithm for simulator calibration are integrated into the framework. They are external tools and communicate with *evaluable entities*, LISP objects representing a generalized input-output relationship e.g. simulator runs or response surfaces. By defining an objective function which depends on the input and output parameters the optimal process parameters can be found. Thus also an optimization task is represented by an *evaluable entity*, and complex problems can be formulated in a straightforward manner by linking these objects together.

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Advanced Process Modeling in Multilayer Structures

Helmut Puchner

Process modeling is an important task in process simulation. By decreasing the thermal budget during processing many effects have been figured out in the last years. For specific applications it is no longer tolerated to ignore effects like point-defect enhancement, stacking faults or mechanical stress. The conventional process models have to be revised with state-of-the-art methods to gain new perspectives. The main problem of diffusion models developed nowadays is the insufficient verification of experimental data, because there are less data available or the data are measured under different process conditions. Therefore the process modeling procedures mostly capture specific problems. Nevertheless, process simulation gives a more detailed description of the "real" process than the measured results alone can do.

We have been developing the new process simulator PROMIS-NT to solve the diffusion problem in an arbitrary two-dimensional structure. The box integration method is used to discretize the diffusion equation on a specified ortho-product or unstructured grid. Several physical models for the diffusing dopants are available, e.g. uncoupled diffusion or coupled diffusion including the Scharfetter-Gummel discretization. Different models can be applied on different target materials to avoid a modeling overkill in inactive device regions.

Another important task in the simulation of diffusion pro-

cesses is finding the initial dopant distribution by a former ion implantation process. There are two basic methods to simulate the ion implantation, first the Monte Carlo method, where the flight path of a single ion is calculated and stored in boxes when the final energy is reached, and second an analytical description of the implantation process by means of probability moments. Several distribution functions can be derived from these probability moments. We have used the so-called "L-Moments" in combination with the "Four-parameter Kappa Distribution Function" for the first time in semiconductor simulation to specify the dopant profile. To resolve the arbitrary two-dimensional simulation geometry we have used a slab method, where in each slab the vertical distribution function is initialized and the lateral distribution is given by a convolution integral.

All of the above activities are embedded in the VISTA project, and all the physical parameters are provided by VISTA's Material Server data base.

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Simulation of Thermal Oxidation in Three-Dimensional Silicon Structures

Mustafa Radi

Thermal oxidation of silicon is one of the most important steps in the fabrication of highly integrated electronic circuits being mainly used for efficient isolation of adjacent devices from each other. Knowledge of the physical processes that affect thermal oxidation is essential for optimizing applications. Because of their complexity the physical mechanisms are not yet fully understood and until today no satisfying model that matches all experimental conditions has yet been found.

Miniaturization of devices based on silicon technology leads to the realization of integrated structures exhibiting an increasingly complex topology. The evolution of isolation techniques using local oxidation of silicon (LOCOS) is one of the most striking examples for that purpose. In order to reduce the developing duration of such state-of-the-art technologies, two- and three-dimensional process simulation capabilities are of prime interest. Difficulties in numerical modeling of silicon oxidation arise from the necessity to ensure both a wide prediction capability and a very flexible numerical solution method. The modeling accuracy involves the characterization and calibration of the mechanical thin film properties of integrated circuit materials as well as stress effects of the oxidation kinetics, while the efficiency of the numerical implementation concerns its ability to handle complex topological configurations within reasonable computing time. To cope with these different requirements an extremely flexible simulator has to be developed.

Therefore a mathematical input-parser has been implemented to simplify the handling of several differential equations. As a second step a finite-element solver for one, two and three dimensions has been added to this mathematical input-parser which automatically detects the degree of coupling between different quantities as well as moving grids, parameters and abbreviated quantities. With these tools it should be possible to solve many physical problems without high efforts, even the diffusion-reaction behavior in order to compute the oxidant concentration, thus leading to a growing oxide-layer with material deformation based on several mechanical models.

Obviously the computation time and memory requirements of such a complex coupled simulation, especially in three-dimensional problems, will rapidly increase if no powerful numerical solver is available. Therefore first steps to develop a fast multigrid solver, which is known as a very stable method for solving non-linear equation systems, are undertaken. Furthermore, using this kind of solver preserves all possibilities of efficient parallelization on massively parallel computers as well as on heterogeneous networks, which will surely be of increasing interest in the near future.

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A Graphical Editor for TCAD Applications

Gerhard Rieger

The PIF editor (PED) is a program for interactive and batch mode data processing within the VISTA framework. Its extensibility makes it a powerful tool for complex TCAD applications as well as for some tasks that it has originally not been designed for.

A couple of already implemented functions for basic semiconductor modeling operations may be combined to procedures for the generation of complete semiconductor devices using the extension language Vienna LISP (VLISP). This makes it possible to generate input data for the simulation of semiconductor devices and processes.

Example procedures have been developed for diode, MOSFET, and CCD devices. They are implemented as functions using steps that perform subdomain, grid generation, analytical doping generation, and deposition to build the desired structure. Control panels allow to interactively specify the structural, geometric, and doping parameters for these functions.

To support the editing of three-dimensional structures support for displaying, for some simple modeling operations, and for inquiring properties of such devices has been implemented.

A task that is less mainstream-related is an interactively controlled data conversion from horizontal layout to device data. For this purpose the PIF editor has been extended for displaying layout data. In this layout mode it is possible to import files in GDS II or CIF formats and convert them to a special

layout-oriented PIF version. For further processing a cut line or a rectangular area may be specified graphically. An external program cuts the layout down using this selection and further generates waferstate data by combining the mask information with a technology description.

Another extension of the PED is the generation of geometrical figures. For a technical description of a three-dimensional transformation and projection a routine has been written using the extension language VLISP to show the geometric circumstances and relations. Starting from a simple geometric object it calculates the projection onto a plane and converts these spatial images to one picture. The complete result is displayed in the usual three-dimensional mode.

These examples give a brief overview of the capabilities of the PIF editor which are archieved by combining the data interface, user interface, and graphical features by means of its universal extension language VLISP.

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Automatic Grid Refinement for Device Simulation

Martin Rottinger

For a numeric simulation of semiconductor devices the simulation domain has to be discretized, therefore an appropriate grid is required. The quality of the grid is crucial for the accuracy of the simulation results. A coarse grid or a grid with strongly varying density will produce inaccurate results or will prevent convergence. On the other hand a grid containing many nodes, especially in areas not important for the accuracy of the simulation, might exceed memory or runtime resources. Therefore a carefully adapted grid is a prerequisite for fast and accurate simulations and deserves much effort.

The input data for a device simulation is often provided by a preceding process simulation. Because of the properties of the physical effects taken into account, such as deposition, etching, implantation, and diffusion, the grids used for process simulation are not suitable for device simulation. A simple example is the channel region of a MOS transistor which has to be gridded completely differently for process and device simulation. The channel only builds up under appropriate biasing and a much finer grid than in the bulk region is necessary to obtain accurate results.

In contrast to tensor product grids triangular grids make it possible to vary the grid density according to variations in the simulated device without introducing a large number of unwanted grid nodes. Additional grid nodes can be placed in

areas of the simulation domain where they are necessary to obtain the desired accuracy, minimizing the number of overall grid nodes.

Starting from the results of a process simulation the first step is to use the net doping and the location of the contacts to search for pn-junctions and possible channel areas. This information is used to create a suitable starting grid. Using this grid a simulation is performed. From the result different attributes, such as potential, carrier concentration or current density are used to decide whether a further grid refinement is necessary. It is important not only to increase the number of grid nodes where it is necessary, but also to remove nodes which are not crucial for the accuracy of the simulation in order to reduce the memory and runtime requirements.

The aim is the developement of an algorithm and to integrate it into the device simulator MINIMOS-NT in such a way that MINIMOS-NT can be used as part of a simulation flow consisting of process and device simulation steps without the need of user interaction for grid specification or refinement.

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Three-Dimensional Thermal Interconnect Simulation

Rainer Sabelka

In very large scale integrated (VLSI) circuits reliability issues with respect to interconnects are an important concern. These include the electromigration phenomenon for interconnects stressed at a current density for a relatively long period of time as well as the instantaneous failure caused by high current pulses. Efficient investigations of temperature rise due to Joule heating created by current flow can be achieved by means of a coupled electro-thermal simulation.

Hence we have developed the simulator STAP (Smart Thermal Analysis Program), which uses the finite element method to calculate the distributions of the electric potential and the temperature of two- and three-dimensional interconnect wiring structures. The potential is calculated by solving Laplace's equation for each isolated wiring structure separately, leaving out areas with zero conductivity. Neumann (constant current density) or Dirichlet boundary conditions (constant voltage) can be specified on the borders of the electric simulation subdomains.

To obtain the temperature profile the heat conduction equation is solved over the whole domain. Therefore the power loss density has to be derived from the calculated potential distribution. For the thermal part of the simulation the user can specify Dirichlet boundary conditions (constant temperature) on the surface.

The simulator features a static and a dynamic mode. Hence one can calculate the temperature distribution for constant current densities as well as for transient pulses.

The electrical resistivity of the conducting materials can depend on the temperature. Therefore in static mode both the electric and the thermal simulations have to be repeated several times until an equilibrium has been established.

The finite element solver uses triangular and tetrahedronal elements with linear or quadratic shape functions. A preconditioned conjugate gradient solver is used to solve the linear system. The backward Euler method has been implemented for simulating the transient behavior.

The format of the simulator's input and output files are compatible to those of our capacitance extraction program SCAP (Smart Capacitance Analysis Program). Thus various already existing pre- and post-processing tools can be utilized.

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Ultra-Low-Power VLSI Technology

Gerhard Schrom

The fast growing portable-electronics market as well as thermal dissipation, reliability, and scalability issues have launched a massive trend towards low-power and low-voltage technologies. Following the approach of *ultra-low-power CMOS*, the power consumption can be cut down substantially by drastically reducing the supply and threshold voltages – down to several 100mV – without compromising the system's performance. A loss in device speed can be compensated on the system's level by appropriate parallel architectures. This leads to an even better device reliability and process scalability, and to a reduction of the power consumption by orders of magnitude at the same performance of the system. Analytical investigations of the minimum CMOS switching energy E_s of the intrinsic inverter have shown that E_s decreases with the square of the effective gate length. Moreover, E_s can be reduced to a point where the electron charge and thermal noise are the limiting effects, confining the minimum switching energy to 0.25aJ. This is more than four orders of magnitude better than today's low-power technologies.

The development towards lower voltages poses increasingly stringent demands on compact device model accuracy. Therefore a new approach to dynamic MOSFET modeling has been developed which is especially suited for the simulation of low-voltage mixed- analog-digital circuits. The model is based on terminal charges and conductive currents which are determined from transient current/voltage data. These data sets can easily

be obtained through measurement or simulation of the devices. Using a physically motivated interpolation method the model supplies accurate current/charge data and their derivatives for given terminal voltages. This enables accurate simulation of modern low-voltage mixed-analog-digital circuits.

For low-power mixed-analog-digital systems it would be advantageous to have compatible ultra-low-voltage (ULV) analog components such as op-amps to keep the process technology simple. A major challenge is the discrepancy between analog and digital technologies concerning the supply and threshold voltages which must be higher for analog applications. To find the lower limits of the supply voltage a set of basic analog circuits designed with dedicated digital ultra-low-power (ULP) processes has been simulated to determine the achievable performance. It has been found that voltage gains of more than 60dB are possible at $V_{DD} = 0.5$V and more than 38dB at $V_{DD} = 0.3$V. The big advantage of this strategy is the compatibility of analog and digital devices which enables a simple ULP mixed-analog-digital process technology without compromising performance on the system's level.

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Simulation of Heterostructure Field-Effect Transistors

Thomas Simlinger

In recent years Heterostructure Field-Effect Transistors (HFETs) have been amongst those heterostructure devices which have become an essential component of industrial electronics because of their outstanding high-frequency performance. Gate lengths below 250 nm and gate-to-channel distances of about 30 nm are state-of-the-art. A further reduction of the feature sizes to improve the high-frequency performance poses new problems to the device design. Besides the requirements on process technology these problems can be attributed to non-local effects such as *velocity overshoot* of electrons within the channel, tunneling effects at the interfaces, and the *real-space transfer* due to carrier heating.

Thus, the simulation of HFETs becomes increasingly important for studying the influence of non-local effects on device characteristics. The device simulator MINIMOS-NT has been developed as a flexible tool for the simulation of HFETs. It is capable of analyzing the complex structures of various transistors and of selecting the appropriate physical models automatically. The modeling of the interfaces between different layers is crucial for the consideration of non-local effects. Therefore, several interface models for heterojunctions have been developed and implemented.

To properly account for the real-space transfer it has been necessary to implement a model for thermionic emission of

the electrons. For the calculation of the carrier temperatures, which are essential for this model, the hydrodynamic model of MINIMOS-NT is used. Additionally, the model of the current flow across the heterojunction into the upper barrier layer at the drain-sided end of the channel must include tunneling effects. Thus, the thermionic emission model has been extended to the thermionic field emission model, which accounts for the field-related tunneling of the carriers through the interface. The exponential dependence of the thermionic field emission on the carrier temperature tends to deteriorate the efficiency of the simulator, which must be taken into account for the implementation of these models. The functionality of MINIMOS-NT has been extended to the interface models and thus makes it possible to control the influence of the interface models on the behavior of the simulation process.

The simulation results of different state-of-the-art HFETs show a good agreement with the measurements and point out that modeling of the interface characteristics is of crucial importance. The achievement of simulation results with suitable accuracy to sustain the further development of HFETs is impossible without appropriate interface modeling.

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Three-Dimensional Geometry Generation for Interconnect Analysis

Andreas Stach

Miniaturization of VLSI device dimensions improves circuit speed and packing density. Down-scaling reduces the device delay, whereas the RC delay of interconnects stays approximately constant. While devices are steadily scaled down, interconnect delay that is mainly determined by the resistance and capacitance of the metal lines becomes more and more a significant limitation of VLSI circuit performance.

In the past interconnect capacitances were estimated at the circuit level by using analytical formulas with parameters derived from the layout, e.g. metal thickness, line width, and spacing between the lines.

For more accurate investigations of interconnect capacitances the three-dimensional geometry of the VLSI circuit has to be considered. This geometry has to be generated out of layout information and process information. Therefore a boundary-representation-based solid modeler is under construction which performs basic process steps (e.g. deposition, etching) with two-dimensional geometric mask data available in CIF or GDS-II format.

To permit flexible, memory-efficient and fast geometric data handling a linear dually hashed data structure is used. Each relation between two modeling primitives (points, lines, faces, solids, segments) is stored in a forward hash (e.g. face⇒line) and a backward hash (e.g. line⇒face). This data structure

also allows the representation of non-manifold geometries (with loops and shells) by referring primitives of the same hierarchical level (e.g. face⇒face, solid⇒solid).

The interconnect capacitances between the conductors of a generated three-dimensional geometric structure are calculated by means of our three-dimensional capacitance analysis program SCAP, which uses the finite element method to discretize Laplace's equation to derive the potential distribution for certain potentials applied to conductors.

To permit accurate transient-analysis of VLSI circuits, the existing interconnect capacitances have to be inserted into the active device net list of the investigated circuit. With MINISIM a charge based circuit simulator has been developed which allows the performance of transient and dc-analysis of discretized active device models extracted by the device simulator MINIMOS-NT as well as analytical device models.

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Simulation and Characterization of Complex Semiconductor Processes

Rudolf Strasser

The simulation of today's semiconductor technology requires the application of highly specialized tools for the appropriate modeling of process steps. This leads to a modular concept of process simulation as implemented in the VISTA framework. The TCAD shell makes use of various simulation tools, each of which is tailored to specific needs.

Using heterogeneous tools requires a so-called wafer-state gridder, which provides the input data to the simulators and assures the consistency of the output data. An implementation of a wafer-state gridder is TRIANGLE. Based on a highly efficient Delaunay grid algorithm it takes care of the recovery of the wafer state, merges dopant distributions with the output of topography steps, or re-grids the simulation domain, producing high quality locally refined grids.

Using the high level capabilities of VISTA's simulation flow control module (SFC), TRIANGLE is extended to a so-called wafer-state server. Conceptually simulators can be viewed as wafer-state processors which receive the wafer state from the server, operate on the data and provide them to the server again. This concept provides a well-defined data interface and thus enables the integration of heterogeneous simulation tools. The achievements in VISTA's process simulation capabilities have led to a pool of simulators being capable of simulating state-of-the-art technology.

As the development of a new semiconductor technology requires a lot of experiments, the design of experiment (DOE) features incorporated in the VISTA framework are heavily used. DOE is used for finding a process window, identifying key parameters and for producing the experiment databases needed for response surface modeling.

A key issue in process simulation is a reliable characterization of the devices delivering a measure for the quality of a specific process variant. Electrical parameters extracted by means of device simulation are valuable inputs for optimization tasks. Therefore a library of characterization modules including threshold voltage-, saturation current-, sub-threshold slope-, body effect- or substrate current extraction etc., will be implemented.

With the ongoing miniaturization of semiconductor devices not only the simulation of intrinsic devices is of interest, but also parasitic effects such as latch-up or isolation effects are becoming the targets of process optimization. Characterization of these effects will be carried out with the new device simulator MINIMOS-NT.

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Nonlinear Electron Transport in Silicon Inversion Layers

Christian Troger

To meet the demands of modern microelectronics, field effect transistors have to be scaled down in size, which leads to a strong confinement of carriers to the channel and restricts the motion of electrons to one dimension. Therefore device simulation must investigate the accuracy of the existing models for the carrier transport in such devices.

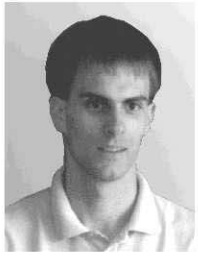
For the theoretical study of the transport properties of a quasi two-dimensional electron gas at an inverted Si/SiO_2 interface the semi-classical Monte Carlo method has become very popular. All subsequent calculations in such a simulation are based on the determination of the eigenstates of the electrons, which are obtained from a self-consistent solution of the Schrödinger and Poisson equations. Since non-parabolicity has a strong impact on high field transport, this effect has to be considered when choosing a representation of the operator of the kinetic energy.

The developed Schrödinger-Poisson solver for MOSFET structures uses the effective mass approximation and a new formalism that allows the inclusion of non-parabolicity. It is assumed that the wave functions can be separated into a plane wave parallel to the interface and an envelope function in the normal direction. Using the momentum representation and assuming a vanishing wave function at the boundaries, sine functions can be choosen for the base and the numerical task reduced to the

solution of a matrix eigenvalue problem. In contrast to the parabolic case, the envelope function is no longer independent of the wave vector parallel to the interface, so this dependence has to be included in an analytical model.

From the simulation tool described so far a better insight in quantized systems can be obtained. Thanks to a simultaneous visualization of all relevant quantities and a graphical user interface which allows the modification of all parameters it is easy to estimate the impact of different approximations and to study the progress of the iterative solution.

Actually, it seems favorable to introduce a nonparabolicity coefficient and an effective mass for each subband and extract their values using first order perturbation theory. As a consequence of the inclusion of nonparabolicity a larger effective mass in each subband and a narrowing of the wave function can be observed. This will result in increased scattering rates.



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Multiple Projects within VMAKE

Walter Tuppa

The VISTA project of our institute has grown larger and larger during the past years so that it has become problematic to handle it as one big project. This was because existing software has turned more complex and new simulators have been added to the project. Therefore VMAKE was enhanced to allow splitting this very large project into smaller ones which can be handled easier. In addition to file dependences VMAKE is now able to handle project dependences.

Within VMAKE, projects are defined by a special short description file in the top directory of the project (all working projects are required to be a subdirectory of a common parent directory). In this file the developer declares a symbolic name for the project and dependencies to other projects handled by VMAKE.

Handling multiple projects at the same time with consistent checking of dependences between them is quite a difficult task. Each project can be used as a working project (all sources are available for compilation) or as an installed project (only objects and libraries are available at a common location). Further cross dependences between projects are not allowed. Project information is only loaded on demand to speed up the startup of the tool. Dependence information of files is generated on demand, too, and is only extracted from one level instead of from all inclusions, so that include files are handled in the same way as source files. This speeds up the dependence generation process significantly and allows dependence generation on de-

mand during any run of VMAKE. Because of the support of multiple projects, the developer has now to declare include files if they shall be used by some other projects.

In addition to supporting multiple projects at the same time VMAKE is now capable of building goals in parallel if they are independent from each other on a homogeneous workstation cluster with a symmetric filesystem. Under UNIX remote shells and under VMS batch queues are used for parallel execution. This can speed up the build process significantly (e.g. by a factor of 4 to 5 using seven DEC Alpha workstations compared to one local execution).

After having split VISTA into smaller projects VMAKE itself now consists of three projects. The first one is the Vienna Base System, which handles all system dependences. The second one is the LISP interpreter which is used by VMAKE and reused within the VISTA project. The last one is the VMAKE project consisting mostly of LISP source files.

Walter Tuppa was born in Vienna, Austria, in 1966. Having received the degree of 'Diplomingenieur' in computer science from the Technical University Vienna in 1991 and in electrical engineering in 1992, he joined the 'Institut für Mikroelektronik' in July 1991. He works on th VISTA project. At present, he is working for his doctoral degree in electrical engineering.

SIMON: A Single Electron Tunnel Device and Circuit Simulator

Christoph Wasshuber

Due to the tremendous capabilities inherent in the field of Single Electron Tunneling (SET) this technology has gained a lot of interest in the last years. Although being still far away from producing SET devices industrially one is close enough to fabricate experimental devices and consider possible future applications and production techniques. With this technology extremely small and low-power devices can be produced, with the advantage that their basic performance parameters improve by down-scaling their spatial dimensions. In the laboratory many SET devices such as transistors, memory cells, pumps, turnstils and various logic gates (Inverter, NOR, etc.) have already been produced and tested. Recent advances have been the fabrication of a seven-junction-electron-pump which is used for metrology, and a 64-bit single electron memory chip operating at room temperature.

In this phase, where theoretical results are experimentally verified, where new ideas in process technology and device architecture emerge, the need for a quick numerical evaluation of the proposed devices is obvious. Furthermore, interest in the circuit level of SET increases. Analytical results are only possible for the simplest devices. The aim of this project was to develop a SET device and circuit simulator which fills a part of the gap between theory and industrial production.

The goal was to build a tool which makes it possible to quickly

and efficiently simulate a wide variety of single electron circuits. SIMON uses a Monte Carlo technique to simulate the tunnel events of single electrons through various arbitrarily connected tunnel junctions. The change in energy for the whole system for each possible tunnel event determines the probability of this particular event, which further determines the average time between consecutive tunnel events. A main feature of SIMON is the inclusion of the so-called Macroscopic Quantum Tunneling of Charge (q-MQT) phenomenon. This quantum mechanical effect is a simultaneous tunneling of two or more electrons in two or more tunnel junctions via an intermediate virtual state. This parasitic effect is the main source of errors in single electron logic. Besides tunnel junctions and capacitors, one can specify ideal voltage sources, either constant, piece-wise linearly time dependent or voltage controlled. For the ease of use a graphic user interface with a graphic circuit editor has been implemented.

The goal is to use SIMON for the numerical verification of proposed devices and whole logic architectures, to support the improvement of these devices and to evaluate disturbing effects coming from thermal agitation and q-MQT of electrons.

Christoph Wasshuber was born in Vienna, Austria, in 1968. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in March 1993. Afterwards he studied for one and a half years at the University of Tokyo, Japan, starting his doctoral research. In April 1995 he joined the 'Institut für Mikroelektronik', where he is currently working for his doctoral degree. His work is focused on device simulation, especially quantum mechanical devices.

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