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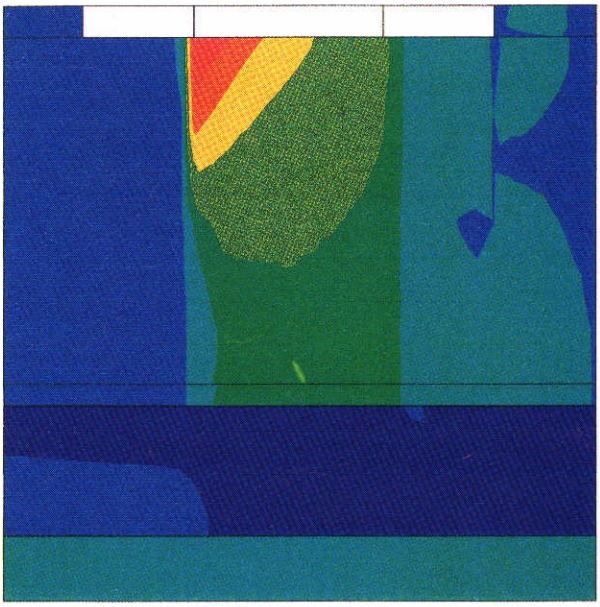

Annual Review
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INSTITUTE FOR MICROELECTRONICS

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INSTITUT FÜR MIKROELEKTRONIK
Technische Universität Wien
Gußhausstraße 27 – 29
A – 1040 Wien
AUSTRIA

Tel: *43/1/58801/3850
Fax: *43/1/5059224

Staff

Robert Bauer	Dipl.–Ing.	
Walter Bohmayr	Dipl.–Ing.	(Dec. 1, 93 –)
Franz Fasching	Dipl.–Ing.	
Claus Fischer	Dipl.–Ing., Dr.	
Predrag Habaš	Dipl.–Ing., Dr.	(– March 31, 94)
Michael Hackel	Dipl.–Ing.	
Stefan Halama	Dipl.–Ing., Dr.	
Ewald Haslinger		
Marion Kaltenbrunner		(– Oct. 31, 93)
Christian Köpf	Dipl.–Ing.	(Nov. 1, 93 –)
Hans Kosina	Dipl.–Ing., Dr.	
Erasmus Langer	Dipl.–Ing., Dr.	
Ernst Leitner	Dipl.–Ing.	
Christoph Pichler	Dipl.–Ing.	
Hubert Pimingstorfer	Dipl.–Ing., Dr.	(– Dec. 31, 93)
Helmut Puchner	Dipl.–Ing.	
Gerhard Rieger	Dipl.–Ing.	
Gerhard Schrom	Dipl.–Ing.	
Siegfried Selberherr	O.Univ.Prof., Dipl.–Ing., Dr.	
Thomas Simlinger	Dipl.–Ing.	
Andreas Steidl	Ing.	
Martin Stiftinger	Dipl.–Ing.	
Hannes Stippel	Dipl.–Ing., Dr.	(– Dec. 31, 93)
Ernst Strasser	Dipl.–Ing.	
Walter Tuppa	Dipl.–Ing.	
Renate Winkler		(Nov. 1, 93 –)

Preface

Siegfried Selberherr

This brochure is the sixth annual research review of the institute for microelectronics. The staff supported by the Austrian Ministry of Science and Technology consists presently of eight full time employees: the head of the institute, four scientists, a secretary and two technical assistants. Fourteen additional scientists are funded through scientific projects!

From September 7-9, 1993 the 5th International Conference on Simulation of Semiconductor Devices and Processes (SISDEP) took place under our guidance and organization. An extensive programme was compiled with 80 oral presentations and 40 posters selected by the international conference committee from 227 contributed abstracts. This attracted 245 participants from 28 countries. SISDEP 93 was the largest event of its kind that ever took place.

The projects of the institute are, in a continuation of our previous work, focused on microelectronics modeling issues. Regarding academic and scientific output we are quite satisfied. We are particularly proud of the number and quality of the doctoral and master's theses which have been completed this year.

We are pleased to report that our institute did extremely well in the evaluation process of the electrical engineering departments of Austria. We are entering the seventh year of our institute with considerable motivation.

Siegfried Selberherr was born in Klosterneuburg, Austria, in 1955. He received the degree of 'Diplomingenieur' in electrical engineering and the doctoral degree in technical sciences from the Technical University of Vienna in 1978 and 1981, respectively. Since that time he has joined the Technical University of Vienna as professor. Dr. Selberherr has been holding the 'venia docendi' on 'Computer-Aided Design' since 1984. He has been the head of the 'Institut für Mikroelektronik' since 1988. His current topics are modeling and simulation of problems for microelectronics engineering with particular emphasis on semiconductor devices.

Renate Winkler was born in Vienna, Austria, in 1960. She joined the 'Institut für Mikroelektronik' in November 1991. Since that time she has been in charge of the organizational and administrative work of the institute.

Ewald Haslinger was born in Vienna, Austria, in 1959. He joined the 'Institut für Mikroelektronik' in December 1991. Since that time he has been in charge of organizational, administrative and technical work of the institute.

Andreas Steidl was born in Herzogenburg, Austria, in 1965. He joined the 'Institut für Mikroelektronik' in September 1991. Since that time he has been in charge of all technical hardware and software work of the institute.

A Package for Capacitance Extraction

Robert Bauer

The package SCAP (Smart Capacitance Analysis Program) has been finished. The package consists of three input processors, the capacitance extractor, a visualization tool and a shell that collects all tools.

The first preprocessor is suited for two–dimensional cross section structures, for which it produces a triangular grid for the capacitance extractor. The second one utilizes the layered configuration of wiring structures. This preprocessor for layered structures reduces the cumbersome problem of three–dimensional geometry specifications to defining flat masks and nonplanar layers, since masks can be extracted from a layout description, and layers can be derived from cross sections (*i.e.* SEMS). The integrated gridder produces a tetrahedronal grid. The third preprocessor is based on hyperpatches. The user has to supply a crude grid based on distorted hexahedronal elements.

It is assumed that the conductor material has infinite conductivity. The conductors represent Dirichlet boundary conditions for the simulations. A finite element module is used to calculate the electrostatic field energy for several applied conductor potentials. From the computed energies and applied conductor potential the capacitances are extracted by solving a small system of linear equations. The energy method achieves a higher accuracy than the method of charge integration on the conductors.

The solver package has been extended and improved. It allows the user to choose between a Gaussian skyline solver and a preconditioned conjugate gradient method to solve the large linear system in order to obtain the potential distribution and energy. To reduce the fill in of the Gaussian solver a reverse Cuthill–McKee node ordering has been implemented.

For the whole capacitance extraction process, only one half of the compressed stiffness matrix is stored. The stiffness matrix is assembled only on the first run. This is possible by a right–hand–side matrix which stores the coefficients for the Dirichlet points. For each run calculating the energy the Dirichlet points are assembled from the right–hand–side matrix into the right–hand–side vector.

Additionally, our visualization tool which is able to visualize two– and three–dimensional potential distributions is extended to display a shaded conductor structure and to allow a non nested rotation of the objects. The deep sorting hidden line algorithm is extended and checks now all possible face arrangements to produce a correct display.

Robert Bauer was born in Vienna, Austria, in 1963. From 1983 to 1984 he was working in the support of medical analysis devices. In the course of his studies he has held various summer positions in the medical branch. He received the degree of 'Diplomingenieur' from the Technical University Vienna in electrical engineering in 1990. After seven months of industrial development of Brain Mapping Systems — a medical brain diagnostic device, in spring 1991 he joined the 'Institut für Mikroelektronik', where he is currently working toward his doctoral degree in the field of three-dimensional interconnect simulation of multilevel wired VLSI circuits. In spring 1993 he held a visiting research position at SONY, Atsugi, Japan.

Monte Carlo Simulation of Ion Implantation into arbitrary crystaline structures

Walter Bohmayr

Today ion implantation is the most important technique to introduce dopants into silicon. The miniaturization of semiconductor devices imposes an accurate description of the implantation profiles which depend on the properties of the ions as well as on those of the target. Thus, the consideration of special physical characteristics of crystaline structures is essential.

To meet all the requirements for realistic simulations two main goals had to be satisfied. First we developed geometry modules for arbitrary semiconductor device structures. Geometrical checks in two–dimensional targets are performed by using the slab method. The planar polygones are partitioned into slabs by cutting each vertex with a vertical or horizontal line. In this manner several convex sections, trapezoids and triangles, are created within each slab. To represent three–dimensional structures an octree is used for geometry discretization. The octree consists of cubes which are recursively subdivided into eight subcubes until either the desired accuracy of the discretization is reached or no intersection of the actually checked cube with the polygones defining the geometry exists. A cube is also a convex geometrical object and the point location problem can be solved trivially.

Crystaline targets with regular arrangements of atoms need

advanced physical models because the atom rows or planes line up so that there are long–ranging open spaces in which the ions can travel without significant scattering. Because of this the final ion distribution extends deeper into the target.

The advantage of our geometry routines can also be seen in the possibility of scaling the structures according to the grid spacing of the crystal. As each ion travels through the target, it undergoes a series of nuclear collisions and a fraction of its energy is transferred to a target atom, which is displaced from its original position. The resulting implantation damage is calculated by the modified Kinchin–Pease model. Its influence on ion trajectories in an originally crystaline layer is considered by employing the amorphous mode with a probability to the local number of displaced atoms.

Walter Bohmayr was born in Steyr, Austria, in 1969. During his studies of electrical engineering and computer science at the Technical University of Vienna he was employed with 'Austrian Industries' as a software engineer. In 1993 he received the degree of 'Diplomingenieur' in electrical engineering and joined the 'Institut für Mikroelektronik' in October 1993, where he currently is working towards his doctoral degree. His work is focused on physical models and algorithms for silicon oxidation and Monte Carlo ion implantation in process simulation.

The VISTA Grid Support Module

Franz Fasching

Through the PIF (Profile Interchange Format) Application Interface (PAI) the VISTA framework provides a unified way for TCAD applications to access and exchange information in the common PIF database. Due to the varying nature of TCAD tools accessing the database — ranging from simple maintenance tools to complex simulators written in various programming languages with different concepts in mind — the PAI has to be the "smallest common denominator" of all conceivable interfaces. On one hand it has to offer full and unrestricted access to PIF objects, yet it must not impose a specific memory representation of PIF data on an application, which makes writing a flexible PIF application sometimes a tedious and unpleasant task.

To overcome this situation the grid support module presents a well–defined yet opaque memory representation of PIF grids and attributes to the application through a simple and clear interface. It uses object oriented techniques to extend the PIF object model to in–memory objects and provides the application with a comprehensible and orthogonal set of creator, accessor, destructor and manipulator methods applicable to an in–memory PIF object through its unique object handle.

Although there are many advanced object–oriented programming languages available today, none of them is internationally standardized, therefore conflicting with the VISTA design principle of utmost portability. Because of this reason, the VISTA Object–Oriented Programming System (VOOPS) was created.

This enables the VISTA C programmer to use object–oriented programming techniques through specialized UNFUG (Universal Function Generator) constructs in his C programs. VOOPS only features a static class hierarchy and a single inheritance model, but thus effectively gains speed advantages over other more flexible run–time object–oriented programming systems. The static object model avoids searching the whole class hierarchy when sending a message to an object, since the class hierarchy is already known prior to compile time, and therefore statically encoded in a class method table.

Both the Unstructured Grid Support (UGS) as well as the generic interpolation support are part of the grid support module, since the notion of unstructured grid elements is ideally suited for a hierarchical class–model. While maintaining the conventional interface for traditional TCAD tools, the UGS in–memory objects are also used for point location to speed up interpolation on unstructured grids.

Franz Fasching was born in Steyr, Austria, in 1965. He received the degree of 'Diplomingenieur' from the Technical University Vienna in electrical engineering in 1989. In February 1990 he joined the 'Institut für Mikroelektronik', where he is currently working towards his doctoral degree. During February and March 1992 he held a visiting research position at SONY, Atsugi, Japan. His work is focused on the VISTA Technology CAD environment and improvement and extension of the capacitance simulator VLSICAP.

Simulation of Ring Oscillator Structures

Claus Fischer

For the increasing density of device components in integrated circuits, new technologies are constantly in development. It is necessary to evaluate these new technologies prior to and during their use in the fabrication process and device simulation.

A typical evaluation structure for a new CMOS technology is a ring oscillator. This structure can determine important technological parameters, such as the delay time of the inverter gates or the signal waveforms.

For the simulation of a ring oscillator structure which should give reliable values for these key parameters, condensed analytical device models that are built into many circuit simulation programs turn out to be too inexact. Numerical models with accurate data about the static and dynamic behavior of the circuit components are one of the minimum requirements. This data must be provided by device simulation (or by measurement). Coupled device simulation of the elementary parts proves an elegant method to circumvent the problems in creating these circuit models. Moreover, it yields a reliable description of the behavior of the CMOS inverter stages in connection with the nonlinear (capacitive) load.

One of the most important points in coupled device simulation is contact current integration. This integration must be implemented as part of the linear system which describes the device equations. Thereby implementing arbitrary combinations of voltages and currents as boundary conditions be-

comes a straightforward task, which leads to numerically stable schemes for solving equations.

As there is no natural and stable stationary solution of a ring oscillator due to the odd number of stages, the stationary solution from which the transient simulation starts must be obtained by special boundary conditions.

The simulation of a 9–stage ring oscillator in ultra low power technology with 18 MOS transistors uses 27000 variables and takes approximately 24 hours CPU–time for 1000 time–steps. The doping profiles of the transistors have been produced by process simulation within VISTA. The waveforms of the signals provide accurate and reliable informations about delay time and power consumption of the technology and show the influences of the technological differences of the n–MOS and p–MOS transistors.

Claus Fischer was born in Vienna, Austria, in 1967. He received the degree of 'Diplomingenieur' in electrical engineering from the Technical University of Vienna in 1989, and his doctoral degree in 1994. In January 1990, he joined the 'Institut für Mikroelektronik'. In summer 1992, he held a visiting research position at Motorola, Austin, Texas, USA. His work concerns the topic of device simulation in VISTA and the simulation of new structures within this TCAD framework, as well as numerical aspects of the coupling of simulation tools and the support required on integration of these tools.

Injection of Carriers from Silicon into Silicon Dioxide

Michael Hackel

In modern MOSFETs, shrinking dimensions result in more and more detailed theoretical investigations and simulations to produce reliable circuits and to improve their performance. Many assumptions have been made to explain the gate current characteristics of transistors in order to reduce degradation. Usually electrons are accelerated by the applied electric field and a very small number obtains kinetic energies in excess of two electron volts (eV). These hot carriers reaching the oxide interface are believed to have significant importance for the injection into silicon dioxide.

The energetic distribution of hot carriers in the channel is calculated by a Monte Carlo program. As only very few electrons reach the interface, an appropriate particle–split algorithm is employed. Once they reach the interface the probability of entering the oxide is determined by the Wentzel–Kramers–Brillouin (WKB) approximation. This quantum mechanical approach accounts for tunneling that enables carriers to be injected whose energies are lower than the barrier height of the semiconductor-oxide interface. If the electron proceeds into the oxide, another Monte Carlo simulator is used to describe the physical behavior of the electrons in the oxide.

Combining semiclassical approaches with quantum mechanical probabilities of injected particles raises several questions about its validity. Nonetheless, first simulations demonstrate

that further quantum effects become non-negligible if the insulating film comprises less than 10 nanometer (nm). In this case only calculations including the full quantum mechanical nature of electrons will give the correct results. As far as it is known, the occurrence of only ballistic transport in silicon dioxide is important for films smaller than $5nm$ if the electrons do not suffer collisions while they are passing the oxide. A Monte Carlo simulator cannot account for these conditions any longer, but then it might be sufficient to calculate the injection probability of carriers into the gate only with a Schrödinger solver.

The theoretical model for electron injection will be tested on real MOSFET devices and compared with experimental data. As it is believed that hot electrons in the channel of the semiconductor also have a strong impact on trapping/detrapping effects in the oxide and at the interface, degradation of the device, leakage effects on drain currents due to crystal defects, tunneling, impact ionization and interface charge formation, work is underway to study these effects that can lead to damage of electronic devices, especially if future devices become ultracompact.

Michael Hackel was born in Vienna, Austria, in 1965. He studied technical physics at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1991. During his studies he worked on projects in solid state physics and quantum field theory. He joined the 'Institut für Mikroelektronik' in January 1992. He is working towards his doctoral degree. In summer 1994 he held a visiting research position at the 'Dipartimento di Elettronica, Informatica e Sistemistica' at the University of Bologna, Italy. His scientific interests include solid state device technology, device modeling and physical aspects of semiconductors in general.

The VORONOI Re-Gridding and Interpolation Service

Stefan Halama

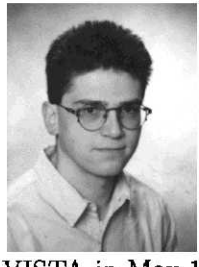
Geometry–conforming re–gridding and efficient interpolation are key methodologies for a robust coupling of independently developed process simulation tools, each neglecting issues which are not of primary concern to the specific models of the respective tool.

As a part of the VISTA framework, the VORONOI re–gridding and interpolation service provides this grid-oriented functionality for the two-dimensional case. It creates a geometry–conforming grid by re–triangulating merged point clouds of existing input grids which need not conform to the geometry of the current wafer state. The generation of the mesh is accomplished by several modules which perform quadtree–based point storage, point cloud generation, boundary refinement, Delauney triangulation, mesh/geometry association, and interpolation of attributes. In the general case, only a subset of the resulting grid points carry attribute values. Reasonable attribute values for all other grid points can be found by solving the biharmonic equation on the supergrid. Special care has been taken to ensure that the algorithmic complexities of all modules of VORONOI do not exceed $O(N \cdot \log(N))$. It is expected that the basic grid generation method can be generalized to the three–dimensional case.

To simulate a fully planarized $0.25\mu m$ CMOS process using shallow trench isolation, the PROMIS Monte Carlo module

for the simulation of ion implantation, the cellular etch and deposit simulation module of PROMIS, and TMA's TSUPREM-4 must be used alternatively. The Monte Carlo module creates the doping profiles on a single tensor–product grid which extends over all segments of the geometry. TMA's TSUPREM-4 requires doping profiles defined on multiple, segment–conforming, triangular grids. The PROMIS etch simulator alters just the geometry and hence often leaves the associated grid and doping information in an inconsistent state. In a sequence consisting of 38 simulation steps, VORONOI has been used repeatedly to resolve all problems arising from the different abstractions and conflicting representations employed by these simulators.

The modular architecture of VORONOI facilitates future extensions. Adding a coarsening module which removes redundant points from grid point cloud will improve the performance of tools integrated into VISTA, especially during long simulation sequences. Initial grid generation for process and device simulation can be provided by adding a point cloud generation module.



Stefan Halama was born in Vienna, Austria, in 1964. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1989. During his studies he was with several Austrian companies where he worked on software development projects in the CAD and computer graphics field. He joined the 'Institut für Mikroelektronik' in September 1989, where he finished his doctoral thesis on VISTA in May 1994. In winter 1991 he held a visiting research position at Digital Equipment Corporation, Hudson, Massachusetts, USA. His research interests include process simulation, automatic grid generation, TCAD frameworks, tool integration, visualization and software technology.

Electronic Properties of III–V Semiconductor Alloys

Christian Köpf

Device simulation of modern heterostructure field effect transistors (HFETs) is a challenging topic due to their small physical dimensions and the two–dimensionality of carrier transport. Monte Carlo calculations are the most accurate in dealing with these problems but, for a practical device simulator, they consume too much time and resources. Therefore, other methods for solving the transport equations must be applied, usually drift–diffusion or hydrodynamic approaches. It is important to characterize the electronic properties such as the carrier mobility which is closely related to the band structure of the bulk semiconductor.

Mixing III–V binary compounds (GaAs, InAs, AlAs, InP) to ternary alloys (*e.g.* $In_xGa_{1-x}As$) is a convenient method for adjusting the band gaps in a favorable range (band structure engineering) since the band edges as well as most basic physical parameters depend on the alloy composition x. Usually this dependence is well approximated by low order polynomials of x. Besides the well–known lattice–matched GaAs/AlGaAs system, the lattice constants of the layers forming the device can be significantly different, and biaxial strain is introduced in the active regions (channel and spacer layers) grown on top of the substrate. Below a critical thickness, at which the strain can be accommodated by the lattice through elastic distortion without generating dislocations, the growth is called pseudomorphic. This gives another degree of freedom for the hetero-

junctions since the strain changes the band edges by shifting the absolute minima and lifting the degeneracy of the upper conduction bands L and X, which can be described by the deformation potential formalism. Secondly, it distorts the constant energy surfaces changing the longitudinal and transversal masses of each valley and the mobility becomes anisotropic, the in–plane value can exceed the perpendicular component.

As a first guess for the low field mobility the scattering rates (momentum relaxation rates) of the individual scattering processes are added by implying they are elastic and independent. Polar optical phonon scattering, which is the predominant scattering mechanism at room temperature, is inelastic and therefore only an expression extracted from an approximative solution of the Boltzmann equation is used. This method can be applied successfully only to the isotropic case *e.g.* the Γ–band. Monte Carlo calculations are employed to extract useful expressions which also account for nonparapolicity and nonspherical energy bands. The overall mobility is obtained by weighting the mobility by the electron population of the bands which can be modeled as a function of the electric field or the carrier temperature.

Christian Köpf was born in Vienna, Austria, in 1968. He studied Communications and Radio–Frequency Engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1993. He joined the 'Institut für Mikroelektronik' in November 1993, where he is currently working towards his doctoral degree. His scientific interests include heterostructure devices, device modeling and solid state physics in general.

Nonlinear Electron Transport in the Quasi Two-Dimensional Electron Gas

Hans Kosina

Field effect transistors (FET) have gained wide spread application in electrical engineering. Apart from the MOSFET which can be seen as the work horse in today's VLSI technology, the high electron mobility transistor (HEMT) has become increasingly popular, mainly because of its high frequency and low noise properties. Usually, in these FET devices a thin layer of mobile charge, which can either be formed at a semiconductor/insulator interface or at a heterojunction, is controlled by a gate electrode. Because of the strong confinement of the carriers their motion is quantized in one dimension, and the conduction band splits into a system of discrete subbands.

This project deals with the numerical study of the transport properties of a quasi two–dimensional electron gas (Q2DEG). A major prerequisite for such a transport calculation is an accurate knowledge of the subband structure of the Q2DEG. A numerical solver for the coupled Schrödinger and Poisson equations is developed which yields the eigenstates of the electrons and the shape of the confining potential. The matrix elements of the various scattering mechanisms are then consistently calculated from the electron wave functions. A key issue is the treatment of non–parabolic conduction bands as they have strong impact on high–field transport. Because space representation is no longer applicable to the Schrödinger equation we have chosen a representation in which the kinetic–energy operator has diagonal form. Currently we are developing a

multi–subband Monte Carlo program for the AlGaAs/GaAs material system. The number of subbands included in the calculation is a configuration parameter and not limited to a low number.

Another project deals with the transport of hot holes in bulk semiconductors. The physical model comprises the heavy and light hole bands that are degenerate at the Γ–point. The bands are represented by series of spherical harmonics. Each coefficient of this expansion may depend on the magnitude of the wave vector in a different way. Therefore, a numerically given density of states can be incorporated as well as anisotropy to an arbitrary high order. Due to the p–like symmetry of the valence band wave functions the overlap integrals strongly depend on the scattering angle. Proper models for the overlap integrals are included in the Monte Carlo program.

Hans Kosina was born in Haidershofen, Austria, in 1961. He received the 'Diplomingenieur' degree in electrical engineering and the doctoral degree from the Vienna Technical University in 1987 and 1992, respectively. For one year he was with the 'Institut für flexible Automation', and in 1988 he joined the 'Institut für Mikroelektronik' at the Vienna Technical University. In summer 1993 he held a visiting research position at the Advanced Research and Development Laboratory at Motorola, Austin, Texas, USA. Currently he is employed as an assistant professor in the device modeling group. His current interests include physics and technology of solid state devices and integrated circuits.

Simulation of Micro–Structures

Erasmus Langer

Since the technologies in all areas of electronics continue to evolve, numerical simulation of micro–structures that are playing the dominant role in the broad field of microelectronic devices is becoming increasingly important. Though the most widespread representatives are ultra large scaled integrated (ULSI) semiconductor devices, there also exist various other devices which are based on micro–structures, such as the surface acoustic wave (SAW) devices.

The simulation of micro–structures is based on the solution of partial differential equation (PDE) sets with adequate boundary conditions. Nevertheless the types of involved partial differential equations strongly depend on the given kind of micro–structure and their derivation is not at all a straightforward process: As an example, submicron MOS transistors can be simulated successfully by solving the well known fundamental semiconductor equations (although with sophisticated models for the physical parameters only) which consist in the time dependent case of the elliptic Poisson equation and the parabolic continuity equations. With decreasing feature sizes numerous second order effects must be taken into account, thus, the starting point of the derivation of the mathematical model for current flow is the Boltzmann equation in the phase space. On the other hand the problem of excitation, propagation, and detection of electro–acoustic waves requires a simultaneous solution of the Poisson equation and the equations of motion which belong to the hyperbolic PDE type.

For the simulation of micro–structures not only their different types but also several substrate materials have to be distinguished. Although a different material enters the mathematical formulation through the models for the physical parameters only and does not affect the PDE structure it may be necessary to redesign the algorithm for the numerical solution. As an example the implementation of the physical parameters of silicon is not directly suitable for gallium arsenide.

A very interesting problem to be tackled is represented by a micro–structure which combines semiconductor devices and SAW devices on one chip. For example, such a chip consists of a SAW filter and the surrounding electronic circuit. In this instance the parasitic effects, such as carrier flow in the filter domain and wave propagation in the area of semiconductor devices, have to be investigated rigorously since the substrate material is a piezoelectric semiconductor. The solution of the underlying mathematical model — a PDE set of elliptic–parabolic–hyperbolic type — is an ambitious challenge.

Erasmus Langer was born in Vienna, Austria in 1951. After having received the degree of 'Diplomingenieur' from the Technical University of Vienna in 1980 he was employed at the 'Institut für Allgemeine Elektrotechnik und Elektronik' first as a research assistant and then as assistant professor. In the beginning, his research field was the numerical simulation of semiconductor devices and later the excitation and propagation of electro–acoustic waves in anisotropic piezoelectric materials in which he also received his doctoral degree in 1986. In 1988 he joined the newly founded 'Institut für Mikroelektronik'. Currently he works mainly in the field of simulation and analysis of micro–structures with emphasis on ultra large scaled integrated semiconductor devices and acoustic wave devices.

Three–Dimensional Simulation of Dopant Diffusion in Nonplanar Structures

Ernst Leitner

Due to the increasing packing–density in semiconductor device design the influence of three–dimensional effects gain more and more importance. Therefore modern process simulators must be capable of handling complex three–dimensional structures consisting of several materials.

To solve the partial differential equations which describe dopant diffusion, it is necessary to find an appropriate discretization of space and time. Whereas the time domain can be simple discretized, the spatial discretization offers many difficult problems. In general, good approximations to the real solution can only be obtained using a well–defined grid.

The grid has to resolve the geometry of the spatial domain as well as the dopant distribution. Usually the geometry can be resolved by comparably few elements. On the other hand the dopant distribution varies quite heavily, so that very small elements are necessary for accurate resolution. Furthermore, distortions of the element–shapes should be avoided because they cause systems of bad conditioned equations. And finally, the overall number of elements should be kept as small as possible. In order to comply with these requirements the basic concept deals with recursive refinement of the elements that are necessary for geometry resolving. But the refinement strategy has to preserve the quality of elements in order to avoid distortions of bad elements. The chosen method refines a given tetrahe-

dron into four small tetrahedrons, located at the corners, and the remaining octahedron. For recursive refinement the octahedrons are split into 6 small octahedrons once again placed at the corners of the parent element, and 8 tetrahedrons filling the remaining leaks. These small tetrahedrons have the same shape as the original "grandparent" tetrahedron.

At the boundaries between two materials, a left– and a right–sided value is necessary to account for segregation effects. Such boundary conditions are treated by special triangular prisms with zero height, which allow arbitrary boundary conditions to be modeled.

Through the redistribution of the dopants, the grid has to be refined adaptively. After each time step the gradient errors of the approximating solution are estimated and build the basis for element refinement.

On these grids the nonlinear partial differential equations describing the diffusion equations are approximated by the finite element method. Linear shape functions and a standard Galerkin weighting are used. For better convergence of the Newton iteration scheme, the full Frechèt derivative of the residual function is used as linear system matrix. The linear system is solved iteratively by a bi–conjugate–gradient–stabilized solver (BiCGStab).

Ernst Leitner was born in Gmunden, Austria, in 1968. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1992. He joined the 'Institut für Mikroelektronik' in January 1993. He is currently working towards his doctoral degree. His research interests focus on three dimensional process simulation, numerical grid generation, and the basic physics of transport phenomena in solids.

Process Flow Representation and Design Automation

Christoph Pichler

The VISTA Simulation Flow Control module (SFC) was implemented and integrated into the framework as the main controlling instance for a variety of multistep simulation experiments, allowing for the point–and–click definition of simulation flows, the automatic parallel execution of these tasks, the detection of split points to avoid recalculation, and the capability to log, store, and retrieve all output and error messages generated by tools called during a simulation run. Extensive experiments modeling a complete $0.5\mu m$ low power CMOS process as well as a $0.25\mu m$ planar CMOS process involving a sequence of PROMIS and TMA's SUPREM-4 tool calls led to new insights into the requirements on the PIF–based wafer state representation that is used for data exchange between process simulation tools.

Simulation flows are built from a set of available process simulation tools using a graphic editor supporting hierarchical flow structures. To support the incremental and iterative design methods most widely exhibited by process design engineers, split points do not need to be defined in the flow, but they are automatically detected when a statement is reached that has not been executed before. A split tree is thus generated and stored in the file system that accurately reflects the designer's work. All results and diagnostic messages of each step of any branch of the tree remain available for analysis at a later

time. The automatic generation of split trees by Design–of–Experiment (DoE) methods is in preparation.

To reach the goal of a completely integrated semiconductor process and device design framework, a number of issues will be addressed in the future that are currently supported only half–heartedly. The most important ones (on the system–side of the framework) appear to be a tool control layer supporting automatic queueing, scheduling, and logging features, and a tool integration unit allowing for high–level descriptions of simulation tools to make available to the framework as well as automatic user interface generation from such descriptions. On the user–side, more attempts will be made for an accurate reflection of the design process, especially with respect to lithography mask data representation and automatic large scale experiment management.

Christoph Pichler was born in Vienna, Austria, in 1966. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1991. During his studies, he held several summer trainee positions at electrical engineering companies in Austria and Switzerland. In November 1991, he joined the Engineering Design Research Center at Carnegie Mellon University in Pittsburgh, Pennsylvania, where he worked on rapid prototyping and automation in manufacturing. He joined the 'Institut für Mikroelektronik' in November 1992 and is currently working towards his doctoral degree. His scientific interests include engineering design, semiconductor technology, and system integration

Two–Dimensional Diffusion Simulation in Multilayer Structures

Helmut Puchner

During the last years it has become increasingly necessary to simulate the whole fabrication process of a semiconductor device. Single process step tools are quite necessary, but they can not provide a realistic input for the subsequent device simulation. Unfortunately, the requirements of new tools which are integrated in a whole process simulation line are much higher as in stand alone versions. The simulators must be capable of handling multilayer structures of arbitrary geometries, different dopant species, arbitrary computational grids and discretization methods, and several physical models.

At the moment the diffusion module of our two–dimensional process simulator PROMIS deals with transformed orthoproduct grids and a finite difference discretization method. Several physical models for the dopants are available *e.g.* clustering, pair diffusion or coupled diffusion. The physical PDEs are solved in the substrate region. To also handle multilayered structures new grid generation techniques are developed with extreme effort. The public domain grid generator TRIGEN was built in our VISTA framework and equipped with a PIF interface. Also special features were added to support the waferstate treatments.

The grid generator TRIGEN generates a triangular grid by only considering the geometric information. Boundary connectivity between different regions is also successfully treated

as automatic scaling in triangle size. Since the grid is a geometry conformity, grid refinements have to be applied to get a dopant conformity grid. The so–called "red" and "green" refinement techniques are used for splitting grid elements to get a higher resolution of the grid. The decision as to whether a grid element should be split or not is given by conventional gradient and dose criteria.

Another important task in simulation of diffusion processes is the modeling of the physical effects (*e.g.* clustering, segregation) by means of numerical methods. In multilayered structures the segregation kinetics is one of the major mechanism for dopant flux from one region into another. Within our polysilicon diffusion model we simulated the out–diffusion of dopants from the poly–Si layer into the mono–Si layer by means of segregation. Thereby we built in a model for multilayer diffusion, where we used different PDE coefficients for different layers according to their material properties.

Helmut Puchner was born in Steyr, Austria, in 1968. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1992. He joined the 'Institut für Mikroelektronik' in October 1992. He is currently working towards his doctoral degree. From 1988 to 1990 he held summer positions in Switzerland and Germany working on control engineering. His research interests include process simulation in poly–crystaline silicon, general diffusion processes and implementation details of the process simulator PROMIS into the VISTA framework.

A Flexible and Extensible Data Front End for PIF

Gerhard Rieger

The PIF editor (PED) is part of the VISTA framework and a powerful tool for creating and modifying device geometries and specifying their physical properties. It uses PIF for reading and writing data from and to files, but internally makes use of a more flexible list oriented data representation with explicit references and back–references, called C–List–Support (CLS).

The PIF editor has been enhanced with an extendable user interface by combining it with the XLISP interpreter. Its configuration and user interaction is now completely handled by LISP functions, while low level functionality is still implemented in C.

All user inputs like mouse button clicks or menu entry selections trigger call–backs with event information in the form of text strings or LISP expressions which are, for the mouse buttons, context–dependent. Input strings may as well be typed in via a text window which is part of the PIF editor application. During event processing strings are interpreted as LISP expressions. The PIF editor tries to evaluate these expressions; if it succeeds it continues with the result, otherwise it uses the original expression.

The output of the previous stage is then used as input to an infinite state machine. This state machine looks — depending on its rules and its current state — for the appropriate actions. These actions may be arbitrary LISP expressions; especially

interesting are combinations of CLS data manipulations and graphic commands. After the action has been performed the state machine changes the user interface context based on the new situation.

LISP files may be loaded during startup as well as at runtime to add functionality. These files may add LISP functions, menus and menu entries, or rules for the state machine. So it is possible to configure the PIF editor to ones' needs, for example a process engineer need not overload his menus with device simulation specific menu entries, but instead could load code to interactively invoke a particular grid generator.

The latter is managed by the PIF editor's new feature to invoke external executables. With some means to assemble and combine interactive and configuration data all command line parameters can be generated and a process can be spawned similar to the VISTA shell. The changes caused on the PIF file are read and displayed by the PIF editor afterwards.

Gerhard Rieger was born in Vienna, Austria, in 1963. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1991. He joined the 'Institut für Mikroelektronik' in December 1991, where he is currently working towards his doctoral degree. His research interests include programming languages and compilers, software technology, geometry, and visualization.

Ultra–Low–Power CMOS Technology

Gerhard Schrom

In traditional integrated circuit (IC) design the supply voltage has been fixed to $5V$ mainly to maintain compatibility with the transistor–transistor logic (TTL) levels. However, this high voltage causes problems in down–scaling the devices due to high electric fields and because of the increased heat generation per area. By a drastic reduction of the supply voltage V_{DD}, even below $3.3V$ or $2.5V$, which are currently taken as the "low–power voltages" the power consumption could be reduced by orders of magnitude and would also reduce if not eliminate several common problems such as hot carrier injection. On the other hand, the circuit speed is also reduced, but this effect can be largely compensated by applying parallelism in the systems design while still achieving a large reduction of the power consumption. In order to accomplish this the first step was to verify the feasibility of the concept of ultra–low–power CMOS and to determine the lower limits for the supply voltage and to find out first guidelines for process and device design.

The processes under consideration are recessed–well dual–gate processes with a very thin gate oxide ($5nm$ and below) to obtain controllably low threshold voltages. The source/drain doping is formed by a single ion implant after the formation of a narrow sidewall spacer which also controls the S/D overlap capacitances. The most critical points are threshold voltage control and good subthreshold behavior which in turn determines the actual lower limit of the supply voltage because the

maximum achievable ratio of I_{on}/I_{off} is limited by $e^{V_{DD}q/kT}$ and indirectly affects the noise immunity. Therefore, the devices are operated in the transition region between weak and strong inversion to achieve high noise margins and speed at the same time. The analysis uses process and device simulation to obtain the device characteristics which are then used for a table–driven circuit simulation of basic logic circuits such as inverters and gates in static and dynamic logic.

For the evaluation of the results the noise margins $NM_{H,L}$ of NAND gates with a fan–in of three and the ratio of maximum and minimum clock frequency f_{cmax}/f_{cmin} were taken for static and dynamic logic respectively. With $NM_{H,L} > 0.1V_{DD}$ and $f_{cmax}/f_{cmin} > 100$ the lower limits of the supply voltage were found to be $200mV$ for static logic and $500mV$ for dynamic logic at $T = 300K$.

Up to now basic work to determine the prospects and the limitations of ultra–low–power CMOS has been done. Further research has to be done to obtain systematic guidelines for design and optimization according to the systems' constraints to make effective use of ultra-low-power CMOS technology.

Gerhard Schrom was born in Mödling, Austria, in 1963. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in March 1992. During his study he was working on software development projects in the CAD field. He joined the 'Institut für Mikroelektronik' in April 1992, where he is currently working towards his doctoral degree. His research interests include device and circuit simulation, circuit design and synthesis, signal and image processing, and TCAD framework aspects. In spring 1994 he held a visiting research position at HITACHI, Tokyo, Japan.

Simulation of High Electron Mobility Transistors

Thomas Simlinger

Recently, the HEMT (high electron mobility transistor) has become a widely used supplement in the spectrum of industrial semiconductor devices. Pseudomorphic submicron HEMTs especially have conquered a broad field of application because of their high–frequency performance. Compared to the simulation of simple MOS devices, several additional requirements have to be met before a HEMT transistor can be analyzed.

The partial differential equations which describe the current transport phenomena have to be extended to inhomogeneous density of states and band edge offset energies. This is necessary to study structures consisting of arbitrary materials, given as a general material description. Graded junctions and compound materials can thereby be consistently treated.

The small dimensions of heterojunction devices in connection with the typical materials used in these devices require a hydrodynamic set of equations, including a carrier temperature equation. This allows the carrier heating in the channel to be described correctly, which is the most limiting effect determining current transport in the normal operation regime.

A consistent discretization of the material interfaces at the heterojunctions requires doubly–valued points at the heterointerface, where two separate values describe the situation on both sides of the interface. These values are connected by arbitrary functional forms. Coupled solutions of all quantities in all re-

gions of the device are necessary, since the mutual influence of the regions is very strong.

The mobility modeling for GaAs-based HEMT structures must account for the special two-band situation in these devices. The distribution of carriers among the bands (Γ, L and X-band) is primarily determined by the local carrier temperature and by the energetic distance of these bands.

The HEMT is a purely electron-based device; holes do not influence the device behavior in any way. This is one difference when compared to the MOS–transistor, which is caused by the fact that in the HEMT the channel is bounded by energy barriers, and the insulating properties of intrinsic gallium–arsenide are sufficient for suppressing high substrate currents. The electron mobility in the channel is the major factor which determines the device characteristics in the normal operation regime; for high gate voltages a drift zone under the drain beneath the heterojunction in that part of the device leads to saturation of the drain current. Even higher gate voltages enable the formation of a parasitic channel, which is parallel to the original channel and has bad electric properties (low mobility). The device is therefore not used in this mode of operation.

Thomas Simlinger was born in Mödling, Austria, in 1963. He studied communication engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1992. He joined the 'Institut für Mikroelektronik' in October 1992, where he is currently working towards his doctoral degree. His scientific interests include algorithms and data models, device modeling and physical aspects in general.

Scalability and Verification of the Circuit Model for Vertical DMOS Transistors

Martin Stiftinger

One of the major advantages of the vertical concept of DMOS (Doubled Diffused MOS) power transistors is — besides the low on–resistance per unit area of a single cell in comparison to lateral power transistors — the possibility to put a large number of cells in parallel. Because of the thermal stability (the current decreases with increasing temperature due to a lowered mobility) of MOS devices a self–stabilizing uniform current distribution among the cells is guaranteed. This allows flexibly to vary the on–resistance and the current capabilities of a DMOS transistor by simply changing the number of cells.

For circuit simulation a model is desirable, which is scalable to a different number of cells. In other words, the only model parameters which should have to be adjusted for a transistor with a specific number of cells are those describing the arrangement of the cells within the transistor. In our case this are three parameters, namely the number of rows per block, the number of columns per block and the number of blocks the DMOS transistor consists of.

In the analytical DMOS model, which was developed as a subcircuit, all elements were especially designed for the DMOS structure. The subcircuit consists of a MOS model describing the channel, a JFET model with drift velocity saturation and a resistor describing the drift–region, a strongly nonlinear gate–drain capacitance model, and some parasitic elements de-

scribing the reverse bias behavior of the transistor. As they are physically based, they also include the geometry of the DMOS cell. This and the knowledge of the arrangement of all cells in the DMOS transistor are the prerequisites for extending all element models for a varying number of cells.

The only difficulty is the treatment of the border cells of the DMOS transistor as the border regions differ essentially from the inner regions between two cells. In the JFET region the current saturation effect is much smaller than in the inner regions. This is solved by putting a second JFET model with different parameters in parallel to the first one. The first JFET model is scaled with the inner area of the device the second one with the border area.

Finally the model parameters have been extracted. A comparison of the DC– and AC– characteristics of the DMOS model with measurements for various numbers of cells have shown very emphasizing results. Both the model itself and the scalability have also been verified in simulations of typical power circuits including analog control circuits, which require higher accuracy of the models than switching applications.

Martin Stiftinger was born in Linz, Austria, in 1964. He received the degree of 'Diplomingenieur' from the Technical University of Vienna in 1989 in electrical engineering. In February 1990 he joined the 'Institut für Mikroelektronik', where he first was concerned with the iterative solution of large, sparse, and nonsymmetric linear systems and vectorization of those algorithms. He is working towards his doctoral degree, now focusing his work on device and network simulation of DMOS and high voltage CMOS transistors. His research area includes also parameter extraction and fitting strategies. In spring 1993 he held a visiting research position at the Philips Research Laboratories in Eindhoven, the Netherlands.

Three–Dimensional Models and Algorithms for Wafer Topography Evaluation

Ernst Strasser

Topography simulation offers the possibility of understanding the time evolution of topographical features in advanced device structures. As the device dimensions are reduced further three–dimensional models and algorithms are increasingly necessary for wafer topography evaluation.

A method for general three–dimensional surface advancement has been developed and coupled with models for etching and deposition. This method is based on morphological operations derived from image processing which are performed on a cellular material structure. We use an array of cubic cells, where each cell is characterized as etched or unetched. A linked surface cell list stores dynamically array addresses and rate information of exposed material cells. To advance on the surface, a structuring element whose spatial dimensions are related to the local etch or deposition rate is applied for the exposed cells. Depending on the simulated process, either material cells are removed or added which are located within the structuring element. Usually, for anisotropic three–dimensional surface advancement structuring, elements are ellipsoids, for isotropic movement of surface points, structuring elements are spheres. The material surface is finally described by the exposed sides of material cells that are in contact with vacuum cells.

The etch or deposition rate distribution along the exposed surface is obtained from macroscopic point advancement models

which use information about flux distributions and surface reactions of directly and indirectly incident particles. As a basic concept we consider a linear combination of isotropic and anisotropic reactions to calculate the resulting velocity vector. The isotropic reaction is mainly a chemical reaction affected by a reactive gas, in which the reactive particles have short mean free paths compared to the device dimensions and move randomly. The anisotropic reaction is a physical or chemical reaction, where the particles have long mean free paths and angular particle flux distributions must be taken into account. To calculate the incident particle flux at a surface point a spherical coordinate system is assumed and the region above the wafer is divided up into several surface patches. The incident flux is then integrated over those patches which are visible from the surface point. To determine if a surface patch is visible from a point on the surface, a shadow test has to be performed along a given direction which, within the cellular structure, is simply a matter of following a discretized line of cells from the surface cell to the boundary of the simulation area. The calculation of the visible solid angle of a surface cell needed to calculate the incident particle flux both in etching and deposition is therefore reduced to a series of shadow tests.

Ernst Strasser was born in Salzburg, Austria, in 1966. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1991. In January 1992 he joined the 'Institut für Mikroelektronik', where he currently is working towards his doctoral degree. His work is focused on process simulation, especially on algorithms and mathematical models for three–dimensional simulation of etching and deposition processes in integrated circuit fabrication. In summer 1994 he held a visiting research position at Motorola, Austin, Texas,USA.

The TIF Wrapper

Walter Tuppa

All process simulators developed at the Technical University of Vienna can be used under the VISTA project within the Simulation Flow Controller (SFC). Since currently not all process steps can be simulated by internal simulators, there is a need to allow usage of external simulators not developed in Vienna. One early example was the sample wrapper SAMWRAP for SAMPLE of the University of Berkeley.

To allow a full process simulation under the SFC, a binding to the TSUPREM-4 process simulator of Technology Modeling Associates (TMA) was built for VISTA. The TIF (Technology Interface Format) wrapper takes a PIF binary input file with a geometry and attributes (mostly doping profiles) defined on a triangular grid (*e.g.* generated by the VISTA VORONOI gridding and interpolation tool) and converts it to a SUPREM-4 save file (used by older versions of TSUPREM-4) or a TIF input file which is known by the new versions of all TMA simulation tools. The TIF file format is quite similar to the older TSUPREM-4 save format but has some enhancements in material and flow information. In addition to the PIF file an input deck is needed for simulation. This must be provided from an external source like the SFC. After finishing the simulation the output is converted back into a PIF binary file that can be used for further processing within VISTA.

The TIF wrapper uses the VISTA material database to convert the materials found in the segment descriptions of the PIF binary file to a material known by TSUPREM-4. If a mate-

rial is unknown by TSUPREM-4 the TIF wrapper looks for a super material of the PIF material to match a TSUPREM-4 known material. This method can lead to a problem because on back conversion the material from TSUPREM-4 is used for generating the segment description in the output PIF binary file and some information may be lost.

The input attributes defined on the input grid are converted only if they are known by TSUPREM-4. An internal conversion table is used for attribute type translation. This table holds the units which have fixed values under TSUPREM-4, but may be given different units on the PIF binary files. Unknown attributes are silently discarded during conversion.

On output the TIF wrapper generates a PIF binary file with all information from the TSUPREM-4 output file. The geometry is converted back into a PIF geometry. The attributes are written on different grids for each segment, because doping values may be different on material boundaries. All information from a TIF file can be converted into the PIF binary file although not all information may be used by the following simulators. The VISTA visualization now supports simultaneous display of multiple attributes (*e.g.* all attributes of one type, but defined on different segments).

Walter Tuppa was born in Vienna, Austria, in 1966. Having received the degree of 'Diplomingenieur' in computer science from the Technical University Vienna in 1991 and in electrical engineering in 1992, he joined the 'Institut für Mikroelektronik' in July 1991. His scientific interests includes all aspects of developing software within the VISTA project. At present, he is working towards his doctoral degree in electrical engineering. In summer 1993 he held a visiting research position at National Semiconductors, Santa Clara, California, USA.

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