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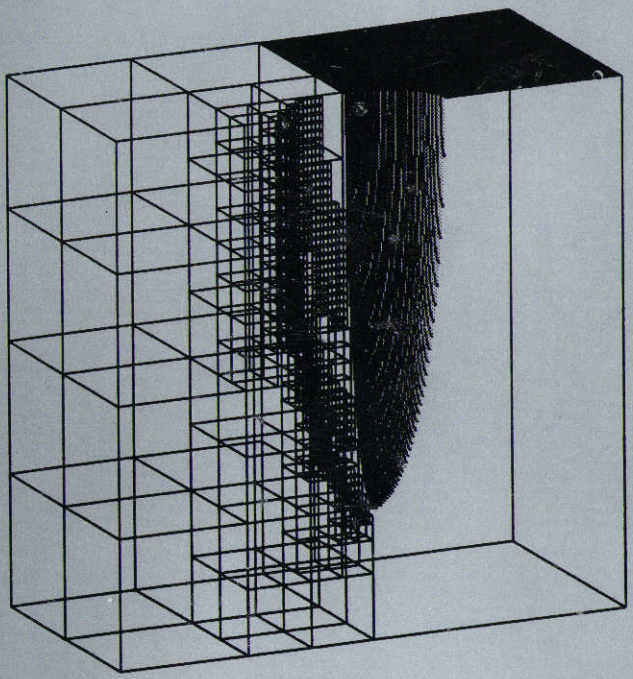

Annual Review
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Preface

Siegfried Selberherr

This brochure is the fifth annual research review of the institute for microelectronics. The staff supported by the Austrian Ministry of Science and Technology consists presently of eight full time employees: the head of the institute, four scientists, a secretary and two technical assistants. Fifteen additional scientists are funded through scientific projects!

We have begun to participate on scientific projects initiated within the European Community. In particular, we are cooperating on two ESPRIT projects, namely ADEQUAT [1], funded by the Austrian 'Forschungsförderungsfonds für die gewerbliche Wirtschaft', and MANPOWER [2], refunded by Siemens, Munich, Germany. Note, since Austria represents an EFTA country, we cannot receive funds directly from the EC. We are also glad to report that two additional industrial partners, namely 'Hitachi' in Tokyo, Japan, and 'Philips' in Eindhoven, the Netherlands, directly support our institute.

The projects of the institute are, in a continuation of our previous work, focused on microelectronics modeling issues. We still assume that integrated "Technology Computer-Aided Design" (TCAD) plays a significant role for the development of the next generations of devices for "Ultra Large Scale Integrated" (ULSI) circuits. The "Viennese Integrated System for Technology CAD Applications" (VISTA) which has been intensively worked on during the last three years, is now available to our industrial partners, and we have received significant positive

[1] Advanced Developments for 0.25μm CMOS Technologies
[2] Manufacturable Power MMICs for Microwave Systems Applications

and motivating feedback. We shall try our best to keep pace with the requirements of the industry, and we are looking forward to the sixth year of our institute.

Siegfried Selberherr was born in Klosterneuburg, Austria, in 1955. He received the degree of 'Diplomingenieur' in electrical engineering and the doctoral degree in technical sciences from the Technical University of Vienna in 1978 and 1981, respectively. Since that time he has joined the Technical University of Vienna as professor. Dr. Selberherr has been holding the 'venia docendi' on 'Computer-Aided Design' since 1984. He has been the head of the 'Institut für Mikroelektronik' since 1988. His current topics are modeling and simulation of problems for microelectronics engineering.

Marion Kaltenbrunner was born in Vienna, Austria, in 1972. She joined the 'Institut für Mikroelektronik' in November 1991. Since that time she has been in charge of organizational and administrative work of the institute.

Ewald Haslinger was born in Vienna, Austria, in 1959. He joined the 'Institut für Mikroelektronik' in December 1991. Since that time he has been in charge of organizational, administrative and technical work of the institute.

Andreas Steidl was born in Herzogenburg, Austria, in 1965. He joined the 'Institut für Mikroelektronik' in September 1991. Since that time he has been in charge of all technical hardware and software work of the institute.

Capacitance Extraction of Three-Dimensional Wiring Structures

Robert Bauer

The parasitic effects of interconnection wiring are gaining a significant importance in the speed of modern VLSI circuits. One of the reasons interconnections limit their performance is the wiring capacitance. With increasing chip dimensions and decreasing feature size, parasitic interconnection capacitances dominate the gate capacitances of the MOS transistors.

To extract the partial capacitances of three-dimensional wiring structures we have developed a program based on the finite element method to compute the electrostatic field for the energy calculation. The post-processing part of the program extracts the partial capacitances from the energy values and the applied conductor potentials.

The most critical part of this work is the grid generation method. In two dimensions well established grid generation methods for unstructured grids exist. Our approach uses a predecomposition in hexahedronal hyper-elements which will be automatically split into smaller elements. To prevent numerical integration of the element stiffness matrices, a special algorithm splits (under the restriction of keeping up the right connectivity) the hexahedronal elements into tetrahedronal elements.

To achieve an efficient usage of computer memory, a columnar packed matrix format stores only the nonzero stiffness matrix entries. An index matrix holds the references to the column

index in the index matrix. An entry will be found with a binary search of the column index in the index matrix. Additionally, because of the symmetry of the equation system, only one half of the matrix has to be stored.

A new implementation of a conjugate gradient solver, which uses this compressed matrix format, reduces the amount of computational time and memory consumption. The disadvantage of column searching is prevented by an intelligent algorithm design for matrix accesses in the solver and preconditioner. This method is now also used in the assembling module of the program. By redesigning the program we achieved a factor five or more in execution speedup for calculated problems such as crossing wire structures.

For the visualization of the potential distribution, a post-processing tool was developed. As a special feature, to obtain the same visualized potential distribution as described by the quadratic element shape functions, a surface subdivision algorithm was implemented to visualize the isofaces.

Robert Bauer was born in Vienna, Austria, in 1963. From 1983 to 1984 he was working on the support of medical analysis devices. In the course of his studies he has held various summer positions in the medical branch. He received the degree of 'Diplomingenieur' from the Technical University of Vienna in electrical engineering in 1990. After seven months of industrial development of Brain Mapping Systems – a medical brain diagnostic device, in the spring of 1991 he joined the 'Institut für Mikroelektronik', where he is currently working towards his doctoral degree in the field of three-dimensional interconnect simulation of multilevel wired VLSI circuits. In the spring 1993 he held a visiting research position at SONY, Atsugi, Japan.

VLSI Interconnect Simulation

and

Technology CAD Environments

Franz Fasching

The "Very Large Scale Integration Capacitance" (VLSICAP) simulator is used to extract capacitances of two-dimensional geometries by solving the Laplace or Poisson equation for the linear and nonlinear case, respectively, on multiple regions. The data level integration of this simulator into the "Viennese Integrated System for Technology Computer Aided Design Applications" (VISTA) has been extended considerably through the development and implementation of two important framework components: The "Unstructured Grid Support" (UGS) and a generic interpolation module.

With the help of the UGS module, VLSICAP is now able to write its result potentials not only on a tensor product grid, but also on unstructured grids with three- or six-node triangular elements. The UGS functions are part of the VISTA application libraries and available for C and FORTRAN applications. Through a flexible configuration, support for new grid element types can be added easily just by providing a decomposition function and an interpolation function for the new element which is then available for all applications of the framework. Data encapsulation techniques make unstructured grids appear as opaque objects to the application, and an orthogonal set of UGS interface functions allows clearly structured grid processing algorithms.

The generic interpolation works on distributed quantities (attributes) defined on grids and extends the idea of data and function hiding to attributes and attribute-grid objects, on which the interpolation functions work. Besides the above-mentioned unstructured grids, the generic interpolation is also able to deal with tensor product grids. Since these are also encapsulated into the attribute-grid object, the user knows nothing about the actual grid an attribute is defined on; it is sufficient to specify the desired attribute for initialization and then call the generic interpolation function for each new point the attribute is to be interpolated on.

This generic interpolation module will soon be used by the VISTA framework interpolation services, allowing the user to interpolate virtually from any grid to any other by just specifying the attribute and the target grid object.

VLSICAP uses the FORTRAN bindings of the generic interpolation, and thus is able to use doping profiles originating from PROMIS, the SUPREM wrapper or any other tool embedded in the VISTA, significantly enhancing its interoperability in the framework.

Franz Fasching was born in Steyr, Austria, in 1965. He received the degree of 'Diplomingenieur' from the Technical University of Vienna in electrical engineering in 1989. In February 1990 he joined the 'Institut für Mikroelektronik', where he is currently working towards his doctoral degree. In the winter of 1992, he held a visiting research position at SONY, Atsugi, Japan. His work is focused on the VISTA Technology CAD environment and improvement and extension of the capacitance simulator VLSICAP.

Simulation of Semiconductor Heterostructures

Claus Fischer

The simulation of heterostructure semiconductor devices presents a new challenge to the device simulation society. This is partly a matter of new physical phenomena and their appropriate modeling in device simulation and partly a purely technical matter concerning the organization and structure of a device simulation tool.

Simulation tools for heterostructure devices require more transparency in the description of the band models. These band models are necessary to describe the interaction of the two types of carriers in the various layers of a state-of-the-art heterojunction device.

Spatial variations not only of the basic variables, such as the potential and the electron and hole concentrations but also of many physical parameters like band edge offset energy, density of states and permittivity must be intrinsic features of a device simulation tool which would be capable of handling these quantities properly.

The hetero-interface itself requires special treatment. Thermionic emission, inversion at the interface and many other physical effects can only be modeled correctly if they are based on a distinct treatment of the physically different layers in the device. Special models are then used to describe the coupling of these layers, thereby connecting the equation systems which are formed in the single layers.

In each layer, a complete subsystem of the Poisson equation and the carrier continuity equations is discretized and assembled. The subsystems are connected at the interface points (where the equations are subject to certain rearrangement and merge processes) before the total system of equations is obtained. This total system can then be solved by a linear solver to perform an iteration of the nonlinear system. Due to the necessity of double valued interface points a general matrix format has to be used for the process of solving (many of the physical quantities, like band edge energies and carrier concentrations may assume different values on both sides of the interface – only the potential is unique).

Assembling and coupling the equations, setting the boundary values and other related tasks have to be performed automatically to preserve the generality of the input structures. No restrictive assumptions as to the number, topological location, the dimensions, or the environment of the different layers are allowed. Finally, the input and output data of the simulation tool are stored in PIF format, which ensures compatibility to the institute's TCAD framework.

Claus Fischer was born in Vienna, Austria, in 1967. He received the degree of 'Diplomingenieur' in electrical engineering from the Technical University of Vienna in 1989. In January of the following year, he joined the 'Institut für Mikroelektronik'. In the spring of 1992, he held a visiting research position at Motorola, Austin, Texas, USA. His work concerns device simulation in VISTA and the simulation of new structures within this TCAD framework, as well as numerical aspects of the coupling of simulation tools and the support required on integration of these tools. At present, he is working towards his doctoral degree.

Physics and Modeling of Hot-Carrier Degradation in MOSFETs

Predrag Habaš

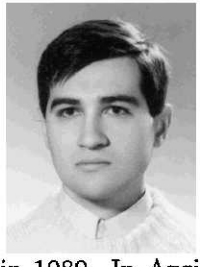
The transient numerical model of the charge-pumping effect implemented in MINIMOS has been extensively applied to study the changes in the charge-pumping characteristics after electrical stress. The cases of interface-state creation, hole trapping in the oxide, electron capturing on the trapped holes and neutral traps and the combinations of these effects are discussed by means of model-experiment. The ability of the charge-pumping to detect properly a localized fixed charge of both signs is investigated for the simultaneous presence of the localized interface traps. Charge-pumping characteristics of the virgin LDD device is studied in more detail. An analytical model of the gate-corner/LDD-region electrical field fringing effect is developed and applied to study the charge-pumping in the deep-tail region. The charge-pumping characteristics of stressed n-channel LDD devices is investigated to extract the spatial trap distribution in these device after the stress. The calculated trap distributions are used to calculate the evolution of the drain-current changes in time. The extraction of the spatial distribution and the amount of the fixed-oxide charge due to charge trapped in the oxide by the charge-pumping technique is analyzed.

The potential perturbation induced by the localized interface charge is studied by analytical and numerical means. A shortcomings of the formula Q_{ox}/C_{ox} for the gate-bias shift induced by the interface charge Q_{ox} are investigated, where C_{ox} is the

oxide capacitance. It has been shown that the width of the depletion region in the bulk, the width of the charged region, the condition at the interface around the localized charge (depletion, inversion or accumulation) and the oxide thickness influence the local potential perturbation and the gate-bias shift in a complicated, but well explained manner.

A hot-carrier injection model has been developed and implemented in MINIMOS. The gate current due to both, hot-electron and hot-hole injection and tunneling into the oxide are calculated. The complete bulk is considered in two-dimensions, regarding to injection path, injection angle and barrier in the oxide. The model represents a basis for modeling the carrier trapping in the oxide and finally, for the self-consistent calculation of the evolution of the device degradation, which is subject of the current activities.

In addition for the interface traps, the time-dependent basic semiconductor equation have been self-consistently coupled with the trap dynamics equations also for the bulk traps. The transient calculations including bulk traps are particularly interesting in studying SOI devices and GaAs MESFETs.



Predrag Habaš was born in Vrbas, Yugoslavia in 1962. He received the degree of 'Diplomingenieur' from the Faculty of Technical Sciences Novi Sad in electrical engineering in 1985 and the Mr degree from the Faculty of Electrical Engineering Belgrade in physical electronics in 1989. From 1985 he worked at the Institute for Power and Electronics University of Novi Sad as Research Assistant and Instructor, where he became a full Assistant in 1989. In April 1989 he joined the 'Institut für Mikroelektronik', where he is recently finishing his doctoral thesis. He held a visiting research position at Digital Equipment Corporation, Hudson, Massachusetts, USA in 1990. His research area includes physical electronics in general, and physics and modeling of MOSFETs in particular.

Electronic Properties of Silicon Dioxide

Michael Hackel

Silicon dioxide is of vital interest for "metal oxide semiconductor" (MOS) technology because of its importance as an insulator for gate electrodes. For "Ultra Large Scale Integrated" (ULSI) circuits the thickness of the insulating film is only comprised of a few nanometers, which results (for typical bias voltages) in a normal field approximately of 1 – 10 megavolts per centimeter (MV/cm). Experimental and theoretical studies give evidence that material breakdown will not occur under the influence of applied field-strengths as high as 20 MV/cm. Under these enormous fields, the electronic distribution becomes unstable if the energy being gained from the field can no longer be given to the lattice.

In low electron energy levels, polar longitudinal optical phonons are the dominant scattering process in silicon dioxide. The electrons lose a large amount of energy to the lattice due to a strong interaction of the polar phonon modes via the polarization field of the ions, but at high and intermediate fields they cannot prevent "velocity runaway" or even material destruction. Nonpolar acoustic phonons force electrons to scatter and stabilize the electronic distribution. As electrons reach the threshold for the emission of nonpolar acoustic phonons, the probability of having Bragg reflections (Umklapp-processes) increases keeping electronic carriers from gaining more energy from the field.

Recently, a realistic electronic band-structure has been implemented in our Monte Carlo transport model in order to get

reliable information about high energetic electrons. Carriers are accelerated by the applied electric field till they suffer a collision. One scattering mechanism is chosen accordingly to its statistical probability. The new state of the scattered electron is calculated and another free flight is performed until the maximum number of scattering events is reached.

In MOS structures, high-energy electrons in the semiconductor are responsible for trapping/detrapping effects in the oxide, degradation of the device, leakage effects on drain currents due to crystal defects, tunneling, impact ionization, interface charge formation and others. These effects can lead to dramatic failure or even damage of electronic devices, especially if future devices become ultracompact. Thus, new theoretical concepts have to be developed if we intend to design nanostructure devices. Injection of electrons from silicon into silicon dioxide and the possibility of inducing impact ionization, the emission of surface plasmons (which are responsible for the production of electron-hole pairs and, thus, for the creation of a positive interface charge) as well as the inclusion of collision-broadening in the scattering rates are considered and critically reviewed.

Michael Hackel was born in Vienna, Austria, in 1965. He studied technical physics at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1991. During his studies he worked on projects in solid state physics and quantum field theory. He joined the 'Institut für Mikroelektronik' in January 1992. He is currently working towards his doctoral degree. His scientific interests include solid state device technology, device modeling and physical aspects of semiconductors in general.

Software Aspects of the VISTA Technology CAD System

Stefan Halama

In the past two years, the VISTA project has grown to a size where it deserves major attention and effort. During the last year, besides continuous extensions and improvements of various parts of the VISTA framework, the major emphasis has been on the introduction of methods for achieving, maintaining, and verifying software quality.

A global error system has been implemented which replaces local error systems and provides a unified, flexible, and expandable method for signaling and handling errors between applications and framework modules. The error system features backtracing, error level filters, and a user interface. Specific error handlers can be added, removed, and configured at run-time.

The user interface segment of VISTA has undergone a major redesign, motivated by the need for platform independence and comprehensibility. A wrapper layer of functions has been put on top of the Athena widgets which will facilitate potential migrations. A widget for comfortable operating-system independent selection of files (including logical PIF files) has been developed and many LISP-based segments of the user interface has been re-implemented in C as a library so that they are now available in both C and LISP. This provides a unified appearance of LISP and C-based VISTA applications and a clearly structured and homogeneous programming interface.

With the development of the "VISTA MAKE" (VMAKE) utility, an already existing "Tool Abstaction Concept" (TAC) has been consistently integrated into the build process. It uses a formal definition of modules, functions, and constants, from which interface code is generated automatically, e.g., to link C-coded modules with the XLISP interpreter (the VISTA task level shell).

A general-purpose triangular grid generation module is currently being integrated into VISTA, which will work on PIF grid and attribute data without requiring any simulator-specific information. The synergetic effect together with the new unstructured grid support library can be expected to solve many open problems related to grid generation, arising in simulator coupling, preprocessing, and postprocessing.

Stefan Halama was born in Vienna, Austria, in 1964. He studied electrical engineering at the Technical University of Vienna where he received the degree of 'Diplomingenieur' in 1989. During his studies he collaborated with several Austrian companies, where he worked on software development projects in the CAD/CAE field. In September 1989 he joined the 'Institut für Mikroelektronik'. He is currently working towards his doctoral degree. In winter 1991 he held a visiting research position at Digital Equipment Corporation, Hudson, Massachusetts, USA. His research interests include process simulation, tool integration, TCAD frameworks, and software engineering.

Monte Carlo Device Modeling

Hans Kosina

Effort has been made to redesign the Monte Carlo facility of MINIMOS. It automatically generates a default setup, so that no further user interaction is required after invocation. All physical parameters as well as simulator specific configuration data can be supplied in the MINIMOS input-deck syntax in a very user-friendly manner.

The Monte Carlo device simulation program exploits several new algorithms in order to make it more efficient. First, by means of a free-flight time calculation method using a new self-scattering algorithm the amount of wasteful self-scattering events can be reduced dramatically. Second, a unique Monte Carlo-Poisson coupling scheme is used which converges faster than all presently known schemes. It is based on the so-called Monte Carlo–Drift Diffusion coupling technique. This technique also allows application of the Monte Carlo and drift-diffusion models simultaneously in different device regions. With this hybrid approach drift zones and other low field regions eventually present in a device are treated by the cheaper drift-diffusion method.

Recently, for polar semiconductors a bulk Monte Carlo model has been implemented. It has been evaluated for gallium arsenide, indium arsenide and indium phosphide. The model comprises a three-valley (Γ, L, X) band structure, the corresponding equivalent and non-equivalent intervalley scattering mechanisms, acoustic and optic deformation potential interaction, and polar-optic and Coulomb scattering. It is now ready

for implementation in a space-dependent fashion, so that the MESFET simulation capability existing in MINIMOS will be enhanced.

MINIMOS 6, the next version to be released, will include the Monte Carlo facility as one new feature. Among the others will be a transient simulation mode, that treats volume and interface trap rate equations self-consistently.

Further projects planned in the field of Monte Carlo device modeling focus on size quantization effects as they occur in surface inversion layers, and on the inclusion of the bipolar feature. The latter project aims at the simulation of novel bipolar devices, in which due to ultra-thin base layers non-local transport effects such as quasi ballistic transport become important.

Hans Kosina was born in Haidershofen, Austria, in 1961. He received the degree of 'Diplomingenieur' and the doctoral degree from the Technical University of Vienna in 1987 and 1992, respectively. He spent one year with the 'Institut für flexible Automation and joined then in 1988 the 'Institut für Mikroelektronik'. Currently he is being employed as an assistant professor heading the device modeling group. His current interests include physics and technology of solid state devices and integrated circuits.

Simulation of Micro-Structures

Erasmus Langer

Micro-structures are playing the dominant role in the broad field of microelectronic devices, therefore, their simulation and analysis has become eminently important. Doubtless, the most widespread representatives are "Ultra Large Scaled Integrated" (ULSI) semiconductor devices, but there exist also various other kinds of devices which are based on micro-structures, for instance the "Surface Acoustic Wave" (SAW) devices. Whereas the simulation of the latter can be restricted more or less to the device level, the analysis of ULSI semiconductor structures implies the necessity of the simulation of the technological fabrication processes, too.

The mathematical model for the simulation of micro-structures is represented by a "Partial Differential Equation" (PDE) set with adequate boundary conditions. Nevertheless the types of involved partial differential equations strongly depend on the given kind of micro-structure and their derivation is not at all a straight forward process: As an example, submicron MOS transistors can be simulated successfully by solving the well known fundamental semiconductor equations (although with sophisticated models for the physical parameters only) which consist in the time dependent case of the elliptic Poisson equation and the parabolic continuity equations. With decreasing feature sizes numerous second order effects must be taken into account, thus, the starting point of the derivation of the mathematical model for current flow is the Boltzmann equation in the phase space. On the other hand the problem of genera-

tion and excitation of electro-acoustic waves requires a simultaneous solution of the Poisson equation and the equations of motion which belong to the hyperbolic PDE type.

For the simulation of micro-structures not only their different types but also several substrate materials have to be distinguished. Although a different material enters the mathematical formulation through the models for the physical parameters only and does not affect the PDE structure it may be necessary to redesign the algorithm for the numerical solution. As an example the implementation of the physical parameters of silicon is not directly suitable for gallium arsenide.

A very interesting problem represents a micro-structure which combines semiconductor devices and SAW devices on one chip. Such a chip consists for instance of a SAW filter and the surrounding electronic circuit. In this case the parasitic effects, such as carrier flow in the filter domain and wave propagation in the area of semiconductor devices, have to be investigated rigorously since the substrate material is a piezoelectric semiconductor. The underlying mathematical model – a PDE set of elliptic-parabolic-hyperbolic type – is rather complex.

Erasmus Langer was born in Vienna, Austria in 1951. After having received the degree of 'Diplomingenieur' from the Technical University of Vienna in 1980 he was employed at the 'Institut für Allgemeine Elektrotechnik und Elektronik' first as a research assistant and then as assistant professor. His research field was first the numerical simulation of semiconductor devices and later the generation and excitation of electro-acoustic waves in anisotropic piezoelectric materials where he received his doctoral degree in 1986. Currently he works mainly in the field of simulation and analysis of microstructures with the strong point on ultra large scaled integrated semiconductor devices and acoustic wave devices.

Two Dimensional Simulation of Diffusion in Nonplanar Structures

Ernst Leitner

During the integration of the process simulator PROMIS into the VISTA framework the simulator has been divided into separate modules for the different process steps.

The diffusion module reads the geometric structure, the doping profiles and additional computational and control parameters from the PIF database. This PIF input file can either be generated interactively using the "VISTA User Interface" (VUI) or, for given process sequences, by the "Simulation Flow Control" (SFC) module.

Based on the polygonal boundaries of the geometry a grid with systematic "tensor product" connectivity between the grid points is generated automatically. This initial grid is modified by user-selectable methods in order to improve the grid quality criteria, like orthogonality inside of the domain and at the boundaries, grid line smoothness, and the area distortion of the grid cells. These criteria assure well conditioned equations for fast numerical solution.

This grid is refined adaptively by inserting and deleting grid lines in order to resolve the initial doping profiles sufficiently.

The resulting grid represents a curvilinear coordinate system. In the curvilinear coordinates the domain appears as a rectangle. The governing physical equations do not contain cross derivatives. The transformation of the model equations to the

curvilinear coordinates introduces cross derivatives in the differential equations depending on the deviation from the orthogonality of the grid. Instead of the five point discretization a nine point discretization is necessary to take into consideration the additional dependencies caused by the cross derivatives.

However, the cross derivatives tend to induce numerical instabilities and require additional criteria for grid adaptation in order to prevent generating ill conditioned geometric elements which, in turn, deteriorate the condition of the nonlinear system of equations. Therefore, in addition to the Deuflhard-damping in the Newton algorithm the damping strategy proposed by Bank and Rose has been implemented. This scheme, widely used in device simulators, proved to be the most satisfactory for our process simulation applications.

Future work will be focused on the design and implementation of a three dimensional diffusion module. This module is intended to allow for rather general geometric structures consisting of multiple domains. A high flexibility of the model equations, like in the existing two-dimensional module, should be maintained.

Ernst Leitner was born in Gmunden, Austria, in 1968. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1992. He joined the 'Institut für Mikroelektronik' in January 1993. He is currently working towards his doctoral degree. His research interests include process simulation including numerical grid generation in two and soon also in three dimensions.

Process Flow Representation and Design Automation

Christoph Pichler

Modern semiconductor device technology calls for several hundred fabrication process steps. At the design stage of a new product, the variation of certain critical device performance parameters is analyzed as a function of the pattern transfer mask geometries and the production process settings. Simulators exist for virtually all of these process steps as well as for the electrical behavior of the device itself, although they usually are rather particular about the representation of wafer data and control arguments. Therefore, the simulation of an entire process sequence cannot be done satisfactorily, comfortably and fast. Although a syntactically standardized interface for the exchange of data between simulators exists, semantic liberties cause ambiguities in the data written by the tools; there is no agreement regarding how to pass control parameters to a simulator or how to represent a process sequence independently from any specific simulation tool command language.

This work focuses on automation in semiconductor device design, putting special emphasis on a consistent wafer state representation, on the integration of a large number of simulations tools from a data interchange as well as from a tool control point of view, and on the comfortable definition end execution of multi-step process sequences. When first implemented it resulted in the "Simulation Flow Control" module of the VISTA framework. It allows for the definition of simulation tasks by

means of symbolic names for tools to be invoked and includes a macro mechanism which enables the user to build up large sequences from smaller, predefined modules, and for the simultaneous execution of multiple tasks. The current state of the simulated wafer is derived from the input and output data of the tool being called. The calculation results of each single simulation step remain available for later analysis and can be used to recompute a task from an intermediate step from the point at which a parameter of a process step is changed.

In order to further help the device designer with finding the optimal geometrical, topological, and process parameters, the future work will concentrate on the attempt to replace a conventional run traveller with its machine-readable equivalent, which can be directly used for controlling the simulation of the fabrication process. Furthermore, an interface with a knowledge-based system will be established, which will check for the violation of design rules and minimize computational efforts by checking for the possibility of reusing previous results.

Christoph Pichler was born in Vienna, Austria, in 1966. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1991. During of his studies he held several summer trainee positions at electrical engineering companies in Austria and Switzerland. In November 1991, he joined the Engineering Design Research Center at Carnegie Mellon University in Pittsburgh, Pennsylvania, where he worked on rapid prototyping and automation in manufacturing. He joined the 'Institut für Mikroelektronik' in November 1992 and is currently working towards his doctoral degree. His scientific interests include engineering design, semiconductor technology, and system integration

Technology CAD Applied for Multi-Mega-Bit Memory Development

Hubert Pimingstorfer

Our "Technology Computer Aided Design" (TCAD) environment VISTA has been successfully applied in the development of state-of-the-art "Dynamic Random Access Memory" (DRAM) chips. During the design of the MOS devices, process and device simulation, process parameter optimization, process sensitivity studies and input generation for MOS model parameter extraction were contributed.

The sequence of the CMOS fabrication steps were simulated using the two-dimensional process simulator PROMIS. The diffusion models were selected after comparison of measured and simulated one-dimensional profiles of a similar technology.

Automatic iterations over coupled process and device simulation were conducted to compute the threshold adjust implant dose to result in the intended threshold voltage for the NMOS transistor. Implanting into the channel region of the PMOS transistor also (therefore counterdoping it) and compensating this by a slightly higher well implant dose normally saves one mask. Simulation verified the feasibility of the simplification for this very process and calculated the correct well implant dose with respect to the intended threshold voltage for the PMOS transistor.

Process sensitivity studies included variation of oxide thickness, spacer width, channel length and channel implant dose. The device parameters observed were threshold voltage, cur-

rent drive capability, transconductance, and substrate current. For memory cells as well as access circuitry transistors worst case conditions were identified. For each of a total number of twelve devices the drain current versus gate and drain voltage characteristics were simulated in more than 200 bias points by the device simulator MINIMOS. Formatted properly, the results served as input for the extraction of MOS model parameters, which are the primary link between device and circuit design.

The specific contribution of the framework aspect of VISTA (besides its simulation tools) was the ease and automation of input deck generation, simulator sequencing, coarse-grained parallelization of simulation tasks onto a workstation cluster, output data collection, and postprocessing.

The benefit of the utilization of technology CAD for the described DRAM development, besides the additional insight into process and device physics generally gained from simulation, was that accurate circuit simulation could start several weeks before first silicon was ready.

Hubert Pimingstorfer was born in Linz, Austria, in 1964. He received the degree of 'Diplomingenieur' from the Technical University of Vienna in 1989 in electrical engineering. In November 1989 he joined the 'Institut für Mikroelektronik', where he is currently finalizing his work towards the doctoral degree in the field of integrating and applying simulators for the improvement and miniaturization of MOS devices. In 1992 he held a visiting research position at the Hitachi Device Development Center at Tokyo, Japan.

Process Simulation in Polycrystalline Silicon

Helmut Puchner

Heavily doped polycrystalline silicon (polysilicon) plays a crucial role in advanced integrated circuit technology. It is used as a gate material on most metal-oxide semiconductor (MOS) devices or as interconnect material. In bipolar technology it is being used as an active emitter material. In each application, understanding the way in which dopant diffuses during a thermal treatment in the polycrystalline material is essential to the processing of good devices.

A thin polysilicon layer, deposited by pyrolizing silane (SiH_4) between 600^oC and 650^oC in a low pressure-reactor, can be doped by diffusion, implantation or the addition of dopant gases (phosphine, arsine or diborane) during deposition (in-situ doping). After the doping process a thermal treatment process (diffusion, oxidation,..) can be started. In all these processes the structure of polysilicon is strongly influenced by dopants or impurities, temperature and process time. Polysilicon has a columnar grain-orientated structure and during a thermal treatment grain growth and crystallization occurs.

For the simulation of polysilicon diffusion processes a new model was incorporated in PROMIS. The basic idea to simulate the diffusion in polysilicon is to split the doped concentration C_{dop} into a grain inside concentration C_{gi} and a grain boundary concentration C_{gb} in a certain manner. After this split the diffusion equations can be solved for both concentration. Our model includes dynamic grain growth, grain bound-

ary motion, grain inside clustering and grain boundary clustering and dynamic dopant segregation between grain inside and grain boundary. The grain growth rate depends on the grain boundary energy, a geometric shape factor of the grains, the diffusivity across the grain boundary, the grain boundary thickness and the process temperature. It is to be assumed that during the grain boundary motion the moving grain boundary collects the dopants in which the grain grows.

Within the scope of the VISTA framework a high integration level of PROMIS into VISTA has been reached. PROMIS for VISTA provides an etching and deposition module, an analytical and a Monte Carlo ion implantation module and a nonplanar diffusion module based on geometry transformation method to handle nonplanar structures. The different modules of PROMIS communicate with each other via the PIF data base. The control of the modules can be done by the VISTA framework via user interface panels or by a "Simulator Flow Controller" (SFC). Also the simulators documentation can automatically be generated by VISTA's documentation system.

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The Profile Interchange Format Editor, a Comfortable Simulation Data Front End

Gerhard Rieger

The "Viennese Integrated System for Technology Computer Aided Design Applications" (VISTA) project of the Institute for Microelectronics provides a general data exchange format for simulation tools - the profile interchange format (PIF). It represents a consistent and stable basis for tools and their integration as well as for other high level segments of VISTA.

The profile interchange format editor (PED) is a powerful tool for creating and modifying device geometries and specifying their physical properties. It uses PIF for reading and writing data from and to files, but internally makes use of a more flexible list oriented data representation with explicit references and backreferences, called "C-List-Support" (CLS).

The PIF editor offers the user a set of menus and a drawing area. The former holds a spectrum of items to control PED and its display, while the latter allows the user to view, input, modify or delete geometric and physical data in a pure graphical manner.

While working with the PIF editor the user is supported by a number of features like background-grid, a display of the actual cursor coordinates, a field showing the current mode, and labels indicating the actual configuration of the mouse buttons. A text command line allows the user to enter commands via keyboard instead of menus or mouse.

To avoid multiple implementations of one and the same feature within PED, an internal command language has been designed, whose interpreter gathers commands from menus, the command line, and the mouse buttons.

To prevent conflicts inside the PIF editor due to unrelated command sequences, a stack automaton filters the user input, and controls and switches the modes. The mouse button configuration and the mode display are tightly coupled with the states of the automaton.

In addition to the two-dimensional capabilities of PED, a one-dimensional mode exists that allows full editing of one-dimensional geometries and devices. As a basis for a projected three-dimensional mode a primitive method for entering and viewing three-dimensional devices has been introduced.

To provide a user interface that is more flexible and easy to configure, and to increase the accessibility of external modules (for example grid generators and volume modelers) to interactive control, a LISP-interpreter-binding, similar to that of the VISTA system, is projected.

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Investigation of BiCMOS Devices with BAMBI

Gerhard Schrom

Modern integrated circuits often require performance features that can only be provided by combining bipolar and CMOS devices on one chip (BiCMOS technology). The implementation of a BiCMOS manufacturing process depends to the requirements to be met ranging from the development of a high-performance BiCMOS process down to the enhancement of a CMOS process with one or two types of bipolar devices with only a few or even no additional process steps.

In cooperation with the Austrian semiconductor manufacturer AMS, a CMOS-compatible vertical npn bipolar transistor (BJT) has been designed and developed. The BJT requires no additional process steps and offers acceptable bipolar performance at no additional cost. The device is especially suitable for high-voltage applications in electrically hostile environments such as automotive circuits. Its applications include overvoltage protection circuits, series and shunt regulators, buffers, solenoid drivers, and stepper motor drivers.

For the numerical simulation of mixed bipolar and MOS devices the general-purpose two-dimensional device simulator BAMBI is used. The current version of BAMBI is a traditional independent tool which has its own input-deck format, its own file format, and virtually no support in terms of user interface. Furthermore, the investigation of BiCMOS devices also involves the simulation of the manufacturing process and

the extraction of device parameters. Thus, if one goes beyond the investigation of just one device or the development of just one simulator it is certainly necessary to integrate the simulation tools into a TCAD framework such as VISTA. This will be done with BAMBI in order to achieve the flexibility needed for rapid device and process design.

As a part of VISTA, a material database system, a so-called VISTA material server has been designed and implemented. It consists of one or more material databases and a set of functions for accessing and maintaining the data. The intention of the VISTA material server is to provide a semantic buffer layer between the different tools which must deal with materials on different levels of abstraction and to free the tool programmers from the tedious task of case-checking and exception-handling. For example, a process simulator can write specific material names such as "BPSG" or "Si3N4" onto its output-file and a device simulator can then use the VISTA material server to recognize the material as an insulator and inquire its permittivity.

Gerhard Schrom was born in Mödling, Austria, in 1963. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in March 1992. During his studies he was working on software development projects in the CAD field. He joined the 'Institut für Mikroelektronik' in April 1992, where he is currently working towards his doctoral degree. His research interests include device and circuit simulation, circuit design and synthesis, signal and image processing, and TCAD framework aspects.

Simulation of Heterojunction Semiconductor Devices

Thomas Simlinger

Semiconductor transistors which rely on the use of heterojunctions for their operations are the most mature of a new generation of semiconductor devices. The heterojunctions in these devices are formed between layers of semiconductors of different compositions and bandgaps, like GaAs/AlGaAs as well as Si_xGe_{1-x}. Devices consisting of several layers, such as GaAs "High Electron Mobility Transistors" (HEMTs) and SiGe "Modulation Doped Field Effect Transistors" (MODFETs), alleviate the problems of surface scattering and impurity scattering at low temperatures. High electron mobility transistors rank among the fastest solid state devices ever constructed. These devices are therefore undergoing experimental and theoretical investigations which should be supported by powerful simulation tools. Significant changes and extensions of the institute's device simulator MINIMOS are made in order to be able to deal with these novel semiconductor devices.

Device geometries consisting of several layers can be seen as a step towards arbitrary device geometries. At present new capabilities are added to handle complex device geometries, such as layered structures, and hence the different materials and semiconductor compositions. This implies that the band description as well as many other parameters, like permittivity and low field mobility, must be definable at every point in the grid. To take into account abrupt heterojunctions, multiple values per grid point must be considered on interface.

Moreover, simulating the effects across the interfaces, such as thermionic-field emission boundary condition, requires a careful implementation of the coupling of adjacent layers. The complex device geometries and the great number of different materials and physical parameters make the integration in the VISTA environment desirable, as it supports a geometry editor as well as an extensive material database. Compatibility with the PIF application interface is also an issue, as it easily offers to import and export data, such as doping concentrations, device geometry and results for each simulation step.

Even though many of the problems simulating GaAs/AlGaAs and SiGe structures are similar for both types of devices, the significant mismatch of the lattice constants between SiGe layers leads to mechanical tensions which have an important influence on the electronic properties. Thus, when simulating SiGe devices it is required to take into account the splitting of the conduction band in two-fold and four-fold X-valleys, while the three-fold degeneration hole band is split into a light-hole, heavy-hole and spin-off band.

Thomas Simlinger was born in Mödling, Austria, in 1963. He studied communication engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1992. He joined the 'Institut für Mikroelektronik' in October 1992, where he is currently working towards his doctoral degree. His scientific interests include algorithms and data models, device modeling and physical aspects in general.

An Analytical AC Model for Vertical DMOS Transistors

Martin Stiftinger

The analytical subcircuit model for the vertical "Double diffused Metal Oxide Semiconductor" (DMOS) transistor was extended for the AC case. This model was developed on the basis of extensive device simulations and consists of an extended MOS transistor model which describes the channel of the device, a modified JFET which approximates the drift region together with a voltage dependent resistor. A nonlinear capacitor accounts for the source-drain capacitance (the model also describes the Miller-effect properly). Two bipolar transistors and some additional resistors model the behavior under reverse bias conditions.

The first important task was to adjust the JFET to the special geometry of the DMOS cell. This model also includes drift velocity saturation which is very important for the characteristic quasi-saturation behavior of the device.

As the channel profile is defined by the different lateral subdiffusions of p-base and n^+-source it is nonconstant in the lateral direction. The doping decreases from the source to the drain end of the channel. This was constantly taken into account by extending the MOS model describing the channel region. This nonuniform channel doping leads to a higher drain current and a decrease in the threshold voltage in comparison to a non-decreasing channel doping. This can be explained by a smaller bulk depletion charge at the drain end of the channel.

Device simulations confirm that these results are physically sound. The approach for taking into account the nonuniform channel doping can also be used to extend charge based capacity models in a consistent way. AC device simulations have shown that there is a significant dependence of the capacitances on the steepness of the doping profile which can properly be described by this new AC model. As in the DC case the AC model gives the "classical" results for a constant channel doping.

Also very important for a good AC model is the description of the source-drain capacitance. The first approach with a very simple network approximating the behavior of this capacitance was inexact. The gate-drain capacitance is mainly determined by the surface potential of the drift region. This potential can be described by a simple, but implicit equation. Therefore an additional node at the surface of the drift region was introduced and the surface potential was also determined by the nonlinear solution algorithm of the network simulator. This increased the simulation time a bit, but on the other hand gave much better results than the first approach described above.

Martin Stiftinger was born in Linz, Austria, in 1964. He received the degree of 'Diplomingenieur' from the Technical University of Vienna in 1989 in electrical engineering. In February 1990 he joined the 'Institut für Mikroelektronik', where he was first concerned with the iterative solution of large, sparse, and nonsymmetric linear systems and vectorization of those algorithms. He is working towards the doctoral degree, now focusing his work on device and network simulation of DMOS and high voltage CMOS transistors. His research area includes also parameter extraction and fitting strategies. In the spring of 1993 he held a visiting research position at the Philips Research Laboratories in Eindhoven, the Netherlands.

Three-Dimensional Monte Carlo Simulation of Ion-Implantation

Hannes Stippel

The miniaturization of today's semiconductor devices suggests a change from the common two-dimensional layout to three-dimensional structures to increase the amount of devices on the same wafer area. Therefore modern process simulators must be capable of modeling arbitrarily complex three-dimensional structures.

To satisfy this need for a realistic three-dimensional simulation a general module, both for amorphous as well as for crystalline targets has been developed. It is not restricted to any specific structures at all. It can handle any structure which is bounded by planar polygones. The critical point in three-dimensional simulations is the CPU-time consumption. Therefore two main speed-up techniques have been included: The first one is the superposition method. It is used to allow for the simulation of a large number of ions in order to obtain good statistics in reasonable computation times. Additionally, special attention was payed to the representation of the geometry and to the optimization of the geometry checks because these checks are critical in terms of simulation time for three-dimensional structures.

For this general module an octree is used to discretize the three-dimensional structure. The octree represents the geometry by cubes. Every cube is recursively subdivided into eight subcubes until either the desired accuracy of the discretization (defined via the minimum sidelength of the cube)

is reached or no intersection of the actually checked cube with the polygones defining the geometry exists. To determine the location of an ion during the simulation of an ion trajectory only simple comparisons to the sidewalls of the cube can be used, because a cube is a convex geometrical object. By use of the octree the CPU time required for an ion taking into account the real three-dimensional structure could be reduced to the same time needed for two-dimensional computations. For reliability tests, a graphic tool has been developed for the visualization of the octree derived from a discretization of a given three-dimensional structure. This program helps also to decide, whether the desired accuracy is sufficient.

The advantage of the octree can also be seen in the case of a crystalline target. There the structure is scaled according to the grid spacing of the crystal. By using the octree, only the sidelength of the root-cube has to be scaled accordingly instead of every point of the geometry with respect to a reference point. Moreover, the chosen data representation allows for an easy coupling of this module with three-dimensional topography simulators which are based on a cellular method.

Hannes Stippel was born in Vienna, Austria, in 1966. During his study at the Technical University of Vienna he held various vacation jobs at local companies. He also worked as a teaching assistant at the 'Institut für Hochbau für Architekten'. He received the degree of 'Diplomingenieur' in electrical engineering from the Technical University of Vienna in 1990. In July 1990 he joined the 'Institut für Mikroelektronik'. In the summer of 1992 he held a visiting research position at National Semiconductor Corporation, Santa Clara, California, USA. Presently he is working towards his doctoral degree. His work is focused on the simulation of ion implantation in arbitrary three-dimensional structures by using the Monte Carlo method.

A New Method for Simulation of Etching and Deposition Processes

Ernst Strasser

Computer modeling of topography processes such as plasma assisted etching, ion milling, thin film evaporation, and sputtering becomes increasingly important for semiconductor technology development. Numerical algorithms for surface advancement play a key role in the development of new simulators and lead to major differences in accuracy, robustness, and efficiency of the simulation tools.

Cell removal methods allow the simulation of arbitrary geometries, but they suffer from inherent inaccuracy. Surface advancement methods like string and segment based algorithms offer highly accurate results, though with potential topological instabilities such as erroneous surface loops resulting from a growing or etching surface intersecting with itself.

We developed a new method for simulating etching and deposition processes which is based on a cellular material representation and on morphological filter operations for surface movement. The simulation geometry is basically considered as a black and white image (material or vacuum). Fundamental morphological operations derived from image processing provide a well defined methodology for altering the given image. We use an array of square or cubic cells for material representation, where each cell is characterized as etched or unetched. In addition a material identifier is defined for each cell, therefore material boundaries need not be explicitly represented.

To advance the etch front, adaptive spatial filter operations are performed along the surface boundary. During the etching process, all cells within a filter are etched away, while cells outside stay unchanged. Usually, filters for anisotropic simulation are ellipsoids, filters for isotropic movement of surface points are spheres, although there is no restriction on the filter shape. Thus, the simulation of etching with preferred etch directions as in crystalline etching is also possible. The spatial filter dimension is related to the simulation time step and to the local etch rates. The etch front at a given time step is obtained by the envelope of filtered cells. This method allows an accurate simulation of arbitrary three-dimensional structures.

Modeling of specific processes requires information about shadowing of surface points and local surface orientation. Additionally, some surface regions will have a restricted view of the 'sky' above the wafer which for instance determines the amount of incoming flux during a sputter deposition process. All this information is used to calculate the etch or growth rate distribution along the surface boundary starting from a primary given rate. The calculated etch or growth rate distribution and the angular flux distribution of incoming particles in turn influences the shape and direction of the applied filters and therewith the evolution of the wafer surface.

Ernst Strasser was born in Salzburg, Austria, in 1966. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1991. In January 1992 he joined the 'Institut für Mikroelektronik', where he is currently working towards his doctoral degree. His work is focused on process simulation, especially on algorithms and mathematical models for three-dimensional simulation of etching and deposition processes in integrated circuit fabrication.

The VISTA Make Utility

Walter Tuppa

In the last year the VISTA project reached a complexity which cannot be handled by standard MAKE utilities any longer. There are many cross dependencies throughout the directory tree of the project and the number of libraries have increased dramatically due to newly implemented features. Moreover the port to VMS made a system independent MAKE utility absolutely necessary.

Therefore it was decided to create our own CASE oriented MAKE utility. It is based on the XLISP interpreter which runs on many platforms and operating systems and is also used as extension language of the VISTA project. The utility was designed to allow easy compilation of object modules, creation of libraries and executables and even execution programs and selftests. All these dependencies are stored in a small description file in each directory which is read by VMAKE during the first run. From this information an internal database is built where all dependencies are stored so that the information is available for the next execution. Since all dependency information is stored in one location even cross dependencies over directories can be checked very easily. In addition to program generation it is also able to handle the documentation of the VISTA project due to special comments in source files, additional documentation directories and special rules in the description files of VMAKE.

Dependencies for include-files in sources are automatically handled by VMAKE. During evaluation of a goal, required actions

to update the goal are performed project wide or locally (like the UNIX make utility) on request.

For easy use there is a so-called interactive mode. This allows the user to change options on the fly and check different goals as many times as required without the overhead of starting the XLISP interpreter and loading the LISP files and database. All user actions are automatically logged to a file for later review.

As a CASE utility VMAKE has module support. Each declared module in a description file can be turned on or off for building and installing. Due to the fact that all dependencies are known VMAKE is able to build releases and generate patch information for minor releases. It allows the generation of a installed version after full compilation. It also has the capability of checking the source against a common source database (in this case CVS) for user changes and missing files which are needed for building all modules of the project.

Walter Tuppa was born in Vienna, Austria, in 1966. Having received the degree of 'Diplomingenieur' in computer science from the Technical University of Vienna in 1991 and in electrical engineering in 1992, he joined the 'Institut für Mikroelektronik' in July 1991. He works on the VISTA project. At present, he is working towards his doctoral degree in electrical engineering.

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