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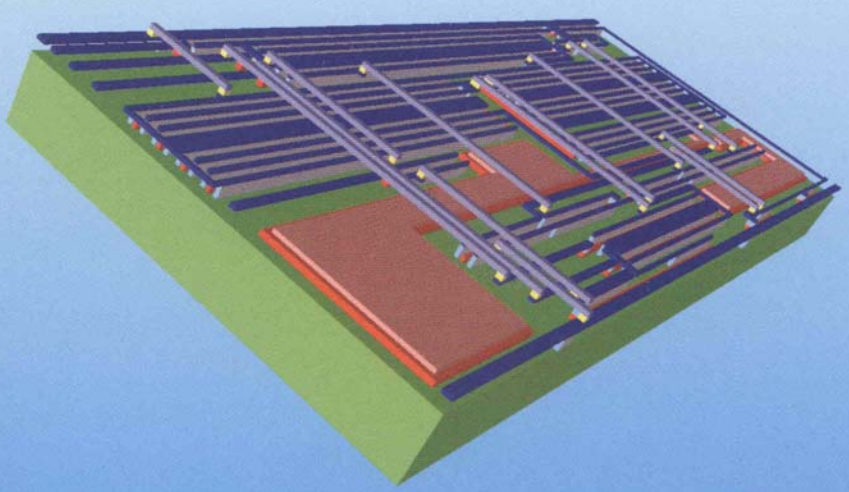

Annual Review
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Preface

Erasmus Langer and Siegfried Selberherr

This brochure is the eleventh annual research review of the Institute for Microelectronics. At the same time, it is the first review within the new organization of the 'Technische Universität Wien' according to the law 'UOG 1993'. In consequence of the election of Professor Selberherr as dean of the 'Fakultät für Elektrotechnik', the management of the institute has been extended. The staff financed by the Austrian Ministry of Science and Transportation consists of nine full-time employees: a full professor, two associate professors, three scientists, a secretary, and two technical assistants. Fifteen additional scientists are funded through scientific projects supported by our industrial partners, by the Austrian Science Fund (FWF), and by the EC Framework Programme.

We have been successful with projects focused on Technology Computer-Aided Design (TCAD) which is now the commonly established designation for our microelectonics modeling issues. The Special Research Program 'AURORA' whose title reads 'Advanced Models, Applications, and Software Systems for High Performance Computing' has recently passed its second year. Within this project funded by the FWF our main interests are focused on the efficient parallelization of our developed software tools by taking advantage of synergy effects with research groups in other fields.

Despite announcements of the ministry concerning a further reform of the universities we shall continue our way, and are entering the next year of our institute with high expectations.

Erasmus Langer was born in Vienna, Austria, in 1951. After having received the degree of 'Diplomingenieur' from the 'Technische Universität Wien' in 1980 he was employed at the 'Institut für Allgemeine Elektrotechnik und Elektronik'. In 1986 he received his doctoral degree and in 1988 he joined the 'Institut für Mikroelektronik'. In 1997 he received the 'venia docendi' on 'Microelectronics'. Since 1999 Dr. Langer is head of the 'Institut für Mikroelektronik'. His current research topic is the simulation of micro-structures using High Performance Computing paradigms.

Siegfried Selberherr was born in Klosterneuburg, Austria, in 1955. He received the degree of 'Diplomingenieur' in electrical engineering and the doctoral degree in technical sciences from the 'Technische Universität Wien' in 1978 and 1981, respectively. Dr. Selberherr has been holding the 'venia docendi' on 'Computer-Aided Design' since 1984. Since 1988 he has been the head of the 'Institut für Mikroelektronik' and since 1999 he is dean of the 'Fakultät für Elektrotechnik'. His current topics are modeling and simulation of problems for microelectronics engineering.

Renate Winkler was born in Vienna, Austria, in 1960. She joined the 'Institut für Mikroelektronik' in November 1993. Since that time she has been in charge of the organizational and administrative work of the institute.

Ewald Haslinger was born in Vienna, Austria, in 1959. He joined the 'Institut für Mikroelektronik' in December 1991. Since that time he has been in charge of organizational, administrative and technical work of the institute.

Manfred Katterbauer was born in Schwarzach St.Veit, Austria, in 1965. He joined the 'Institut für Mikroelektronik' in February 1995. Since that time he has been in charge of all technical hardware and software work of the institute.

Object-Oriented Wafer-State Management

Thomas Binder

Since the simulation of semiconductor fabrication process steps has gained importance over the last years a large number of simulators from various software vendors has become available. Each vendor thereby introduces a file format suitable to the very need of the simulator at hand. It is quite obvious that the coupling of such simulators nowadays becomes the limiting factor in the simulation of whole process flows. The developed *Wafer-State Server* addresses this kind of problems.

The *Wafer-State Server* is realized as a number of different modules each dedicated to a special task, such as file handling or meshing. It provides a set of (interface) classes to easily incorporate new implementations of such a module. This is achieved by a rigorous detachment of a module's interface from its actual implementation in a typical object-oriented manner.

To handle various different file formats an interface class (*reader*) has been defined. This class basically consists of a few function declarations which are coded for any supported file format. The *Wafer-State Server* internally only uses this interface functions and does not know about a certain implementation of a *reader*. Currently the *readers* for PIF and for the new ASCII file format WSS (**W**AFER **S**TATE **S**TRUCTURE) are available.

Another aspect of a *Wafer-State Server* are the supported gridding mechanisms. Some process steps, such as etching or deposition only modify the underlying geometry of a wafer

but leave its grids and thereon stored distributed quantities untouched. The problem arises that after such a step, the grid has to be adapted to reflect these changes. It is obvious that for a smooth interaction of several simulators this repair step has to take place in the *Wafer-State Server*, as opposed to using a stand-alone tool. As a direct consequence the *Wafer-State Server* needs the ability to invoke a gridding mechanism. To let the user choose what *gridder* implementation he would like to use, an interface class similar to the *reader* has been defined. All functions necessary for a *Wafer-State Server* internal gridding step are declared in this class. As with the *reader* class, the *Wafer-State Server* only uses functions from this class. Currently implementations for the *gridders* TRIANGLE (2D) and DELINK (3D) are available.

For the implementation of the *Wafer-State Server's* core classes the programming language C++ has been used. This, on the one hand, makes the utilization and combination of different modules (*reader*, *gridder*) at all possible and, on the other hand, allows for easy software management as well as future extensions.

Thomas Binder was born in Bad Ischl, Austria, in 1969. He studied electrical engineering and computer science at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in December 1996. During his studies he was working on several software projects mainly in the CAD, geodesy and security fields. In March 1997 he joined the 'Institut für Mikroelektronik', where he is currently working for his doctoral degree. In autumn 1998 he held a visiting research position at Sony, Atsugi, Japan. His scientific interests include data modeling, algorithms, software engineering, and semiconductor technology in general.

Simulation of Ferroelectric Materials

Klaus Dragosits

A promising approach to increase the capabilities of integrated-circuit nonvolatile memory is to take advantage of the hysteresis in the polarization of ferroelectric materials. For a rigorous analysis of these devices a suitable model for the simulation of two-dimensional hysteresis effects is necessary. This model has been developed and was implemented into the device simulator MINIMOS-NT.

The simulation of the two-dimensional hysteresis curve leads to the non-trivial problem of field rotation and requires the calculation of a set of parameters for the non-linear locus curve at each grid point. To allow the calculation of transfer characteristics, the algorithm has to be insensitive to the magnitude of the applied voltage steps. For a general approach to two-dimensional hysteretic effects an inhomogeneous field distribution must be assumed. This prevents the use of a simple one-dimensional hysteresis model using the same locus curve for the entire ferroelectric region. Two different locus curves have to be calculated for each grid point. Depending on the simulated ferroelectric material, different shape functions of the locus curve may be applied. These are $arctan$ functions for SBT ($SrBi_2Ta_2O_9$) and $tanh$ functions for PZT ($Pb(Zr,Ti)O_3$). The $tanh$ function allows an analytic calculation of the parameter set of the locus curves, the parameters of the $arctan$ function are determined numerically by the Newton method.

Similarly to magnetic properties the rotation of a constant magnetic field causes a lag angle χ of the induction. For a

rigorous two-dimensional analysis, the simple approach to decrease the electric field first to zero, then to increase it to the value of the next operating point and to add the two polarization components derived cannot be applied, as it is inconsistent with the one-dimensional hysteretic properties. Additionally, the results strongly depend on the distance between the calculated operating points. According to this we assume a straight trajectory between the vectors of the old and the newly applied electric fields. This also secures a proper numerical behavior if the applied voltage steps are increased. The basic principle of the applied algorithm is to split polarization and electric field of the previous operating point into components parallel and orthogonal to the next electric field. These curves yield the polarization in the direction of the electric field and the remanent polarization in the orthogonal direction, thus forming a primary guess for the next polarization. The scalar values of the two components are added and compared to the maximum polarization at the given magnitude of the electric field, forming an upper limit for the available number of switching electric dipoles. Due to the vanishing electric field in the normal direction, making it easier to switch the dipoles in this direction than the dipoles held by the electric field, the orthogonal component is reduced in respect to this limit.

Klaus Dragosits was born in Bruck an der Mur, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1996. He joined the 'Institut für Mikroelektronik' in September 1997, where he is currently working for his doctoral degree. His scientific interests include device simulation with special emphasis on nonvolatile memory cells.

Mesh Generation for Topography Simulation

Peter Fleischmann

The three-dimensional Delaunay mesh generator DELINK has been further developed. The data interface to the institute's topography simulator has been improved. It has been possible to automate the link from the output of the topography simulator, which uses a surface description, to the mesher, a finite element solver, and back to the topography simulator which reads the new etching or deposition rates as input.

It has become feasible to efficiently simulate processes which require an iteration between the topography module and the finite element module. The key issue is the capability of the mesher to allow arbitrary structures and to have an independent set of control parameters. The minimal information, which is one list of surface polygons or triangles, must suffice as input to the mesher. No extra knowledge about the structure, like the division into sub-blocks or special geometrical characteristics or the location of triangles, can be assumed. No restrictions on the surface triangles, for example the direction of their normal vectors, can be permitted. With one set of control parameters for all iteration steps a control unit repeats the execution of the topography tool, the meshing tool, and the finite element tool without any interaction.

The finite element solver applied to diffusion problems leads to the important topic of mesh quality. Some key experiments have been conducted on very special mesh types. Three ex-

ample meshes have been constructed which are all based on the same set of mesh points. In fact, the first two examples possess an identical ortho-product point cloud. For the third example a specific point of each sub-block of 27 points, which form a set of four cubes, has been shifted. The mesh topology of the first two examples with the same point cloud has been set up quite differently. On the other hand the topology of the third example with the shifted points has been identical to the topology of the second example.

In such a way the dihedral angle of the mesh elements was controlled to guarantee non-obtuse angles, or to purposely introduce obtuse angles in some elements. The results have given a significant new understanding of the different mesh requirements for non-stationary finite element simulation with very high gradients, the finite volume discretization, and respectively conclusions in two and three dimensions.

Peter Fleischmann was born in Kabul, Afghanistan, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in December 1994. In December 1997 he was with NEC in Sagamihara, Japan. He is currently working for his doctoral degree. His research interests include mesh generation as well as algorithms and data structures in computational geometry.

Electro-Thermal Mixed-Mode Simulation

Tibor Grasser

In mixed-mode device simulation the solution of the basic transport equations for the semiconductor devices is directly embedded into the solution procedure for the circuit equations. Compact modeling is thus avoided and much higher accuracy is obtained. Due to the increasing package density electro-thermal effects become more and more pronounced. Therefore, MINIMOS-NT has been extended with electro-thermal circuit simulation capabilities.

The standard way of treating temperature effects in semiconductor devices and circuits is based on the assumption of a constant device temperature which can be obtained by *a priori* estimates on the dissipated power or by measurements. However, in general this *a priori* assumed dissipated power is not in accordance with the resulting dissipated power. Furthermore, devices may be thermally coupled resulting in completely different temperatures than would be expected from individual self-heating effects alone. This is of special importance as many circuit layouts rely on this effect, e.g. current mirrors and differential pairs. Therefore, the temperature must not be considered a constant parameter, but must be introduced as an additional solution variable.

Thermal coupling can be modeled by a thermal circuit. The topological equations describing a thermal circuit are similar in form to Kirchhoff's equations and the branch relations map to familiar electrical branch relations. The electrical compact models have been extended to provide the device temperature

as an external node. For distributed devices MINIMOS-NT solves the lattice heat flow equation to account for self-heating effects. This is of course far more accurate than assuming a spatially constant temperature in the device and estimating the dissipated power by Joule-heat terms alone as is done for the compact models. To provide a connection to an external thermal circuit arbitrary thermal contacts are defined.

Thermal effects are of fundamental importance to the chip design of integrated circuits. Typical operational amplifiers (OpAmps) can deliver powers of 50–100 mW to a load, and as the output stage internally dissipates similar power levels the temperature of the chip rises in proportion to the dissipated output power. As the transistors are very densely packed, self-heating of the output stage will affect all other transistors. This is especially true as silicon is a good thermal conductor, so the whole chip tends to rise to the same temperature as the output stage. However, small temperature gradients develop across the chip with the output stage being the heat source. These temperature gradients appear across the input components of the OpAmp and induce an additional input voltage difference which is proportional to the dissipated output power.

Tibor Grasser was born in Vienna, Austria, in 1970. He received the 'Diplomingenieur' degree in communications engineering and the Ph.D. degree from the 'Technische Universität Wien' in 1995 and 1999, respectively. He joined the 'Institut für Mikroelektronik' in April 1996. His current scientific interests include circuit and device simulation, device modeling, and physical aspects in general.

Non-Parabolic Energy-Transport Modeling

Markus Gritsch

The design and implementation of a suitable simulator for general semiconductor devices is a demanding task, and the derivation of suitable models of the physical behavior is very important. Monte Carlo simulators allow the inclusion of rigorous physical models, but they need a lot of computational resources. A way to get quicker results is to use partial differential equation systems. The starting point to do this often is the Boltzmann transport equation. During the derivation, some assumptions are made due to the complexity of the problem. For example in the drift-diffusion transport model the temperatures of the carriers are constant and equal to the lattice temperature of the semiconductor. The energy-transport model, which takes the carrier temperatures into account, is usually derived under the assumption of a single parabolic valley of the conduction band.

The density of integration increases from year to year. With this down-scaling of the device geometry into the deep submicron range, some of the assumptions made in the derivation of the physical models are no longer valid. Therefore it is necessary to implement an improved formulation of the energy-transport model which more accurately models transport under submicron device conditions by accounting for the non-parabolic nature of the energy band structure. Commonly, a parabolic band assumption is used in order to facilitate the derivation of the conservation relations which form the energy-

transport model. The conservation relations are, however, affected by non-parabolicity.

Formally, the derivation of the conservation equations is complicated substantially by including non-parabolicity. Higher order moments of the distribution function, which are difficult to approximate, appear in the momentum and energy conservation equations. The relationship between the carrier temperature (as defined by the variance of the velocity distribution) and the average energy also involves higher order terms which can only be estimated with limited accuracy. In contrast the parabolic band assumption yields a simple relationship between the average energy, carrier temperature and drift velocity. The carrier temperature is a useful concept with a parabolic band since it results in the heat flux as the only higher order unknown which must be approximated. For a non-parabolic band, the carrier temperature is effectively an unknown quantity independent of the average energy and drift velocity, and the advantage of defining a carrier temperature is largely lost. Non-parabolicity therefore mandates additional approximations in order to close the set of transport equations with a tractable number of unknowns.

Markus Gritsch was born in Zams, Austria, in 1974. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1999. He joined the 'Institut für Mikroelektronik' in May 1999, where he is currently working for his doctoral degree. His scientific interests include circuit and device simulation, device modeling, and physical aspects in general.

Inductance Calculation in Interconnects Using the Magnetic Vector Potential

Christian Harlander

For a long time the speed of integrated circuits was largely determined by the switching speed of the individual transistors. The characteristics of the signal transfer from one device to the next were negligible. As switching times were accelerated, interconnect characteristics became critical and required accurate chip layout and system design for reducing the transfer delay.

Interconnection- and packaging-related issues are the main factors determining the chip performance as well as the number of circuits that can be integrated into a single chip. Reflections, cross talk and simultaneous switching noise increase delays or may cause logical faults, and therefore should be minimized by careful design. Cross talk is a result of capacitive and inductive coupling between neighboring lines. It increases as the lines get closer and the distances they neighbor each other get longer.

The package SAP (Smart Analysis Programs) has been extended to perform the extraction of inductances. We obtain the inductances of complex structures in general by applying the vector potential and not the magnetic scalar potential. Our three-dimensional simulation tool uses the finite element method to solve the Laplace equation for domains of conducting materials. Using the derivative of the electrostatic potential the distribution of the electric current density is obtained

by applying Ohm's law. The current density is used for the computation of the magnetic vector potential. Thereby, tetrahedral grid elements with quadratic shape functions are used. Two preprocessors allow a layer-based input of the simulation geometry and the specification of the boundary conditions. They automatically perform the meshing of the structures. A global grid level refinement is also available as a possibility of refinement for an area of interest.

In contrast to other simulation tools our general approach does not assume a uniform current density in the conductive domains, provided the inductances can be related only to the geometry.

For our approach it makes a great difference whether the self-inductance or the mutual inductance is computed. Calculating the mutual inductance is done by rewriting the integrations as summations over each element of the conductors, which is possible due to the behavior of the integrand without any numerical difficulties. The calculation of the self-inductance demands special formulae with certain integration points caused by singularities of the integrand. This method achieves accurate results for complex structures with large penetration depth. Our procedure is carried out without dividing the conductors into filaments and without assuming a uniform current density in the conductors.

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Multi-Dimensional Ion Implantation Simulation

Andreas Hössinger

In modern semiconductor process technology, ion implantation is commonly used to introduce dopants into semiconductor materials. Ultra shallow junctions, very complex device structures with strongly non-planar surfaces, and the necessity to provide very accurate point defect distributions for the simulation of rapid thermal annealing processes require Monte Carlo methods for the simulation of ion implantation. To achieve this accuracy, complex damage generation methods have to be used which result in very long computation times, especially when they are applied to three-dimensional process simulation.

The Monte Carlo ion implantation simulator MCIMPL is a multi-dimensional simulator which can handle one-dimensional, two-dimensional and three-dimensional problems. The simulated device may be of arbitrary shape and may consist of various amorphous and crystalline materials. The implantation of a wide variety of single atomic and molecular ions, such as boron, nitrogen, fluorine, silicon, phosphorus, arsenic, indium, antimony, BF_2, and N_2 can be simulated.

To achieve a very precise calculation of the distribution of interstitials and vacancies we have implemented a follow-each-recoil method into MCIMPL. The calculated point defect distributions make it possible to describe transient enhanced diffusion effects that occur due to a local super saturation of vacancies or interstitials, which originates from a shift between inter-

stitials and vacancies. While the super saturation can only be described by the follow-each-recoil method, the major disadvantage is that the simulation time for three-dimensional problems can easily exceed one day, despite very sophisticated algorithms and methods to reduce the simulation time.

For process simulation analytical ion implantation simulators are preferred to Monte Carlo simulators because of their lower CPU time requirements. We have implemented a point response interface into MCIMPL to combine the high accuracy of the Monte Carlo simulation with the low CPU time requirements of an analytical simulator. When using this point response interface method MCIMPL only calculates point response functions for the doping and point defect distributions at a representative point of the simulation domain. This point response function is used by the analytical simulator IMP3D to calculate the final distributions for the complete simulation domain. The gain in simulation time is proportional to the size of the simulation domain, but it has to be mentioned that this method does not deliver very good results in case of strongly non-planar devices. For such applications a full Monte Carlo simulation is necessary.

Andreas Hössinger was born St. Pölten, Austria, in 1969. He studied technical physics at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in January 1996. He joined the 'Institut für Mikroelektronik' in June 1996. He is currently working for his doctoral degree. His research interests include process simulation with special emphasis on the simulation of ion implantation.

Low-Power Electronics

Robert Klima

The quickly growing market for portable electronics and the increasing demand for life time and reliability have initiated a rapid worldwide development of ultra-low-power technologies to drastically reduce the overall power consumption of electronic circuits and devices. As a result, special technologies have been introduced and internal supply voltages have been reduced. The integration of mixed analog-digital functions on the same chip decreases the production costs and enables a broad spectrum of applications, such as portable electronic devices for mobile communications, medical electronic devices (pacemakers), or chip cards.

For industrial use the development of a special mixed analog-digital ultra-low-power technology is necessary. In this case a high clock rate is of less interest than a low power consumption for a specific functionality. Moreover, a closer look on system integration must be taken with the goal to implement all subfunctions of a product into a single chip. A technology must be developed which fulfills these requirements relying on the underlying manufacturing processes.

Nowadays short channel lengths of 0.25 μm and reduced supply voltages are used. It has been shown that several goals for the electrical quantities like low leakage current, high drain current, or a low power-delay product cannot be obtained simultaneously. Thus optimizations performed on one of these quantities yield worse values for the others. Values obtained, for instance, for a 0.25 μm CMOS device with 1.0 V supply

voltage are drain currents of 225 μA/μm for NMOS and 75 μA/μm for PMOS with leakage currents below 0.1 μA/μm and a power-delay product below 100 μWps.

Our device optimizations of the drain current with respect to low leakage current and a low power-delay product using a maximum supply voltage of 1.5 V are performed by taking the channel doping profile as the main optimization parameter. To achieve this, the channel doping is discretized by several ten points near below the gate while the substrate doping outside of the channel region is taken as a constant. By varying the doping concentration at these points in several optimization steps the doping profile can be adjusted as well as possible. The doping concentration between these points is interpolated. After a sensitivity analysis the resulting doping profile is approximated with Gaussian profiles to get a feasible doping profile for industrial productions.

For this work the optimization framework SIESTA and the device simulator MINIMOS-NT have been used which were developed at our institute.

Robert Klima was born in Vienna, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1997. He joined the 'Institut für Mikroelektronik' in September 1997, where he is currently working for his doctoral degree. His scientific interests include device and circuit simulation, computer visualization, and software technology.

Photolithography Simulation

Robert Kosik

LISI, an overall three-dimensional photolithography simulator, which accounts for all three lithography subprocesses of mask imaging, resist exposure/bleaching and resist development, has been developed. The simulator so far consists of three modules, whereby each module is specialized for one subprocess. We complement the simulator by implementation of a fast Maxwell solver.

The by far most demanding physical phenomenon in photolithography simulation is the resist exposure bleaching. The resist is a thin layer of a photosensitive material on top of the wafer. It records the mask pattern by absorbing light energy according to the illumination of the mask. Thereby the resist bleaches and the mask pattern is transferred to a latent bulk image. When modeling the light propagation within the photosensitive layer we have to take into account electromagnetic scattering effects due to a non-planar topography. Since the geometrical dimensions are comparable with the used wavelength, a physically rigorous three-dimensional lithography simulator must solve the Maxwell equations in a non-linear medium.

For this purpose we implement a finite element solver based on edge elements. The boundary conditions in lithography make the situation especially difficult. The aerial image simulator computes the incident light on the wafer surface, so the incoming half of the radiation is known. This corresponds to non-local boundary conditions. We treat them by using a

version of Berenger's perfectly matched layers and by domain splitting. As we use edge elements we can avoid the problem of "spurious" solutions, which haunt the FDTD methods.

A major concern for every simulation in three dimensions is efficiency. Modeling the bleaching requires a repeated solution of the time-harmonic Maxwell equations. As the linear system which results from the discretization is indefinite, conventional iterative methods only give very poor convergence rates. This problem can be solved by using a multi grid scheme, which was recently introduced by R. Hiptmair.

If the system has to be solved for several right hand sides, direct sparse methods are competitive, as the most time-consuming task in a direct solution is the symbolic assembly of the elimination tree. This is also important in case the illumination changes, but the geometry stays the same. For this reason we shall also include a sparse direct solver, which has the additional advantage that there is no problem of convergence.

The use of a Maxwell solver for TCAD in microelectronics is of course not restricted to lithography. While lithography is of our primary concern, we try to keep the solver "general purpose". Adhering strictly to object-oriented design, it is possible to accommodate it to a great variety of applications.

Robert Kosik was born in Eisenstadt, Austria, in 1969. He studied technical mathematics at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1996. After his civil service he joined the 'Institut für Mikroelektronik' in October 1998, where he is currently working for his doctoral degree. His scientific interests include applied and numerical mathematics, especially computational electromagnetism.

Physical Models and Numerical Methods for Advanced Device Simulation

Hans Kosina

The transport models commonly employed in numerical device simulators form a hierarchy comprising the drift-diffusion, the energy-transport, and the Boltzmann transport equation. The latter is usually solved by the Monte Carlo method.

Consistency among the transport models has been investigated. In situations close to equilibrium, i.e. when the applied voltages are small, or for large devices, equal results are expected from each model. To achieve this goal mobility models and scattering models are checked for consistency. For example, the field-dependent and the carrier temperature-dependent mobility models have to satisfy at least the local energy balance equation, and can therefore not be chosen independently. Impurity and surface scattering models are calibrated to yield low field mobility data consistent with both the analytical mobility models and experimental data. The goal of this investigation is to identify non-local and non-equilibrium effects occurring in small devices, and to specify for various simulation targets which model of the hierarchy needs at least to be used to account for the relevant effects.

Another project aims at the development of new Monte Carlo algorithms for device simulation. The starting points of the formal investigation are the integral forms of the transient and the steady-state Boltzmann equation. Approaching the iteration terms of the Neumann series of the two integral equa-

tions by Monte Carlo integration yield the backward ensemble and the backward one-particle Monte Carlo algorithms, respectively. The forward algorithms, which are the well-known ensemble and the one-particle algorithms, are obtained in a formal way from the respective conjugate equations. One goal of the project is to apply the backward and the weighted Monte Carlo algorithm to the problem of rare events in device simulation.

A first implementation of the weighted one-particle algorithms has been tested. The distribution of the scattering angle is altered in such a way that the carriers are guided against a retarding field. It turned out that the weights over different trajectories evolved quite differently giving rise to additional variance. This indicates that means need to be introduced to control the evolution of the weights and to reduce variance.

Hans Kosina was born in Haidershofen, Austria, in 1961. He received the 'Diplomingenieur' degree in electrical engineering and the Ph.D. degree from the 'Technische Universität Wien' in 1987 and 1992, respectively. For one year he was with the 'Institut für flexible Automation', and in 1988 he joined the 'Institut für Mikroelektronik' at the 'Technische Universität Wien'. In summer 1993 he held a visiting research position at the Advanced Research and Development Laboratory at Motorola, Austin, USA. In March 1998 he received the 'venia docendi' on 'Microelectronics'. His current interests include modeling of carrier transport and quantum effects in semiconductor devices, new Monte Carlo algorithms, and computer aided engineering in VLSI technology.

Low-Voltage, Low-Power Operational Amplifiers

Rui Martins

Integrated Circuit CAD has been driven by CMOS digital designers. Although electronic applications become supposedly more and more digital, there are applications that will require some sort of analog processing. In particular, A/D and D/A converters will always be required at the interface between the Digital Signal Processor DSP core and the off-chip peripherals.

Nonetheless, digitally designed oriented CAD tools are becoming unusable for analog circuits that are forced to follow the power supply voltage reduction operated in the digital side. Indeed, the popular criterion for judging device models, such as the mean-square error for currents that are reasonable for digital modeling, fails the prediction of the analog behavior of circuits, as the very low supply voltages bring MOSFETs out of the traditional strong inversion regime.

Realizing that the conventional circuit design tools cannot be used much longer to accurately predict circuit behavior, we propose an integrated simulation environment where all efforts to achieve maximum accuracy are taken into account. It links together ECAD tools with the accurate simulators found in TCAD frameworks. Active devices are characterized with device simulators and a table-based circuit simulator is used to avoid errors introduced by the fitting parameters procedures in compact models. Three-dimensional capacitance and resis-

tance extractor simulators quantify the parasitic parameters in interconnection wires created by three-dimensional topography simulators. This way, it is possible to globally optimize circuit and technology parameters, and to obtain the best solution for a given application.

The operational amplifier (OpAmp) is the most important building block in analog circuits. A novel OpAmp was implemented in a low-voltage technology that has been optimized in the above-mentioned simulation environment. As at sub-volt voltages the dynamic range is at premium, both input and output stages are rail-to-rail compatible, allowing it to operate correctly at power supply voltages as low as 0.5 V. While consuming only 15 μW, it has a 64 dB low-frequency gain and a unit-gain band width exceeding 5 MHz, using a die area of less than 0.1 mm^2.

Rui Martins was born in Porto, Portugal, in 1968. He studied electronic and telecommunications engineering at the University of Aveiro - Portugal, where he received the degree of 'Licenciado' in 1991 and 'Mestre' in 1994. In 1993 he was with INESC (Engineering Institute for Systems and Computers), where he worked on biomedical instrumentation. He joined the 'Institut für Mikroelektronik' in October 1994 where he received the Ph.D. degree in 1999. His scientific interests include very low power analog and digital integrated circuit design, digital signal processing and TCAD framework aspects.

Object-Oriented Model Management in TCAD Applications

Robert Mlekus

The exponential growth of the density of devices packaged on wafers implies the necessity of continuous improvement of physical and chemical models describing their processing, thermal and electrical behavior. For TCAD simulations this calls for the continuous development of new simulators with enhanced modeling capabilities. The increasing complexity of such tools requires their development in teams of people specialized in different fields. Thus, tools and concepts supporting "Rapid Application Development" in the field of TCAD applications gain increasing importance.

The *Algorithm Library* is a new object-oriented approach which implements an integrated tool set for the development of programs in the field of TCAD applications. It combines a library of C++ classes offering "non-networking model and parameter server" functionality with a framework for the development of application-specific extensions of the Model Definition Language (MDL). MDL is an object-oriented interpreter and compiler language designed to optimally meet and utilize the demands and peculiarities of TCAD applications and to achieve the highest possible run time performance within the central simulation algorithms. Another advantage of the MDL interpreter language over other general-purpose interpreter languages in the field of TCAD applications is the built-in support of the model and parameter abstraction concept designed to ease the joint work of physicists and computer

scientists by hiding much of the complexity of the underlying C++ class system. The built-in support for "Just in Time Compilation" of MDL code qualifies the *Algorithm Library* as a valuable tool for the development and final implementation of new algorithms and models for TCAD simulators.

The *Algorithm Library* is used in various simulators and tools developed at the Institute for Microelectronics. Within the diffusion simulator PROMIS-NT the *Algorithm Library* provides the primary interface to control the simulation and specifies the coefficients of a general transport equation describing the impurity distributions. Furthermore, the process temperature function and criteria for adaptation of the simulation grid can be specified by MDL. The device simulator MINIMOS-NT utilizes the *Algorithm Library* for the management of physical models. New models can be developed by sub-classing a number of predefined models either in C++ or MDL and are automatically integrated seamlessly into the standard input deck of the simulator. The simulator AMIGOS (Analytical Model Interface & General Object-Oriented Solver) uses the *Algorithm Library* to manage precompiled models and to provide additional parameter and function definitions to be used in the input deck.

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Statistical Methods for Transient Transport Simulation

Mihail Nedjalkov

The advanced modeling of the transient device behavior relies on the Ensemble Monte Carlo (EMC) algorithm. The algorithm is commonly defined as a simulated experiment which solves the Boltzmann Equation (BE) by emulating the real transport process. The alternative formulation is based on the numerical Monte Carlo theory and the integral form of the transport equation. Two issues related to this approach have been addressed. First, the numerical properties of the EMC have been studied. Second, a physically transparent model of the impulse response of the carrier system has been obtained.

The EMC generally estimates the distribution function (DF) mean value in a given phase space subdomain, i.e. the particle number inside. The successful application of EMC codes to a large variety of transport phenomena serves as an experimental evidence for the convergence of the algorithm. By an analysis of the Neumann series the convergence has been proved theoretically for general physical conditions. Furthermore the EMC has been formulated as a numerical MC experiment by determining the density function and the random variable corresponding to the carrier evolution process. This supplies the EMC with precision estimates such as probable error and variance. The variance in a given subdomain has been expressed as a function of the DF mean inside and the number of carriers participating in the transport process. It is an estimate of the

fluctuations, important in small devices where the carrier number is significantly reduced.

The knowledge of the small signal response of a semiconductor is of significant importance to forecast device performance. The response to a small signal of a general time dependence imposed on a DC field can be evaluated from the knowledge of the impulse response. The latter is provided by a signal whose time dependence is a delta function and cannot be realized by a physical experiment. Accordingly, the EMC is able to simulate the response to a step-like switch of the signal and to obtain the impulse response by a time differentiation. The integral representation of the BE founds a model for the impulse response behavior, allowing a direct stochastic simulation. The impulse disturbs the DC steady state by instantaneously creating two carrier ensembles. Their time evolution is under the action of the DC field. The impulse characteristics at a given time are determined by the difference of the two ensembles distributions at this time. The model allows to generate a variety of Monte Carlo algorithms.

Mihail Nedjalkov was born in Sofia, Bulgaria in 1956. He received the 'Master' degree in semiconductor physics at the Sofia University 'St. K. Ohridski' and the Ph.D. degree at the Bulgarian Academy of Sciences (BAS) in 1981 and 1990, respectively. For twelve years he worked in the Departments of Physical Analysis and Theoretical Research at the 'Institute of Microelectronics', Sofia. Since 1993 he has been with the Center for Informatics and Computer Technology, BAS, currently in a procedure for Associate Professor. He was visiting researcher at the Universities of Bologna (1992), Modena (1994 and 1995), and Frankfurt (1997). He joined the 'Institut für Mikroelektronik' in 1998, where he is currently working as a visiting researcher. His research interests include numerical theory and application of the Monte Carlo method, physics and modeling of the Boltzmann and quantum transport in semiconductors and devices.

Simulation of Heterojunction Bipolar Transistors

Vassil Palankovski

Heterojunction Bipolar Transistors (HBTs) attract much industrial interest nowadays because of their capability to operate at high current densities. AlGaAs/GaAs- or InGaP/GaAs-based devices are used for power applications in modern mobile telecommunications systems. Accurate simulations save expensive technological efforts to obtain significant improvements of the device performance. The two-dimensional device simulator MINIMOS-NT has been extended to deal with different complex materials and structures, such as binary and ternary III-V alloys with arbitrary material composition profiles. Various important physical effects, such as band gap narrowing, surface recombination, and self heating, are taken into account.

Energy transport equations are necessary to account for nonlocal effects, such as velocity overshoot. In recent work a new model for the electron energy relaxation time has been presented. It is based on Monte Carlo simulation results and is applicable to all relevant diamond and zinc-blende structure semiconductors. The energy relaxation times are expressed as functions of the carrier and lattice temperatures and, in the case of semiconductor alloys, of the material composition.

In particular the electrical behavior of AlGaAs/GaAs and AlGaAs/InGaP/GaAs one-finger power HBTs with emitter areas of 90 μm^2 has been studied at several ambient tempera-

tures, ranging from 300 K up to 380 K. Considering the nature of the simulated devices (including graded and abrupt heterojunctions) and the high electron temperatures observed at maximum bias (above 5000 K) we have used sophisticated thermionic-field emission interface models in conjunction with the hydrodynamic transport model. To account for self-heating effects the lattice heat flow equation is solved self-consistently with the energy transport equations (system of six partial differential equations). The thermal conductivity and the specific heat are expressed as functions of the lattice temperature and, in the case of semiconductor alloys, of the material composition.

The simulated Gummel plots for AlGaAs/GaAs and AlGaAs/InGaP/GaAs HBTs at 300 K are in good agreement with experiments. In addition, the simulated Gummel plots at 380 K demonstrate our ability to correctly reproduce the thermal device behavior. The significant increase of collector and base currents with the ambient temperature at low biases has already been confirmed by experiments.

Vassil Palankovski was born in Sofia, Bulgaria, in 1969. He studied electrical engineering at the Technical University of Sofia, where he received the degree of 'Dipl. Engineer' in 1993. Afterwards he worked for Siemens JV in Bulgaria for three years. He joined the 'Institut für Mikroelektronik' at the 'Technische Universität Wien' in May 1997, where he is currently working for his doctoral degree. His scientific interests include device and circuit simulation, heterostructure device modeling, and physical aspects in general.

Inverse Modeling of Semiconductor Doping Profiles

Richard Plasun

In inverse modeling the actual doping profile is predicted by analyzing the measured characteristics of the device. This is an important task because for deep sub-micron devices the actual doping profile differs from the simulated data for various reasons. This can be caused, for example, by missing or uncalibrated models of physical effects in the process simulators. Also vertical SIMS measurements of the manufactured device do not have the necessary accuracy for performance analysis.

Electrical data measured from manufactured devices — in particular output and transfer current-voltage characteristics — are a very strong description of a transistor. This electrical behavior is caused by a specific doping profile which is modeled by a two-dimensional analytical function. For the purpose of inverse modeling, where the electric characteristics of a simulated device are compared to the measured data sets, this procedure is sufficient if the artificial device adequately represents the simulated device.

The inverse modeling task is divided into two subproblems. In the first step the analytical doping profiles are fitted to the simulated output of the process simulation. This profile is used as the initial guess for the second step in which the simulated results are fitted to the measured electrical parameters by fine-tuning the doping profile. These two tasks have been

performed using the optimization capabilities of the SIESTA simulation environment.

For the inverse modeling task the approach of using template based device generation steps for the definition of analytical doping profiles has constituted considerable progress. Thereby a number of very CPU time consuming process simulation steps are replaced by a single generation task. The analytical doping profile has to be consistent with the results of the process simulation, valid for several gate lengths, and match the electrical data measured from the test wafers.

The electrical characterization is done with the device simulator MINIMOS-NT. For the gradient evaluations an initialization file is specified to improve the convergence behavior. In this case the simulator needs only a few iterations to find the solution.

Based on these concepts, integrated into the optimization module, inverse modeling applications are solved efficiently within the SIESTA simulation environment.

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Across-Wafer Non-Uniformities in Etching and Deposition Simulation

Wolfgang Pyka

Decreasing feature size and reduction of time and memory consumption are important driving forces for new developments in semiconductor process simulation. For the etching and deposition simulator ETCH3D these issues have been covered in the last years by accurate modeling and algorithmic optimization. Recently uniformity aspects of integrated plug fill and metalization processes have taken over the role as decisive factor in the development of the simulator.

Several aspects had to be covered to be capable of modeling integrated deposition techniques in three dimensions, namely the possibility for simulations at arbitrary wafer positions to account for particle, temperature, and concentration fluctuations across the wafer, the integration of reactor and feature scale simulation, and the development of a three-dimensional continuum transport and reaction model to include high pressure CVD processes.

Concerning the integration of reactor and feature scale simulation, an interface to the commercially available Monte Carlo particle transport simulator SIMSPUD has been developed for ballistic transport-determined PVD processes. This reactor scale simulator calculates the angular distribution of particles impinging on the wafer from the erosion profile of the sputter target, from the process conditions such as pressure and temperature, and from the reactor geometry. The resulting

distributions are read into ETCH3D and used for the integrative calculation of local deposition rates.

Recently a model for the simulation of continuum transport and chemical reaction-determined high pressure CVD processes has been developed. The model consists of a combination of specialized tools which are invoked iteratively. After extracting the surface of the initial geometry, a three-dimensional mesh of the gas domain above the structure is generated with DELINK. The differential equations describing the mass transfer and the reaction kinetics are set up and evaluated with AMIGOS, a general object-oriented solver which operates on the previously generated unstructured mesh. The resulting deposition rates are transferred to ETCH3D which performs the surface propagation. The advanced surface is again put into the meshing tool and this procedure is repeated until the overall simulation time is completed. This model covers a wide range of deposition processes, such as CVD of W by reduction of WF_6, TiN deposition from TDEAT ($Ti[N(CH_2CH_3)_2]_4$), and SiO_2 deposition with TEOS processes, including homogeneous gas phase reactions of precursors.

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Simulation of Heterostructure Field Effect Transistors

Rüdiger Quay

Heterojunction Field Effect Transistors (HEMTs) based on GaAs or InP substrates cover the whole frequency range within reach at present. HEMTs are in strong competition with MESFETs and HBTs for the frequency range below 10 GHz and are going industrial for the frequency range above 20 GHz. Device simulations of pseudomorphic AlGaAs/InGaAs/GaAs field effect transistors with MINIMOS-NT are used for the optimization and simplification of devices and processes for the frequency range up to 120 GHz.

One focus of our work is the precise correlation of "workable" device characteristics such as geometry, doping and material composition with the RF performance. Physically-based S-parameters simulations have been demonstrated between 2-120 GHz based on the simulation of small signal equivalent circuits for HEMTs. Bias dependence of both small signal equivalent elements and S-parameters shows good agreement with results obtained from real devices. Similarly the RF characterization of HBT is a focus of work. The connection of physical modeling and precision of RF simulation is under investigation.

It has been demonstrated for several devices that DC as well as RF device simulation for different HEMT technologies reveal equally good performance independent of the technology used. This is based on the extended modeling features within

MINIMOS-NT that can be adjusted to the technology without further changes.

The development of heterojunction interface models, i.e. thermionic field emission models in combination with hydrodynamic mobility models is pushed with respect to two issues: First to make these features suitable for optimizing III-V devices using optimization tools in the VISTA TCAD environment. Second, for gate lengths of 100 nm and below, improved interface models are needed to predict the performance when further scaling the devices to account for short channel effects.

With respect to applications for power applications in the 40 GHz range, the description of breakdown and self heating effects in the device becomes crucial. The influence of the saturation velocity has been carefully investigated. For the range above 77 GHz, e.g. for automotive or radar applications, the stability of the device performance with respect to technology and bias variations over various wafers is investigated to develop devices suitable for mass production also in this frequency range.

Rüdiger Quay was born in Köln, Germany, in 1971. He studied physics at the University of Bonn and the RWTH Aachen, where he received his Diploma in Physics in 1997. In summer 1996 he held a visiting research position at Los Alamos National Laboratory, New Mexico, for his master's thesis. He joined the 'Institut für Mikroelektronik' in April 1998. He is currently working for his doctoral degree at Fraunhofer Institute for Applied Solid-State Physics in Freiburg, Germany. His scientific interests include device simulation, heterostructure device modeling, and physically-based RF-parameter extraction.

Optimization of the On-Resistance of a VDMOS

Martin Rottinger

The double-diffused MOS transistor (DMOS) is a special type of MOS transistor in which the channel region is formed by two impurity implants. The channel length is determined by the different lateral extent of the two impurity profiles. In a vertical DMOS (VDMOS) the drain contact is located at the bottom side of the substrate. This makes it possible to densely place several hundreds or even thousands of devices in an array structure and to switch them in parallel.

The on-resistance of a VDMOS is one of its most important parameters because it limits the current which can be conducted by the device before it is damaged by self-heating. Therefore the on-resistance should be as low as possible. Another important parameter is the maximum blocking voltage. This is the maximum voltage, applied between the source and drain contacts with zero gate-source voltage, which does not lead to breakdown.

The investigated device is part of a small-signal transistor for drain-source voltages of up to 100 V and continuous drain currents of up to 1 A. The packaged transistor consists of 1671 devices connected in parallel.

To achieve the desired maximum drain current of the packaged transistor the appropriate number of single devices are switched in parallel and packaged together. Another possibility to improve the maximum current of the packaged device

is to reduce the on-resistance of each single device. The on-resistance of a VDMOS is mainly made up by the resistance of the low-doped epitaxially grown layer (epi-layer). By introducing an additional doping in the epi-layer it is possible to reduce the on-resistance compared with the conventional design. The higher doping not only reduces the on-resistance, it also increases the maximum electric field. High electric fields cause impact ionization which leads to breakdown and thereby limits the source-drain voltage at which the device can be used.

The goal of the device optimization has been to considerably reduce the on-resistance without degrading other performance parameters, such as the maximum source-drain voltage. The design of the optimized device has been further restricted by the requirement that the optimized device can be produced at costs comparable to that of the original device. This considerably limits the degree of freedom for designing improved devices.

The position and doping concentration of the additional n- and p-doped regions have been determined during the optimization and limits for acceptable variations of these parameters have been investigated.

Martin Rottinger was born in Wels, Austria, in 1968. He received the 'Diplomingenieur' degree in communications engineering and the Ph.D. degree from the 'Technische Universität Wien' in 1994 and 1999, respectively. He joined the 'Institut für Mikroelektronik' in November 1994. His scientific interests include solid state device technology and device modeling. In autumn 1995 he held a visiting research position at Philips in Eindhoven, The Netherlands and in autumn 1997 at Digital Equipment Corporation, Hudson MA, USA.

CMOS Gate Delay Time Optimization

Michael Stockinger

The ever-increasing demand for speed enhancement and higher device densities on the chip imposes a big challenge for CMOS process and device designers. New device structures have to be found to overcome imminent problems, such as leakage currents, short-channel effects, punchthrough, and drain induced barrier lowering.

The switching speed of digital circuits is reflected by the average gate delay time of an inverter chain. Decreasing this delay time while keeping the static leakage current low means increasing the speed of the whole technology without changing the standby power. Usually, the device geometry and the supply voltage are fixed for a given technology, therefore the key challenge lies in an optimized doping profile.

With SIESTA we have a powerful tool for closed-loop optimization purposes. In order to set up a complete optimization task, a circuit model is introduced which emulates the behavior of an infinite inverter chain delivering the average gate delay time and leakage current. It consists of an NMOS and a PMOS transistor and a capacitive load. MINIMOS-NT is utilized to carry out transient mixed-mode simulations. In order to obtain consistent input/output characteristics during the optimization, the resulting output voltage curves of the inverter model are repeatedly used as input voltage curves for the following optimization steps. Additionally, the actual load capacitance is calculated from the input current curves of the preceding step.

Two different methods are used to obtain a set of optimization parameters which define the doping profiles in the active regions of the two transistors: A general two-dimensional approach using an optimization grid arranged within the shape of an inverted "T", and an approach with implantation models.

Gaussian implantation models allow for a considerable reduction of the number of doping parameters and, therefore, for a faster optimization procedure. Furthermore, the resulting doping profiles from the two-dimensional approach which look quite complex due to the numeric origin of the optimization procedure can be tailored to more realistic profiles.

With this optimization procedure, the gate delay time is drastically reduced compared with inverters built with conventional devices. The reason for that is the clearly asymmetric channel doping which increases the drive current capability of the transistors. Experimental MOS devices are in fabrication using FIB (Focused Ion Beam) techniques to confirm the theoretical results by measurements.

Michael Stockinger was born in Vienna, Austria, in 1970. He studied communications engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1996. After his studies he worked on an ASIC-design project at the 'Institut für Allgemeine Elektrotechnik und Elektronik' for six months. In February 1997 he joined the 'Institut für Mikroelektronik', where he is currently working for his doctoral degree. In summer 1998 he was with the Advanced Products Research and Development Laboratory at Motorola, Austin, USA. His scientific interests include device and circuit simulation and design, solid state device technology, and low-power technology.

Optimization and Inverse Modeling

Rudolf Strasser

The efficient practical application of TCAD simulation tools requires the services of a simulation environment which establishes their integration. The SIESTA (**Si**mulation **E**nvironment for **S**emiconductor **T**echnology **A**nalysis) TCAD environment is the next generation of simulation environments following VISTA/SFC.

SIESTA is an *open* environment which means that it can work with virtually arbitrary simulation tools. The interface which integrates these simulation tools has been designed very rigorously, and it takes care that SIESTA is able to control the simulation tools and manage their results. SIESTA's users are able to create abstract *models* based on that simulation tool interface. Moreover, networks of such models can be created in order to design a comprehensive model based on several simulation tools. This functionality allows for the formulation of complicated matters on an abstract simulator-independent level.

In practice networks of models can be used to describe problems which arise in the modeling of integrated circuits' fabrication technologies. It is possible to design models including several device categories of an integrated circuit (e.g. NMOS and PMOS devices which are implicitly coupled by their common fabrication process), and, therefore, include several aspects. As a consequence optimization can be performed based on a simulation model which includes multiple integrated devices instead of just a single one.

Based on these abstractions it is possible to carry out optimizations. These optimizations improve the simulation model in terms of a certain respect. On the other hand, a Levenberg-Marquardt optimizer can be utilized to calibrate model parameters, or to perform inverse modeling tasks (e.g. doping profile extractions). In order to cope with the considerable simulation effort which is required for that sort of task within minimal time, SIESTA offers features for distributed parallel computation. Thereby, the simulation work is distributed to computers on a local area network in such a way that the overall computation time becomes minimal.

Job farming features enable the utilization of computers available within a local area network. A mechanism for dynamic load balancing takes care of the optimal utilization of CPUs, taking their computing performance as well as their workload into account. Moreover, SIESTA manages tool licenses and, in particular, node locked licenses.

Rudolf Strasser was born in Ried im Innkreis, Austria, in 1970. He received the 'Diplomingenieur' degree in electrical engineering and the Ph.D. degree from the 'Technische Universität Wien' in 1995 and 1999, respectively. From spring 1992 to autumn 1993 he held a research position at the campus-based Engineering Center of Digital Equipment Corporation, Vienna, Austria. He joined the 'Institut für Mikroelektronik' in April 1995. In summer 1996 he was with the Advanced Products Research and Development Laboratory at Motorola, Austin, USA. His scientific interests include semiconductor technology, grid generation, and software engineering.

Modeling Carrier Transport in Quantized Systems

Christian Troger

As MOS device feature sizes are continuously scaled down in view of better performance, the device parameters are strongly influenced by quantization effects of the carrier motion in the inversion channel. It is therefore common practice to implement fast and reliable quantum corrections in usual device simulation tools. Considering the complex underlying physical theories, the demand for practical computation time limits the complexity of usable models in such device simulators. Thus it will be necessary to have special tools to validate these simpler models. In such a tool we can solve the conflict between accurate modeling and needed computation time by limiting the investigations to simpler geometric structures but using more accurate physical models.

The developed Schrödinger Poisson solver (SPIN) has been designed to consider the electron transport in quantized systems and to study the influence of non-parabolic energy dispersion relations. The simulator is based on the effective mass approximation and includes the non-parabolic correction by means of a modified kinetic energy operator that is solved in the Fourier domain. Some improvements have been added to our simulation tool SPIN: The simulated electron system is split into two parts. Above a certain energy limit the carriers are treated classically. This reduces the number of sub-bands to be considered without sacrifice on the accuracy of the result and helps to avoid numerical problems. Based on a flexible interpola-

tion class it is now possible to include doping effects in the simulation. A further gain in accuracy has resulted from the introduction of two different simulation grids for Schrödinger's and Poisson's equations. This allows to use a finer grid at the interface for the calculation of the charge density and is absolutely necessary to produce accurate C-V curves in a reasonably short time.

To obtain a flexible tool the code of the program has been revised in order to use the object-oriented concepts of C++. A simple parser together with some related classes for the decoding of options helps to handle the user input in the form of a script language. This concept allows to quickly add new commands, to provide a graphical user interface that can be completely separated from the simulation tool and to add new functionality in form of clients for the existing server application. A powerful unit and scaling class is used to manage the input parameters.

The method used to include non-parabolicity in Schrödinger's equation will be compared to the $k \cdot p$ theory for two-dimensional systems. This enables us to use a different set of physical parameters for the simulations and to consider hole and electron quantization.

Christian Troger was born in Vienna, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1995. He joined the 'Institut für Mikroelektronik' in September 1995, where he is currently working for his doctoral degree. His scientific interests include software engineering and the simulation of quantum mechanical devices.

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