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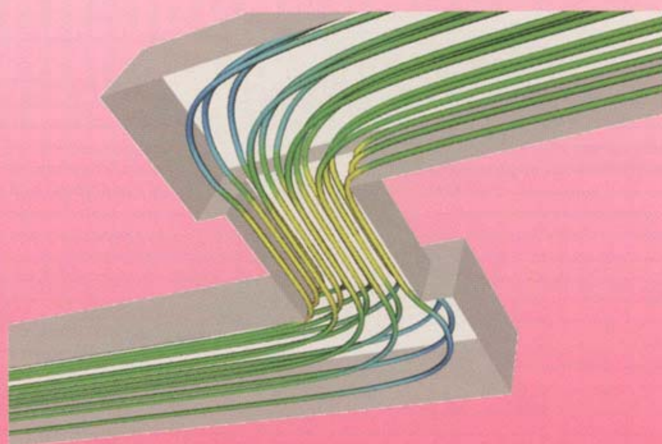

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Preface

Erasmus Langer and Siegfried Selberherr

This brochure is the thirteenth annual research review of the Institute for Microelectronics. The staff financed by the Austrian Federal Ministry of Education, Science, and Culture consists of ten full-time employees: the dean of the Faculty of Electrical Engineering and Information Technology, the head of the institute, one additional professor, four scientists, a secretary, and two technical assistants. Seventeen additional scientists are funded through scientific projects supported by our industrial partners, by the Austrian Science Fund (FWF), and by the EC Framework Programme.

While the two EC projects MAGIC-FEAT and NANOTCAD are continued, we proudly report that a third project within the "Information Society Technology Programme (IST)" is already granted but has not yet started officially. A further EC project is in the state of preparation. We are glad to be able to report that all our industrial partners have continued their cooperation. Furthermore, we have succeeded in starting new cooperative research with SAMSUNG, Seoul, Korea.

Despite the demotivating public discussions around the Austrian university education in general as well as the current legislation and far-reaching plans of the government regarding the future university scene, we are entering the next year of our institute with high expectations because of the trust of our cooperating partners in our scientific work.

Erasmus Langer was born in Vienna, Austria, in 1951. After having received the degree of 'Diplomingenieur' from the 'Technische Universität Wien' in 1980 he was employed at the 'Institut für Allgemeine Elektrotechnik und Elektronik'. In 1986 he received his doctoral degree and in 1988 he joined the 'Institut für Mikroelektronik'. In 1997 he received the 'venia docendi' on 'Microelectronics'. Since 1999 Dr. Langer has been head of the 'Institut für Mikroelektronik'. His current research topic is the simulation of microstructures using High Performance Computing paradigms.

Siegfried Selberherr was born in Klosterneuburg, Austria, in 1955. He received the degree of 'Diplomingenieur' in electrical engineering and the doctoral degree in technical sciences from the 'Technische Universität Wien' in 1978 and 1981, respectively. Dr. Selberherr has been holding the 'venia docendi' on 'Computer-Aided Design' since 1984. Since 1988 he has been the head of the 'Institut für Mikroelektronik' and since 1999 he has been dean of the 'Fakultät für Elektrotechnik'. His current topics are modeling and simulation of problems for microelectronics engineering.

Renate Winkler was born in Vienna, Austria, in 1960. She joined the 'Institut für Mikroelektronik' in November 1993. Since that time she has been in charge of the organizational and administrative work of the institute.

Ewald Haslinger was born in Vienna, Austria, in 1959. He joined the 'Institut für Mikroelektronik' in December 1991. Since that time he has been in charge of organizational, administrative and technical work of the institute.

Manfred Katterbauer was born in Schwarzach St.Veit, Austria, in 1965. He joined the 'Institut für Mikroelektronik' in February 1995. Since that time he has been in charge of all technical hardware and software work of the institute.

Modeling and Simulation of Non-Equilibrium Dopant Diffusion

Tesfaye Ayalew

Within the past decade process simulation has become an essential part of new technology development in the semiconductor industry. The use of TCAD (Technology CAD) tools has been driven by the enormous cost of purely experimental approaches to technology development. Yet the power of these tools and their predictive capability are limited by the models they use. One of the limitations requiring improved models is the redistribution of dopant atoms, which determine the electrical characteristics of the final device structure.

Diffusion is a key area of ULSI processing, since dopants are generally introduced into a wafer by ion implantation requiring a high temperature annealing step which leads to an unavoidable diffusion of the dopants. As devices continue to shrink, better models will certainly be required. The challenges of the future include more detailed information about collateral damage resulting from ion implantation, a better understanding of point defect properties such as equilibrium populations, diffusivities, and transient response to temperature changes, better models for point defect behavior at interfaces, and finally the development of accurate methods to actually measure two- and three-dimensional dopant profiles.

Since many profiles are box-shaped, dopant diffusion in silicon often requires a three-dimensional investigation of problems. One tool rendering model development substantially simpler

is the recently developed general purpose partial differential equation (PDE) solver AMIGOS (Analytical Model Interface and General Object Oriented Solver), which can implement models of diffusion in time and space, for two or three dimensions. It has been recognized a long time ago that such a simulator could be very useful for investigating the detailed physics of the reactions involved between dopants and defects.

A significant opportunity for the future is to greatly expand this simulator in order to integrate it with other process and device simulation tools to help in the development of modern semiconductor process technology. Much of the effort in modeling nonequilibrium dopant diffusion has focused on ion implantation and rapid thermal annealing (RTA) because of the great industrial importance of these processes. Efforts are being made to understand the evolution (form, grow and eventually dissolve) of {311} defects during the RTA process, and to the simulation of these extended defects to predict transient enhanced diffusion (TED) and to estimate model parameter values.

Tesfaye Ayalew was born in Addis Ababa, Ethiopia in 1966. He earned his BSc degree in Electrical Engineering from Addis Ababa University in 1989. Afterwards he served for five years at the Medical Equipment Engineering Service in Ethiopia. In 1995 he joined the Institute for Biomedical Engineering, University of Vienna, where he carried out a one year research work on functional electrostimulation. In the same year he was accepted by the 'Technische Universität Wien' where he studied Electrical Engineering and received the degree of 'Diplomingenieur' in March 2000. He joined the 'Institut für Mikroelektronik' in May 2000, where he is currently a doctoral fellow in the field of TCAD. His research interest is focused on multi-dimensional modeling and simulation of dopant diffusion.

Integration of Process Simulation Tools

Thomas Binder

In a state-of-the-art TCAD environment a large number of different semiconductor process simulation tools are available. Their capabilities range from computing single or abstract process steps like etching or diffusion up to simulating a whole process flow or even semiconductor fabrication equipment. Nevertheless, a combination of such tools allowing that the output of one simulator can be used as input for another one is still difficult. An early approach to this problem was to use a file format common to all tools involved in a simulation. However, it turned out, that supplying the necessary conversion tools to incorporate commercial tools is a tedious task. Furthermore, a common file format does not sufficiently address all the problems arising in the simulation of a process flow.

Our wafer-state data model has been designed to approach this kind of problem. The wafer-state server is realized as a C++ class library and presents the tool developer with a set of modules for I/O handling, gridding and core functionality like point location and interpolation. The modules are realized as interface classes; several implementations exist for each module. All interface classes are dimension-independent.

Our process simulators AMIGOS, MCIMPL and ETCH3D have been extended to work with the wafer-state server classes. The simulators are now capable of choosing the desired input and output file format as well as the gridder implementation to be used at runtime, as specified on the command line or in the

input deck. Furthermore, both read and write I/O support for the DFISE file format is being implemented. This will allow for a seamless integration of all ISE tools.

As native binary file format of the wafer-state server the HDF standard has been chosen. HDF is a very well standardized file format which offers features like parallel I/O to increase performance. Also, a large number of tools directly supporting HDF is available. For visualizing the data, the tool ROCKETEER which is based on VTK can be used. This tool is capable of directly reading HDF files that are generated by the wafer-state server.

Thomas Binder was born in Bad Ischl, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in December 1996. During his studies he was working on several software projects mainly in the CAD, geodesy and security fields. In March 1997 he joined the 'Institut für Mikroelektronik', where he is currently working on his doctoral degree. In autumn 1998 he held a visiting research position at Sony, Atsugi, Japan. His scientific interests include data modeling, algorithms, software engineering and semiconductor technology in general.

Electromigration Simulation

Hajdin Ceric

One of the most important issues in the reliability study of integrated circuits interconnect lines is electromigration. Defined as the mass transport resulting from the collision of conducting electrons and metal atoms of interconnect lines, this phenomenon results in the formation and growth of voids which in the extreme case may cross the inteconnect line and sever the connection.

In order to predict the lifetime and resistance change of the interconnect line, accurate models for the void dynamics are needed. Void dynamics includes nucleation, growth, migration and occasionally coalescence of voids. It is influenced by the physical characteristics of the metal line such as grain boundary structure, crystal dislocations, anisotropy of bulk and surface diffusivity.

To model the effect of time evolution of insulating voids on the interconnect lifetime and resistance change, it is essential to describe the development of the interface between void area and the metal. This interface takes different shapes during the void evolution, a phenomenon known as void facetting. Generally, characteristic void shapes enable a prediction of the future behaviour of the void: circular and elliptical voids tend to migrate through interconnect lines without further changes in shape, thus having only a minor influence on the resistance of the interconnect. On the other hand, wedge and slit-like voids may grow and develop into structures causing interconnect line

failure. A widely adopted approach assumes a sharp interface, which requires explicit finite element tracking of the void surface. Despite the considerable success of the method, simulating realistic void evolution phenomena involving complex topology changes is numerically challenging. Diffuse interface models are a possible alternative. This approach is based on a characterization of the interconnect line by an order parameter field. Changes in void shape are described by the evolution of this field, which has been shown to be governed by a modified form of the Cahn-Hilliard equation.

To simulate the behavior of voids at the critical locations in interconnect lines where a strong current density divergence develops, we have implemented an additional feature to the general PDE solver AMIGOS (Analytical Model Interface and General Object Oriented Solver) which enables a solution of the Cahn-Hilliard equation coupled with the equations of the electro-thermal problem. In related literature, a variety of numerical methods have been proposed for the solution of the Cahn-Hilliard equation. We have studied several algorithms with respect to convergence and stability properties to determine the most appropriate one for the problem of electromigration.

Hajdin Ceric was born in Sarajevo, Bosnia and Hercegovina, in 1970. He studied electrical engineering at the Electrotechnical Faculty of the University of Sarajevo and the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 2000. He joined the 'Institut für Mikroelektronik' in June 2000, where he is currently working on his doctoral degree. His scientific interests include interconnect and process simulation.

Three-Dimensional Mesh Generation for Electronic Device Simulation

Johann Cervenka

Coming along with the rapid development of electronic devices, the consideration of highly sophisticated physical effects is necessary. To achieve device simulation with highly accurate results, equivalent models have to be implemented. Unfortunately, many of these phenomena require a three-dimensional analysis, and the device simulators have to be extended to deal with three dimensions. For this purpose appropriate grids have to be generated. Because of the influence of the simulation grid on the quality of the simulation, grid generators must be especially adapted.

For device simulation, two conflicting effects must be considered. On the one hand, badly fitted grids have to be avoided to achieve accurate simulation results. Therefore, a refinement of the grids is necessary, which results in a boost of grid points and grid elements. On the other hand, particularly for three-dimensional simulations, the simulation results should be delivered within an acceptable execution time and memory consumption. Therefore, the amount of grid points should be minimized.

With ortho-product grids the density of grid points can be varied independently in the three spatial directions. However, with the complex and nonplanar device structures used nowadays, this method will produce a huge number of unnecessary grid points. Tetrahedral meshes can well resolve the geometry,

but the grid density cannot be varied in such a straight-forward way. A method has been developed which combines the benefits of these two methods. The simulation domain is treated as a resistor with a voltage applied at two electrodes on top and at the bottom of the domain. In this area the grid points are placed at the intersections of selected equipotential lines and vector lines. For the subsequent device simulation the set of grid points has to be tetrahedrized.

For the evaluation of the electric field inside the resistor, the discrete Laplace equation is solved on an initial grid, which is generated by the mesher deLink, also developed at the Institute. Because of the sparsity and the high rank of the matrices of the resulting equation system, a conjugate gradient solver is chosen. The cells surrounded by equipotential lines and field lines are approximately cuboidal in shape, the grid is conforming to the surfaces, and the spacings between the selected equipotential and field lines can be varied independently.

Special emphasis must be put on the method for choosing the spacings between the potential and vector lines. Therefore, a refining method – especially suited for semiconductor devices – depending on the doping concentrations is under development.

Johann Cervenka was born in Schwarzach, Austria, in 1968. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1999. He joined the 'Institut für Mikroelektronik' in November 1999, where he is currently working on his doctoral degree. His scientific interests include three-dimensional mesh generation as well as algorithms and data structures in computational geometry.

Analysis of Ultra Short Channel Devices with High-k Gate Dielectrics

Klaus Dragosits

According to the International Technology Roadmap for Semiconductors (ITRS), the gate dielectric becomes one of the critical issues for short channel devices. If SiO_2 is used the proposed oxide thicknesses are getting smaller than 1nm, thus leading to massive direct tunneling current. To reduce this parasitic effect, alternative materials with higher k values and consequently a higher layer thickness have to be investigated.

The first basic analyses of the effects related to the increased insulator thickness have been carried out in recent years by investigating the transfer characteristics of CMOS devices. Basically a degradation of the device performance due to an increase in the parasitic capacitances has been observed. The increase in parasitic capacities leads to a reduction of the channel control. Depending on the dielectric constant k of the dielectric layer two effects can be observed: A reduction of the slope of the transfer characteristics and a decrease in the threshold voltage.

An increase in the k-value increases the drain to channel capacitance, which adds an additional charge to the channel independently from the applied gate voltage. This additional charge causes a shift of the transfer characteristics to the left. This effect can be compensated by other measures such as workfunction engineering in the gate or a modification of the channel profile. Thus, materials with an 'only-shifting' k-value

can be considered as alternative gate dielectrics. The decrease in the slope can be interpreted as a general loss of channel control by the gate as the fringing fields and consequently the gate to drain/source capacitance increase. This effect can only be compensated by a variation of the stack geometry.

Another matter of interest is the significance of the static transfer characteristics for the transient device performance. This analysis is performed simulating a five-stage ring oscillator. Since the delay time is closely linked to the contact capacities of the device an influence of the geometry on the obtained result is expected. Comparison between a k=3.9 and a k=19.5 gate dielectric shows a significant impact on the delay time, which increases by about 30% for the mid-k device.

This result is remarkable as it cannot be expected from the static transfer characteristics, which were almost identical for the two devices. The increased delay time can be explained by an increase in the capacities between the gate contact and the drain/source doping due to the higher k-value of the gate oxide.

Klaus Dragosits was born in Bruck an der Mur, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the 'Diplomingenieur' and the Ph.D degrees in 1996 and 2001, respectively . He joined the 'Institut für Mikroelektronik' in September 1997. He held visiting research position at Philips Research, Eindhoven, in March 2000 and at the Samsung Advanced Institute of Technology, Seoul, in June 2000. His scientific interests include device simulation with special emphasis on nonvolatile memory cells and high-k dielectrics.

Mesh Generation for Thin Layers and the deLink Release

Peter Fleischmann

The three-dimensional mesh generator deLink has been released. deLink is a Conforming Delaunay Triangulation code. The input is a structure boundary description which must be closed under intersection: All intersections between input points, edges, and polygons must be contained in the input. For example, two polygons may not overlap and they may only touch each other along shared points and edges. The polygons can be non-convex. Edges which share more than two polygons, for example triple edges, are allowed.

Optionally, the input may contain a set of points which do not belong to the boundary description. These points can have any location, outside, inside, or on the surface of the structure. In automatic mode deLink generates points which cover the domain by itself. The output is a Delaunay mesh of the structure with additional points on the surface (conforming) and in the interior. The input and output data can be supplied via a file for the deLink standalone program, or via a functional interface (API) when deLink is used as a library.

A test suite has been created by collecting relevant benchmark structures and special-case geometries from various fields. These examples also include non-manifold boundary descriptions. Using scripts, these approximately 200 test examples have been successfully as well as automatically meshed on several platforms.

Furthermore, work has been concentrated on constructing reasonably sized meshes for structures with thin layers. Thin layers demand certain anisotropic mesh spacing capabilities. A purely isotropic mesh generator would create elements in the thin layer which possess a largest edge length of approximately the size of the thickness of the layer. Hence, the lateral mesh spacing is too small and the thin layer requires a too high number of isotropic mesh elements especially in three dimensions. By means of orthogonal projection, point snapping, and Steiner point refinement, a scheme has been implemented into deLink which yields satisfactory results in most cases. However, further development is required for more general types of thin layers, for example thin layers which consist of non-parallel surfaces.

Peter Fleischmann was born in Kabul, Afghanistan, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in December 1994. In December 1997 he was with NEC in Sagamihara, Japan. In February 2000 he finished his Ph.D. degree at the 'Institut für Mikroelektronik' where he is currently enrolled as a post-doctoral researcher. In fall 2000 he held a visiting research position at the University of California at Berkeley. His research interests include mesh generation, CAD, and computational geometry.

Modeling of Tunneling Currents in MINIMOS-NT

Andreas Gehring

Oxide tunneling currents play a major role in microelectronics. They are used in flash memory cells to transfer charge to an isolated floating gate by applying high voltages at a control gate. They cause an increased power consumption of deep-submicron MOS transistors due to parasitic currents through the ultra-thin gate oxide. Memory cells are facing reduced retention times due to a leakage through the memory node isolation. Resonant tunneling diodes use tunneling currents to achieve a negative differential resistance, resulting in extraordinarily high operating frequencies. Even gate stacks of alternative high-k gate dielectrics like Si_3N_4 or TiO_2, which are proposed to limit tunneling currents, introduce interface states which alleviate trap-assisted tunneling.

The quantum-mechanical phenomenon of oxide tunneling has been studied since the early days of Fowler and Nordheim in 1928, who reported electron emission through a dielectric layer under high electric fields. They presented a first empiric model of the tunneling current density, which was extended by Lenzlinger and Snow in 1969 to the commonly known Fowler-Nordheim formula. This simple model describes the tunneling current through triangular energy barriers. The tunneling current only depends on the electric field, the barrier height and the electron mass in the oxide. In 1992, Schuegraf et al. presented an extension of the Fowler-Nordheim model to include direct tunneling, which occurs for trapezoidal energy barriers.

However, the Fowler-Nordheim and Schuegraf models apply a number of assumptions which are not justified in real devices, like the replacement of the Fermi function with a step function. The Bardeen model represents a higher degree of accuracy. It originates in the independent-electron theory formulated by Bardeen, Harrison and Stratton in 1962. This model calculates the tunneling current by an integration over the product of an energy-dependent supply function and a quantum-mechanical transmission coefficient. It can be shown that the Fowler-Nordheim model as formulated by Lenzlinger and Snow and the Schuegraf model are special cases of the Bardeen model.

The Fowler-Nordheim, the Schuegraf and the Bardeen models are now implemented in MINIMOS-NT and can be chosen independently for each insulator segment. The barrier height and the oxide mass can also be specified for each segment. Further studies will be made into two directions. First, hydrodynamic simulations require a non-Maxwellian form of the electron energy distribution, where first approaches have been made by Fiegna in 1991. Second, the emerging field of single-electron discrete-charge tunneling cannot be covered by any of the presented models. The applicability of the Master Equation method will be studied for this purpose.

Andreas Gehring was born in Mistelbach, Austria, in 1975. He studied communications engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in March 2000. He joined the 'Institut für Mikroelektronik' in April 2000, where he is currently working on his doctoral degree. His scientific interests include device simulation, memory cell techniques and semiconductor physics in general.

Simulation of Semiconductor Devices Including Higher Order Moments

Tibor Grasser

For modern semiconductor devices, non-local effects gain more and more importance. In the traditional drift-diffusion model the average carrier energy is assumed to be in equilibrium with the electric field. This assumption has been shown to be invalid as the increase in average carrier energy lags behind the electric field increase. In order to obtain information about this non-local behavior of the carrier energy, various hydrodynamic and energy-transport models have been proposed. However, it has been found that the average carrier energy is not sufficient for an accurate modeling of physical parameters like mobility and impact ionization.

To overcome the limitations of the available energy-transport models we have developed a consistent transport model based on six moments of Boltzmann's equation. In addition to the concentration and the carrier temperature as provided by the energy-transport models, we have obtained the average of the square energy which we have mapped to a new solution variable, representing the kurtosis of the distribution function.

Within the new transport model we have developed an analytical description for the symmetric part of the distribution function which goes beyond the Maxwellian assumption. This extension is necessary because for a given average energy the distribution functions are completely different depending on whether they are taken from regions where the absolute value

of the electric field increases or decreases. In addition, the shape of the distribution function is only poorly approximated by the Maxwellian shape assumption.

With an analytical model for the distribution function together with a proper description of the density of states we can integrate microscopic scattering rates to yield models suitable for macroscopic device simulators like MINIMOS-NT. These models have proven to accurately reproduce impact ionization rates as predicted by Monte-Carlo simulations. In particular, these models are valid for bulk and deep submicron devices, a property which allows for bias and geometry-independent calibration.

As the six moments model is a consistent extension of standard energy-transport models it allows for a more detailed study of the characteristic properties. Especially spurious velocity overshoot has attracted a lot of attention. Our simulations show that these spurious peaks are largely caused by the truncation of the infinite moment hierarchy when defining a closure relation for the energy-transport models.

Tibor Grasser was born in Vienna, Austria, in 1970. He studied communications engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' and the doctoral degree in technical sciences in 1995 and 1999, respectively. He joined the 'Institut für Mikroelektronik' in April 1996. From October to December 1997 he was with Hitachi Ltd., Tokyo, Japan, as a visiting research engineer. In February 1998 he was appointed Assistant Professor at the 'Institut für Mikroelektronik'. His scientific interests include circuit and device simulation, device modeling, physical and software aspects in general.

Modified Hydrodynamic Transport Model for SOI-MOSFET Simulation

Markus Gritsch

By using the hydro-dynamic (HD) transport model for the simulation of the output characteristics of partially depleted SOI MOSFETs, an anomalous decrease in the drain current with increasing drain-source voltage has been observed. It is believed that this decrease is a spurious effect because to our knowledge it is neither present in experiments nor can it be observed when using the drift-diffusion (DD) transport model.

However, the applicability of the HD model is desirable. In contrast to the DD model it takes nonlocal effects into account, which gain importance in the regime of the ever decreasing minimum feature size of today's devices.

The main difference between the HD and the DD transport models is the presence of the additional energy balance equation. The benefit of the increased computational effort is that the carrier temperature can differ from the lattice temperature. Since the diffusion of the carriers is proportional to their temperature, the diffusion can be significantly higher when using HD transport.

When simulating SOI MOSFETs this increased diffusion has a strong impact on the body potential, because the hot electrons of the pinch-off region have enough energy to overcome the energy barrier towards the floating body region and thus enter into the sea of holes. Some of these electrons in the floating body are sucked off from the drain-body and source-body

junctions, but most of them recombine. The holes removed by recombination cause the body potential to drop. A steady state is obtained when the body potential reaches a value which biases the junctions enough in reverse direction so that thermal generation of holes in the junctions can compensate this recombination process. The decrease in the output characteristics is directly connected to the drop of the body potential via the body effect.

In Monte-Carlo (MC) simulations the spreading of hot carriers away from the interface is much less pronounced than in HD simulations. If we assume that the Boltzmann equation does not predict the hot carrier spreading, and if the HD equations derived from the Boltzmann equation do so, the problem must be introduced by the assumptions made in the derivation of the HD model. In this regard, the approximation of tensor quantities by scalars and the closure of the hierarchy of moment equations are relevant.

A modified HD transport model using different closure relations and an anisotropic carrier temperature are currently being worked on.

Markus Gritsch was born in Zams, Austria, in 1974. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1999. He joined the 'Institut für Mikroelektronik' in May 1999, where he is currently working on his doctoral degree. His scientific interests include circuit and device simulation, device modeling and physical aspects in general.

Inductance Calculation in Interconnects by Applying the Monte-Carlo Method

Christian Harlander

One of the consequences of technology scaling by shrinking feature sizes and increasing clock frequencies is that the design of interconnect lines becomes increasingly crucial. The performance of interconnects is limited by various parasitic effects, such as signal delay, capacitive and inductive crosstalk, and attenuation.

The utilization of new materials, such as copper and low-k dielectrics, reduces the RC time constant. Thereby decreased resistance and capacitance increase the influence of inductive effects, requiring consideration of the latter in circuit simulation. Thus, inductance extraction becomes necessary for critical nets.

Both inductance calculation methods implemented in the package SAP (Smart Analysis Programs) are based on a numerical solution of Neumann's formula for a precalculated stationary current density distribution.

The Monte-Carlo method is a well-known choice for the evaluation of multiple integrals. This method, where point coordinates are chosen randomly, requires a fairly high effort on CPU time, owing to the time-consuming search for the associated element of the random point coordinates.

To reduce the error, a high number of function evaluations have to be carried out, whereby for each evaluation the aligned el-

ement with the precalculated current density must be found. To improve the convergence during the Monte-Carlo sampling, several variance reduction schemes such as importance sampling or control variates can be applied.

A major advantage of our implementation is the bypassing of the high computational effort for the element location. We first determine the associated element and then locate the point inside the tetrahedron.

For this purpose we take two arrays for each conductive segment. The first one contains the volume of each element, whereby the sum of all entries is scaled to one. The second array contains the probability function already evaluated for each conductor element by adding up all entries from the beginning to the current index of the first array. Then the random generator chooses a number between zero and one. The associated element complying to the probability function is found by a binary search.

To ensure a uniform probability the local coordinates of the integration points are found by selecting a point in the unit cube. The first point inside the registered unit tetrahedron is taken. For the interpolation of the current density inside each element, quadratic shape functions are used.

Christian Harlander was born in Taxenbach, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1997. He joined the 'Institut für Mikroelektronik' in December 1997, where he is currently working on his doctoral degree in the field of three-dimensional interconnect simulation of multilevel wired VLSI circuits. In winter 2000 he held a visiting research position at Sony, Atsugi, Japan.

Faithful Approximations for Optimization, Inverse Modeling, and Design for Manufacturability

Clemens Heitzinger

The main problem in optimization for TCAD purposes still is the fact that the evaluation of the objective function is very computationally expensive. There are two main approaches: the first is to optimize the given objective function, and the second is to optimize an approximation of the objective function. Both approaches are implemented in the SIESTA (Simulation Environment for Semiconductor Technology Analysis) framework. The second approach relies on how well an approximation was chosen, and that it can be evaluated much faster than the original objective function so that conventional optimization algorithms requiring a substantially higher number of evaluations can be applied.

In the traditional RSM (response surface methodology) approach polynomials of degree two are used almost exclusively. However, this method suffers from the fact that such an approximation does not preserve the global properties of the given function: the set of all polynomials of degree two or less is not dense in $C(X)$, $X \subset \mathcal{R}^p$ compact. Moreover, evaluating the objective function at more and more points generally does not improve the RSM approximation, rendering these evaluations wasted.

To overcome the shortcomings of the RSM approach, we are using generalized Bernstein polynomials. The basic theorem

states that if $f : [0,1] \to \mathcal{R}$ is a continuous function, then the Bernstein polynomials $B_{f,n}(x) := \Sigma_{k=0}^{n} f(k/n)\binom{n}{k}x^k(1-x)^{n-k}$ converge uniformly to f for $n \to \infty$. Additionally to uniform convergence, also the derivatives of the approximation converge to those of the given function. In our applications we have used generalizations to the multi-dimensional case.

Also, good approximations resembling the global properties of the objective function can be used for solving design for manufacturability problems. This method of computing approximations gives rise to a recursive optimization algorithm. After a first approximation, either further approximations of interesting areas are computed, or – if needed – the first approximation is refined using additional points.

Furthermore, the SIESTA optimization framework has been refined and an interface to the Mathematica computer algebra system has been added. Using SIESTA and the new approach with Bernstein polynomials, we have solved several problems and demonstrated its advantages. We have worked on the minimization of the leakage current of a new two transistor storage cell, on a calibrated model of P interstitital cluster formation and dissolution in Si, and on extracting the diffusion parameters of As in Si after predeposition matching up to 19 measurements.

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Advanced Algorithms for Cellular Topography Simulation

Andreas Hössinger

For the three-dimensional simulation of etching and deposition processes, cellular-based algorithms have advantages compared with polygonal-based algorithms and level-set algorithms due to their high robustness. For instance, the formation of voids which is a very serious problem for polygonal-based algorithms is implicitly handled and therefore no complicated collision detection algorithms are required.

Nevertheless, the major drawback of the cellular-based simulators is the cellular data format. On the one hand the cellular resolution is normally not very high because the memory requirement increases dramatically by choosing a higher accuracy. But when a topography simulator is applied to front end process simulation, also thin layers like the gate oxide in a MOS transistor have to be resolved accurately. This means that the cell size should be smaller than one tenth of the gate oxide thickness. For instance, if the volume of the simulation domain is 1 μm^3 and the gate oxide thickness is 5 nm then 8 billion cells will be necessary to discretize the simulation domain, while the error is still not less than 10%.

Additionally, a cellular-based simulator suffers from the fact that the discrete geometry representation is normally not compatible with the polygonal-based data format of other process simulators. As a consequence, several conversions between the cellular and the polygonal data formats are necessary if the

cellular-based simulator is integrated into a process flow. Errors of the order of the resolution of the cellular representation are introduced by each conversion. In the worst case small structures can even get lost.

To overcome these problems we have developed a new advanced hybrid approach for three-dimensional etching and deposition simulation based on the cellular data format. On the one hand this approach significantly reduces the memory requirement of the simulator, while on the other hand it attacks the discretization error problem. The idea is to couple a cellular-based simulator with a so-called wafer-state server which holds the complete information describing the simulation domain in a volume mesh discretized format. During the simulation the topography simulator exchanges information with the wafer-state server. Therefore, there is no need for discretizing the whole simulation domain in the cellular data format. Only the area passed by the process front is discretized, which significantly reduces the memory requirement. After finishing the topography simulation, a volume-based representation of the modified simulation domain is generated by cutting the wafer-state data with the process front. Consequently, no conversion to a polygonal data format is necessary afterwards.

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Three-Dimensional Device Simulation with MINIMOS-NT

Robert Klima

With the increasing integration density of integrated circuits, the feature sizes of the devices become smaller and smaller. Nowadays MOS device structures with gate lengths below 100 nm are of high industrial interest. Due to the miniaturization the three-dimensional properties of the device structures become more pronounced, and the device geometries noticeably influence the electrical characteristics and the behavior of the device. Therefore, three-dimensional device simulations have to be performed. Typical examples are short and narrow channel effects, and punch-through effects in Dynamic Random Access Memory (DRAM) cells.

Within the last two years MINIMOS-NT has been extended to a full three-dimensional device simulator, where the old PIF-based (Profile Interchange Format) libraries have been replaced by a more flexible one supporting one-, two- and three-dimensional grids and attributes. Due to the lack of a standardized, commonly used general device description format we have decided to use a library instead – the so-called wafer-state server – which supports a reader and a writer module for several available device description formats. MINIMOS-NT now provides a powerful quantity server, which is independent from libraries used for reading and writing the input files and supports one-, two-, and three-dimensional attributes and operations. The libraries for geometry support and grid generation are completeley separated from the simulator to be more flex-

ible. MINIMOS-NT is now able to read any kind of grid, once it is supplied. Therefore grids like tensor product grids, triangular grids, tetrahedral grids, or unstructured grids can be read.

For effective mixed-mode simulations, information about the dimensionality of a device is hidden. Therefore, an object-oriented design has been used to handle information of the devices being simulated. This approach allows one-, two-, and three-dimensional devices to be used within a circuit at the same time.

In three-dimensional simulations the equation systems to be solved are very large. The computational costs increase dramatically. So, performance is one of the main issues, and performance analyses over all modules have been done to determine the critical issues. Various algorithms have been optimized. To guarantee short simulation times some further optimizations like appropriate data structures and data management are initialized to reduce the access time to the most frequently used data. Furthermore, the quality of the grid and the number of grid points become a crucial factor. Since simulation times and memory consumption increase in three dimensions, optimized grids help to speed up simulation. Too coarse grids in the third dimension deteriorate the results.

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NanoTCAD

Robert Kosik

Modern ultra-small devices are mesoscopic systems with physical dimension on the scale of the electron coherence length. When designing such devices it is mandatory to take quantum mechanical effects into account.

The Wigner formulation of quantum mechanics is a powerful tool for modeling, because it allows for a mathematical description in close analogy to the classical case. The Wigner equation is the quantum analogy of the Liouville equation, the Wigner function is the analogy of a phase space distribution. Like a classical distribution function the Wigner function is real, but in general it also takes on negative values, and hence cannot be naively interpreted as a probability distribution.

Starting from a full quantum mechanical description of electron-phonon interaction, we develop a hierarchy of semi-classical transport equations with the Boltzmann equation at the low end of the hierarchy. These equations account for quantum effects at different levels of approximation.

Over the last three decades the Monte-Carlo method has evolved into a reliable and frequently used tool that has been successfully employed to investigate a great variety of transport phenomena in semiconductors and semiconductor devices. By using the Wigner formulation it is possible to generalize classical Monte-Carlo algorithms to the quantum case. Quantum Monte-Carlo is then used for the simulation of dissipative transport processes.

First, Monte-Carlo algorithms are formally developed for the solution of the derived set of transport equations. For this, integral representations of the transport equations have to be found. An integral equation is then iteratively substituted into itself yielding the Neumann series, which is finally approached by the numerical MC method for evaluating integrals and series of integrals.

The algorithms are implemented and tested and their performance and applicability to various conditions and structures is investigated. Compared with the classical case there is an additional level of difficulty, known as the negative sign problem. Negative values in the Wigner distribution can cause a deterioration of the convergence of the algorithm.

Transport equations of manageable complexity have to be identified. Effects such as collision broadening, intra-collisional field effect or memory effects can be numerically demonstrated. A solver for selected transport equations based on the Monte-Carlo method is under construction and will be employed to study the resonant tunneling structure.

Robert Kosik was born in Eisenstadt, Austria, in 1969. He studied technical mathematics at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1996. After his community service he joined the 'Institut für Mikroelektronik' in October 1998, where he is currently working on his doctoral degree. His scientific interests include computational physics and applied mathematics.

Statistical Enhancement and Variance Estimation in Monte-Carlo Simulation

Hans Kosina

Monte-Carlo simulation of semiconductor devices requires measures to enhance the statistics in phase space regions of interest that are sparsely populated. There are two general classes of statistical enhancement techniques, namely population control techniques and event bias techniques. To date virtually all Monte-Carlo device simulation codes utilize population control techniques, whereas the event bias technique, introduced in the field of semiconductor transport only one decade ago, has found no application.

The Single-Particle Monte-Carlo method is generally used to solve the stationary boundary value problem defined by the semi-classical Boltzmann equation. A theoretical analysis of this Monte-Carlo algorithm has been carried out, which begins with the transformation of the stationary Boltzmann equation into an integral equation. Because the equation obtained describes the evolution back in time and we are aiming at a forward Monte-Carlo algorithm, the conjugate equation needs to be formulated. The elements of the Neumann series of the conjugate equation are finally evaluated by means of Monte-Carlo integration. Using this mathematically-based approach the Single-Particle Monte-Carlo method is derived in a formal way. For the first time, the independent, identically distributed random variables of the simulated process have been identified, allowing to supplement this Monte-Carlo method with the natural stochastic error estimate.

Furthermore, the extension of the Monte-Carlo estimators to the case of biased events has been derived. The kernel of the conjugate equation yields the natural probabilities which are generally employed for the construction of the particle trajectory. However, for the Monte-Carlo integration of the terms of the Neumann series one may choose probabilities different from the natural ones. The motivation for using such arbitrary probabilities is the possibility to guide particles towards phase space regions of interest to enhance statistics. In this work carrier diffusion against a retarding electric field has been enhanced by the introduction of artificial carrier heating. The probability for phonon absorption has been increased at the expense of phonon emission, a measure which raises the probability of a numerical particle to surmount an energy barrier. In regions with a small field, where transport is diffusion-dominated, the distribution of the scattering angle has been biased so as to induce artificial carrier diffusion.

Hans Kosina was born in Haidershofen, Austria, in 1961. He received the 'Diplomingenieur' degree in electrical engineering and the Ph.D. degree from the 'Technische Universität Wien' in 1987 and 1992, respectively. He was with the 'Institut für flexible Automation' for one year, and in 1988 he joined the 'Institut für Mikroelektronik' at the 'Technische Universität Wien'. In summer 1993 he held a visiting research position at the Advanced Products Research and Development Laboratory at Motorola, Austin, in summer 1999 a research position at the TCAD department at Intel, Santa Clara. In March 1998 he received the 'venia docendi' in the field of 'Microelectronics'. His current interests include device simulation, modeling of carrier transport and quantum effects in semiconductor devices, new Monte-Carlo algorithms, and computer aided engineering in VLSI technology.

A Wigner Equation for the Nanometer and Femtosecond Transport Regime

Mihail Nedjalkov

The quantum transport in far from equilibrium conditions is determined not only by the nanoscale of the device potential, but also by dissipative processes due to interaction with phonons. A rigorous inclusion of the electron-phonon interaction is provided by the generalized Wigner function which along with the electron coordinates also depends on the phonon occupation numbers. The reduced Wigner function, which is obtained by taking the trace over the phonon coordinates, is of interest. An exact equation only for the reduced Wigner function cannot be obtained, since the phonon trace operation does not commute with the interaction Hamiltonian.

A model equation for the reduced Wigner function has been obtained after a hierarchy of approximations. The equation treats the coherent part of the transport imposed by the nanostructure potential at a rigorous quantum level. It is general enough to account for the quantum effects in the interaction with phonons. These are collision broadening associated with the lack of energy conservation in the scattering process, collision retardation due to the memory character of the equation, and the intra-collisional field effect which is the action of the field during the collision process. The analysis of the equation reveals a novel quantum effect which is due to the correlation between the interaction process and the space component of the Wigner path. The interaction process has a finite duration. During the scattering process the path is shifted in the

real space by a half of the phonon momentum. The equation obtained becomes nonlocal in the real space which is in contrast to the Wigner equation which accounts for the device potential only.

The approximations leading to this equation include a weak scattering limit in the phonon interaction, an assumption of an equilibrium phonon system, a mean phonon number approximation and an effective field in the scattering-Wigner potential correlation.

For the case of a homogeneous field the equation reduces to the Levinson equation. The classical limit in the phonon interaction leads to a Wigner equation, where along with the Wigner potential operator also the Boltzmann scattering operator is present. Finally the classical limit in the Wigner potential recovers the Boltzmann equation.

Mihail Nedjalkov was born in Sofia, Bulgaria in 1956. He received the Master's degree in semiconductor physics at the Sofia University 'St. K.Ohridski' in 1981 and the Ph.D degree at the Bulgarian Academy of Sciences (BAS) in 1990. For twelve years he worked at the Department of Physical Analysis and Theoretical Research at the 'Institute of Microelectronics', Sofia. In 1993 he joined the Center for Informatics and Computer Technology, BAS. He was visiting researcher at the Universities of Bologna, 1992, Modena, 1994 and 1995, and Frankfurt, 1997. Since 1998 he has been holding a visiting research position at the 'Institut für Mikroelektronik' at the 'Technische Universität Wien'. Besides the national research projects, he participated in INFM (Italy) and FWF (Austria) projects. Currently he is supported by the European Commission project NANOTCAD. His research interests include numerical theory and application of the Monte-Carlo method, physics and modeling of Boltzmann and quantum transport in semiconductors and devices.

Industrial Application of Device Simulation

Vassil Palankovski

Heterojunction Bipolar Transistors (HBTs) and High Electron Mobility Transistors (HEMTs) are among the most advanced semiconductor devices. They well match today's requirements for high-speed operation, low power consumption, high integration density, low cost in large quantities, and operation capabilities in the frequency range from 0.9 to 215 GHz. HBT ICs are used for microwave power and low power wireless communications applications, hand-held communication, and high-speed digital data transmission. HEMT ICs are used for local multi-point distribution services for broadband Internet access (LMDS), for automotive cruise control (ACC) radar, and for high-speed transmission (40 Gbit/s and beyond).

An overview of the state-of-the-art of heterostructure RF-device simulation for industrial application has been presented. The work has included a detailed comparison of device simulators and current transport models to be used, and has addressed critical modeling issues. Results from hydrodynamic simulations of HBTs and HEMTs with MINIMOS-NT have been demonstrated to be in good agreement with the measured data. The models and the model parameters have been checked against several independent HEMT and HBT technologies to obtain one concise set used for all simulations. The examples have been chosen to demonstrate how such well-calibrated tools can address technologically important issues, such as process variation or reliability.

The manufacturing process with shrinking technology is becoming so complicated that using simulation in a predictive manner has been recognized as an integral part of any advanced technology development. In order to satisfy predictive capabilities the simulation tools must capture the process as well as device physics. Before going to final production one can optimize the process steps and estimate device performance characteristics such as threshold voltage, saturation current, leakage current, and circuit speed.

A novel methodology for the characterization of subquartermicron CMOS technologies has been created. It involves process calibration, device calibration employing two-dimensional device simulation and automated TCAD optimization, and, finally, transient mixed-mode device/circuit simulation. The proposed methodology has been tested on 0.25 μm technology and has been applied to 0.13 μm technology to predict circuit performance. The simulation results have shown an excellent agreement with available experimental data. This approach can be extremely beneficial in the early stages of process development for an estimate of device performance.

Vassil Palankovski was born in Sofia, Bulgaria, in 1969. He received the diploma degree in electrical engineering from the Technical University of Sofia in 1993. Afterwards he worked in the telecommunications field for three years. He joined the 'Institut für Mikroelektronik' at the 'Technische Universität Wien' in May 1997, where he received the doctoral degree in technical sciences in 2000 and is currently working as a post-doctoral researcher. In summer 2000 he held a visiting research position at LSI Logic Corp., Milpitas, California. His scientific interests include device and circuit simulation, heterostructure device modeling, and physical aspects in general.

Optimization of Smart Power Devices

Jong Mun Park

Smart power ICs and devices, which monolithically integrate low-loss power devices and a control circuitry, including various protections and functions on the same chip, are emerging as viable alternatives to discrete circuits in a wide variety of applications. These ICs improve the reliability, reduce the volume and weight, and increase the efficiency of the system. Considerable effort has been spent on the development of smart power devices for automotive electronics, computer peripheral appliances, and portable equipment, such as cellular phones or video cameras.

Commonly used smart power devices are the LDMOS and LIGBT implemented in bulk silicon or SOI (Silicon on Insulator). The main performance parameters for these devices are the specific on resistance (Rsp), the breakdown voltage (BV), and the switching characteristics. The first two parameters are inversely related to each other. Reducing Rsp while maintaining the BV rating has been the main issue of the smart power devices. The optimization of the smart power devices is done using the two-dimensional device simulator MINIMOS-NT.

One of the key issues in the realization of smart power technology is the isolation of power devices and low-voltage circuitry. SOI technology constitutes an attractive alternative to the traditional junction isolation. When high-voltage devices over 100 V are integrated on SOI wafers, the isolation area between devices shrinks and lower leakage currents result in

greatly improved high temperature performance, thus enlarging the SOI market. The breakdown voltage is a function of the thickness of silicon and buried oxide layer. The buried oxide helps sustaining a high electric field which results in high breakdown voltage. However, the operation of SOI power devices is limited by self-heating occuring during switching or fault conditions such as short circuit. The buried oxide underneath the device is a good thermal insulator, so the temperature rise inside SOI power devices can be much higher than in bulk silicon devices. Self-heating of SOI power devices could result in serious reliability problems during operation in a high temperature environment. This problem could be solved by using partial-SOI technology or by using buried insulators with good thermal conductivity. The main objective in the design of SOI smart power devices is to optimize device parameters such as on-resistance and breakdown voltage, as well as switching performance and self-heating. Extensive two-dimensional analysis using MINIMOS-NT is performed to achieve optimum design procedures.

Jong Mun Park was born in Seoul, Korea, in 1961. He studied electronics engineering at the 'Hanyang University', where he received the degree of 'Master of Science' in 1985. Afterwards he was a senior researcher at the Power Semiconductor Group at KERI, National Laboratory in Korea, where he carried out several projects for developing power semiconductor devices. He joined the 'Institut für Mikroelektronik' in March 2001, where he is currently working on his doctoral degree. His scientific interests include optimization and modeling of power semiconductor devices, Silicon Carbide (SiC) power devices, smart power ICs and Intelligent Power Modules (IPMs).

New Challenges of Heterostructure Device Simulation

Rüdiger Quay

Heterostructure Field Effect Transistors (HFETs) or High Electron Mobility Transistors (HEMTs) are among the three fastest terminal devices existing. They find their application in communications, sensing, and radar, when high output power, high gain, and low noise properties are required.

Device simulations of pseudomorphic AlGaAs/InGaAs/GaAs and InAlAs/InGaAs HEMTs on both InP and GaAs substrates with MINIMOS-NT have been developed significantly further. One focus of the work is the material-dependent analysis of InAlAs/InGaAs HEMTs based on InP or of metamorphic devices on GaAs. Monte-Carlo simulations have been carried out to fill the gaps in the knowledge of the material properties for the metamorphic devices. Furthermore, the generation/recombination mechanisms and their impact on III-V semiconductor device performance have been investigated. Although the HFET is considered a unipolar device, a complete set of generation/recombination models and parameters including Auger, direct recombination, Shockley-Read-Hall and Impact Ionization for GaAs and InP based semiconductors has been developed. A second aspect has been the calibration of electrothermal simulation in agreement with three-dimensional chip simulation to obtain realistic boundary conditions and lattice temperatures. Statistical principles have been applied for the industrial optimization process using device simulation in order to obtain both process-safe

and optimized devices. A strong development effort has been made for high-power HEMT based on GaN semiconductors. For the AlGaN/GaN material system a complete set of material models has been included in MINIMOS-NT based on the state-of-the-art of material research. Piezoelectric effects are included in the simulation. Device simulations of l_g= 200 nm $Al_{0.25}Ga_{0.75}N$/GaN HFET devices have been successfully performed using MINIMOS-NT, showing good agreement with the measured data. Interface transport for the large band gap discontinuities has been demonstrated for Al concentrations up to x= 0.3 in the barrier in agreement with the measurements.

Further challenges are the development of material models for high field transport and impact ionization in agreement with the progress of material research for AlGaN/GaN and InGaN/AlGaN heterostructures.

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Low Temperature Analysis with MINIMOS-NT

Rodrigo Rodríguez-Torres

Microelectronics is reaching the physical limits. The Ultra Large System Integration yields high performance integrated systems at low cost. Improvement of such systems is complex because multiple second and higher order effects must be taken into account. Those effects considerably affect the general performance of integrated systems at room temperatures.

Parameters like electron mobility or thermal resistance are influenced by the temperature of the system. As a result, the general performance can be increased by lowering the operating temperature. Cooling systems down to 77 K (Liquid Nitrogen temperature) are available nowadays at reasonable costs. Merit figures from systems are greatly improved. One requirement for design is to assure that the physical models used will work properly in such conditions.

Unfortunately, low temperature analysis involves different concepts that are ignored in room temperature analysis: Incomplete ionization of dopants must be taken into account at low temperature. Parameters such as effective mass, mobility, and ionization rates are temperature-dependent.

The simulation of semiconductor devices in low temperature regimes is more difficult from a numerical point of view. For example, the intrinsic carrier concentration is usually taken as a scaling parameter in order to get a dimensionless concentration. However, at low temperatures, this parameter can show

large variations, up to 20 orders of magnitude. The probability of getting overflow or underflow problems during the numerical solving process increases considerably. MINIMOS-NT has been tested under such conditions. Historically, the development of this simulator has taken such viewpoints into account.

Sensitivity is a typical example of merit figure improvement on low temperature operation for MAGFET devices. MAGFETs, magnetic sensors based on MOS devices, show a better performance in the low temperature regime because the mobility of the carriers in the inversion layer is increased and leads to an increased drain current. As a result, the signal to noise ratio (SNR) is improved, i.e., the device is able to detect smaller magnetic fields just by operating them at a low temperature. Besides, noise and other parasitic effects are also reduced.

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Accurate Three-Dimensional Interconnect Simulation

Rainer Sabelka

On-chip interconnects have been identified as the bottleneck for further improvements in the circuit speed of next generation integrated circuits. While downscaling generally results in faster semiconductor devices, the performance of the metal interconnect lines is limited by various parasitic effects like attenuation caused by resistive voltage drops, self-heating due to losses, delay times, crosstalk caused by capacitive or inductive coupling or by the substrate, reflections incurred by discontinuities, skin-effect and eddy currents, for example in on-chip spiral inductors. With the introduction of new materials such as copper and low-k dielectrics, parasitic effects could be reduced to a certain degree, but not eliminated. Hence, interconnect parasitics must be taken into account during the design process at an early stage and highly accurate models are required, especially for designs with reduced safety margins close to the physical limits.

The SAP (Smart Analysis Programs) have been developed for this purpose. This simulation package contains tools for highly accurate extraction of parasitic capacitances, resistances, and inductances, quasi-electrostatic simulation, and investigation of the thermal behavior of interconnect stacks. Special attention has been directed at an efficient implementation concerning both runtime and memory consumption. Compared with other (commercial) tools, the simulator has the ability to perform calculations with anisotropic dielectric materials and cou-

pled electro-thermal simulations with temperature-dependent material properties. The finite element method (FEM) is used for the numeric solution of the partial differential equations.

For highly accurate simulations it is essential to model the simulation domain geometrically as exactly as possible. Two- and three-dimensional solid modelers are used either to construct the simulation geometry directly from an input deck, to generate it automatically from layout, or to use the output of a lithography and/or topography simulation. The simulation grid is generated either generated by a layer-based technique or with a fully unstructured Delaunay mesher.

A three-dimensional visualization program has been developed to display the calculated distributed scalar and vector fields such as potential, temperature, and current density by means of contour faces, streamlines, cuts, and surface representation.

Recent improvements in the Smart Analysis Programs include an update to the latest version of the three-dimensional grid generator deLink, a new interface to layout data in CIF or GDSII format, enhanced visualization capabilities, an implementation of flat vertical contacts, and a number of bug fixes.

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Study of Quantum Effects in MOS Devices

Christian Troger

Numerical simulation in the field of semiconductor device development has advanced to a valuable, cost-effective and flexible facility. The most widely used simulators are based on classical models as they need to satisfy time and memory constraints. To improve the performance of field effect transistors such as MOSFETs and HEMTs these devices are continuously scaled down in their dimensions. Consequently, the characteristics of such devices are getting more and more determined by quantum mechanical effects arising from strong transversal fields in the channel.

An approach based on a two-dimensional electron gas is used to describe the confinement of the carriers. Quantization is considered in one direction only. For the derivation of a one-dimensional Schrödinger equation in the effective mass framework a non-parabolic correction for the energy dispersion according to Kane is included. For each subband a non-parabolic dispersion relation characterized by subband masses and subband non-parabolicity coefficients is introduced and the parameters are calculated via perturbation theory.

The method using the non-parabolic subband dispersion relation has been implemented in a software tool that performs a self-consistent solution of Schrödinger - and Poisson - equation for a one-dimensional cut through a MOS structure or heterostructure. The calculation of the carrier densities is per-

formed assuming Fermi-Dirac statistics. In the case of a MOS structure a metal or a polysilicon gate is considered and an arbitrary gate bulk voltage can be applied. This allows the investigation of quantum mechanical effects in capacity calculations, the comparison of the simulated data with measured CV curves and the evaluation of the results obtained with a quantum mechanical correction for the classical electron density. The behavior of the defined subband parameters is compared with the value of the mass and the non-parabolicity coefficient from the model of Kane.

Finally, the presented characterization of the subbands is applied to the carrier transport simulation in a single particle Monte-Carlo program. The input parameters for the developed Monte-Carlo program are supplied by the self-consistent Schrödinger Poisson solver in the form of subband parameters and overlap integrals, specified as effective widths for the wavefunctions.

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