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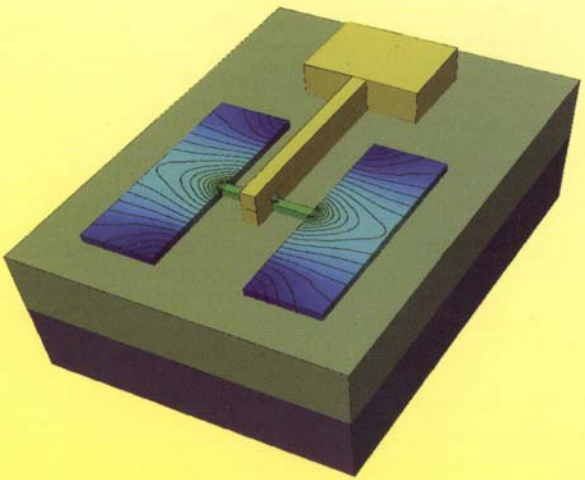

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Preface

Erasmus Langer and Siegfried Selberherr

This brochure is the fourteenth annual research review of the Institute for Microelectronics. The staff financed by the Austrian Federal Ministry of Education, Science, and Culture consists of ten full-time employees: the dean of the Faculty of Electrical Engineering and Information Technology, the head of the institute, one additional professor, four scientists, a secretary, and two technical assistants. Seventeen additional scientists are funded through scientific projects supported by our industrial partners, by the Austrian Science Fund (FWF), and by the EC Framework Programme.

In addition to the two running EC projects MAGIC-FEAT and NANOTCAD, a third project within the "Information Society Technology Programme (IST)" named MULSIC has been started. We proudly report that a further project has already been granted but has not yet commenced officially. We are glad to be able to report that our industrial partners have continued their cooperation. Furthermore, a new cooperative research partnership with HEWLETT-PACKARD, Shrewsbury, USA has been successfully established.

Due to the expected reform of the Austrian university scene by a new organizational law some valuable man power will be wasted which could be used much more efficiently for scientific work. Nevertheless, owing to the successful and promising cooperation with famous industrial partners and the scientific output of our institute, we look at the next year with expectations as high as ever.

Erasmus Langer was born in Vienna, Austria, in 1951. After having received the degree of 'Diplomingenieur' from the 'Technische Universität Wien' in 1980 he was employed at the 'Institut für Allgemeine Elektrotechnik und Elektronik'. In 1986 he received his doctoral degree and in 1988 he joined the 'Institut für Mikroelektronik'. In 1997 he received the 'venia docendi' on 'Microelectronics'. Since 1999 Dr. Langer has been head of the 'Institut für Mikroelektronik'. His current research topic is the simulation of microstructures using High Performance Computing paradigms.

Siegfried Selberherr was born in Klosterneuburg, Austria, in 1955. He received the degree of 'Diplomingenieur' in electrical engineering and the doctoral degree in technical sciences from the 'Technische Universität Wien' in 1978 and 1981, respectively. Dr. Selberherr has been holding the 'venia docendi' on 'Computer-Aided Design' since 1984. Since 1988 he has been the head of the 'Institut für Mikroelektronik', and since 1999 dean of the 'Fakultät für Elektrotechnik'. His current topics are modeling and simulation of problems for microelectronics engineering.

Renate Winkler was born in Vienna, Austria, in 1960. She joined the 'Institut für Mikroelektronik' in November 1993. Since that time she has been in charge of the organizational and administrative work of the institute.

Ewald Haslinger was born in Vienna, Austria, in 1959. He joined the 'Institut für Mikroelektronik' in December 1991. Since that time he has been in charge of organizational, administrative and technical work of the institute.

Manfred Katterbauer was born in Schwarzach St.Veit, Austria, in 1965. He joined the 'Institut für Mikroelektronik' in February 1995. Since that time he has been in charge of all technical hardware and software work of the institute.

Three-Dimensional Simulation of Non-Linear Dopant Diffusion

Hajdin Ceric

Accurate control of dopant diffusion is becoming a critical issue for achieving shallow junctions which are basic building blocks for the realization of modern deep-submicrometer devices for ULSI circuits. Modern models of dopant diffusion take non-equilibrium diffusion and reaction of point defects and defect-dopant pairs into account, considering their charge states, and the dopant inactivation by introducing a dopant clustering reaction.

These complex models of dopant diffusion can be described by a system of non-linear partial differential equations (PDE). Depending on the various process conditions, different diffusion models have to be applied. Since many dopant profiles are box-shaped, diffusion often requires a three-dimensional investigation.

The simulated region generally consists of several different material segments, each requiring an adequate physical model. In order to realistic simulation in such cases a PDE solver is needed which can simultaneously handle systems of non-linear PDEs for each segment of the region together with a model equation describing dopant transport between the segments (Segregation).

For this purpose and for the purpose of oxidation simulation, the program FEDOS (Finite Element Diffusion and Oxidation Simulator) has been developed. FEDOS facilitates simulations

of a sequence of diffusion and oxidation process steps taking changing ambient conditions into account. For each process step it is possible to choose appropriate diffusion or oxidation models from the FEDOS model library.

Segregation models are an important issue in the diffusion and oxidation simulation. A new numerical approach for integrating such models in the finite element scheme has been implemented in FEDOS. Extensive simulations have proven numerical quality of the approach and high consistency of the results with the physical phenomenon of segregation.

The numerical solution of a PDE system by means of the finite element method causes a discretization error. There are several approaches for a posteriori error estimation which is conveyed locally on each element of the spatial discretization. According to this estimated error the finite element grid is adapted for the simulation of the next time step. In FEDOS a method for automated grid adaptation based on the robust recursive refinement-coarsening scheme has been implemented. The method controls the grid density in such a way as to allow efficient simulation with defined accuracy.

Hajdin Ceric was born in Sarajevo, Bosnia and Herzegovina, in 1970. He studied electrical engineering at the Electrotechnical Faculty of the University of Sarajevo and at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 2000. He joined the 'Institut für Mikroelektronik' in June 2000, where he is currently working on his doctoral degree. His scientific interests include interconnect and process simulation.

Three-Dimensional Mesh Generation for Electronic Device Simulation

Johann Cervenka

For the development of today's electronic devices the simulation of fabrication processes and physical effects is a key point in the development of competitive products. Coming along with the complexity of the device structures the used numerical models are three-dimensional. Therefore the device simulators have to be expanded for three dimensions. Especially the simulation results should be delivered within tolerable calculation times and memory limits. Because of the influence of the simulation grid on the quality of the simulation, adaptive grid generators must be used to achieve accurate results.

For three-dimensional device simulation, tetrahedral grids are usually used. A big advantage of these meshes is that they are applicable to arbitrary geometries of the simulation structures. However, the grid density cannot be varied independently. While using ortho-product grids, the grid density can be varied independently in the three directions of space, the drawback being that with complex and nonplanar device structures the amount of grid points will be boosted dramatically. Therefore, a method has been developed where the benefits of both approaches are combined.

The simulation domain is treated as a resistor, with two electrodes on the top and at the bottom where a voltage is applied. After solving the discrete Laplace equation inside the resistor area the grid points are placed at the intersections of selected

equipotential lines and field lines. Then the point set is tetrahedrized. The final tetrahedration, and also the generation of the initial grid for solving the Laplace equation, are performed using the Delaunay grid generator deLink, which has been developed at the institute.

To guarantee a high flexibility of the simulations tools, the WAFER STATE SERVER has been developed. It stores and manages the necessary geometry and material data of the used device structures. It also facilitates the functional separation of the different simulation tools and offers the possibility of constructing modular packages. Each functional unit has to communicate with the WAFER STATE SERVER through defined interfaces and need not know about other packages' data requirements. It has therefore been necessary to develop an interface where the grid data is provided for the finite-voluming solver of the device simulator. Because this functionality is closely linked to grid generation, a library has been developed which can be used by both the grid generator and the WAFER STATE SERVER .

Johann Cervenka was born in Schwarzach, Austria, in 1968. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1999. He joined the 'Institut für Mikroelektronik' in November 1999, where he is currently working for his doctoral degree. His scientific interests include three-dimensional mesh generation as well as algorithms and data structures in computational geometry.

Analysis of Ultra Short Channel Devices with High-κ Gate Dielectrics

Klaus Dragosits

According to the International Technology Roadmap for Semiconductors (ITRS), the gate oxide becomes one of the critical issues for short channel devices. If SiO_2 is used the proposed layer thicknesses are getting smaller than 1 nm, thus leading to massive direct tunneling from the gate into the substrate. To reduce this parasitic effect, alternative dielectrics with higher κ values are used instead of SiO_2.

After studying effects related to the modified device geometry, the focus of our research has been put on an accurate modeling of the carrier profile near the interface. This is motivated by the following notion: As a consequence of the introduction of new gate dielectric materials, the properties of the interface change. The assumptions on surface scattering and its influence on the carrier mobility need to be reconsidered, especially as surface mobility parameters were extracted from classical models assuming that the charge is concentrated at the surface. This is definitely not the case if quantization is taken into account, and even qualitative conclusions on how the increase of surface scattering impacts on the device properties are questionable.

From the analysis of the published quantum correction models, one can conclude that classical device modeling leads to two significant inaccuracies concerning the carrier concentration near the channel surface. First, the splitting of the con-

duction band into several discrete eigenvalues is not accounted for. Second, classical models do not consider that the shape of the wave functions reduces the carrier concentration near the surface. A rigorous approach to simulate the carrier concentration has to account for both effects, by offering approximations for the wave function and the actual band structure.

We model the first of these effects by a reduction of the density of states N_C near the interface following an exponential law. The basic idea of our model for the energy band structure is to replace the effective band edge near the surface by the first discrete eigen energy. This seems reasonable as quantum mechanical calculations show that usually over 90% of the carriers are in this energy band.

The new model was checked by simulations of a MOS capacitor and the results were compared with a self-consistent Schrödinger-Poisson solver. An excellent fit between the results from our new model and the quantum mechanical calculations has been obtained, especially the carrier profile and the onset of inversion have been predicted very accurately. The ability to reproduce the channel profile enables a precise simulation of state-of-the-art CMOS devices.

Klaus Dragosits was born in Bruck an der Mur, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the 'Diplomingenieur' and the Ph.D. degrees in 1996 and 2001, respectively. He joined the 'Institut für Mikroelektronik' in September 1997. He held visiting research positions at Philips Research, Eindhoven, in March 2000, at the Samsung Advanced Institute of Technology, Seoul, in June 2000, and at the European Center of Excellence for Information Technologies at the Bulgarian Academy of Science, Sofia, in August 2001. His scientific interests include device simulation with special emphasis on nonvolatile memory cells, high-k dielectrics, and quantum effects.

Mesh Generation with deLink, Refinement and Visualization

Peter Fleischmann

Features for refinement of an initial mesh have been added to the three-dimensional mesh generation tool deLink. After ion implantation the doping concentration is not necessarily smooth, nor are the gradients. Such conditions require a highly anisotropic mesh density. It is of practical importance to construct an initial anisotropic mesh complying with mesh specifications provided by the application engineer. Such specifications include maximum element sizes given independently for different directions in a certain region. The capability of deLink to provide such mesh spacing commands, whereby non-coordinate-axis-aligned anisotropy and overlapping regions of spacing definitions are supported, can now be controlled via API calls to the deLink library. From the possibly large set of spacing definitions for various regions one global background mesh will be extracted which holds the minimum density at each point complying with the specifications. In such a way an initial anisotropic mesh point distribution is pre-calculated.

With regard to visualization, support has been added to deLink for several new data formats. The various conversion tools have been unified and integrated into deLink to allow automatic detection of the required file type, as well as writing meshes directly in the desired format. Meshes can now be visualized not only through the Visualization Toolkit's (VTK's) native format, but also using MEDIT by INRIA, and TECPLOT from AMTEC. While TECPLOT emerges to be the standard for

three-dimensional visualization of meshes, data, and geometries in TCAD applications, MEDIT provides strong features for the developer like picking and peeling mesh elements.

Another new and important feature of deLink is the ability to detect unreferenced material regions. Especially after topography simulation of deposition steps, the structure boundaries are known, but the material region information might be corrupt or incomplete. In such cases deLink accepts completely or partly missing input region information and assigns new region names to found regions. The application program is then able by a simple point comparison to assign correct material tags to each region. For example, after the deposition of one material, the application might realize that two new regions were found, and is able to restore a complete material region information after receiving the mesh from deLink.

Peter Fleischmann was born in Kabul, Afghanistan, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in December 1994. In December 1997 he was with NEC in Sagamihara, Japan. In February 2000 he finished his Ph.D. thesis at the 'Institut für Mikroelektronik' where he is currently enrolled as a post-doctoral researcher. In fall 2000 he spent two months as a visiting scholar at the University of California at Berkeley. His research interests include mesh generation, CAD, and computational geometry.

Simulation of Tunneling Effects with MINIMOS-NT

Andreas Gehring

With the ongoing reduction of minimum feature sizes, the effects of tunneling through insulating layers play an increasing role for the simulation of contemporary semiconductor devices. The general-purpose device simulator MINIMOS-NT has been extended to account for these effects, and several applications have been investigated.

Examples are multi-barrier tunneling devices such as the PLEDM (Planar Localized Electron Drive Memory), which have been proposed as non-volatile memories offering extremely high retention times. In such devices, the charge on the floating gate contact is provided via tunneling of electrons through a stack of insulating layers. However, common tunneling models such as the Fowler-Nordheim or Bardeen model fail to describe the charging/discharging characteristics of these devices because they assume a triangular- or trapezoidal-shaped energy barrier. For that purpose, the transfer-matrix method has been implemented to estimate the transmission coefficient. With this method it is possible to calculate the transmissivity of arbitrary-shaped energy barriers.

CMOS devices which incorporate gate stacks of SiO_2 and a layer of high-κ dielectric are another application where the transfer-matrix method is necessary for tunneling current evaluation. Such devices have been proposed to block tunneling currents while retaining control over the inversion charge in the

channel of devices with effective oxide thicknesses below 2 nm. A high-κ gate stack consists of an underlying layer of SiO_2, which is necessary due to the poor thermal stability of high-κ materials on silicon, and a layer of a high-κ dielectric on top. Thus, the energy barrier deviates from the trapezoidal shape showing a kink. The transfer-matrix method can be used to compute the transmission coefficient of such structures.

Furthermore, the reduced channel length in contemporary sub-quartermicron CMOS devices causes hot carrier tunneling due to the high electron temperature near the drain side of the channel. The electron energy distribution function in such cases turns out to have a non-Maxwellian shape. However, tunneling models are usually based on the assumption of a cold or heated Maxwellian shape of the distribution function. It has been seen that the heated Maxwellian approximation leads to wrong results for turned-on devices with channel lengths below 250 nm. A new expression for the distribution function which is based on six moments of the Boltzmann equation takes the non-Maxwellian shape of the distribution function into account and can be used for gate current prediction in this regime.

Andreas Gehring was born in Mistelbach, Austria, in 1975. He studied communications engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in March 2000. He joined the 'Institut für Mikroelektronik' in April 2000, where he is currently working on his doctoral degree. In summer 2001 he held a visiting research position at the Samsung Advanced Institute of Technology in Seoul, South Korea. His scientific interests include device simulation, memory cell techniques and semiconductor physics in general.

Using Six Moments of Boltzmann's Equation for Device Simulation

Tibor Grasser

An accurate description of non-local effects is of utmost importance for modern semiconductor devices. In particular, the distribution function has to be modeled properly as it is inherently linked with hot-carrier effects. Within the framework of hydrodynamic and energy-transport models only the average energy is known which does not provide enough information about the shape of the distribution function.

To overcome the limitations of the energy-transport models we have developed a consistent transport model based on six moments of Boltzmann's equation. In addition to the concentration and the carrier temperature, as provided by the energy-transport models, we have obtained the average of the square energy which we have mapped to a new solution variable, representing the kurtosis of the distribution function. Monte-Carlo simulations show that the kurtosis provides the information to differentiate between the channel region and the transition region from channel to drain where the hot carriers from the channel mix with the cold carriers from the drain. Furthermore, the kurtosis describes the changing shape of the distribution function throughout the whole device. This is important for short-channel devices where the distribution function behaves differently than in bulk. Based on this information we have proposed an analytical description for the distribution function which goes beyond the assumption of a Maxwellian shape.

In particular, the modeling of impact ionization is known to be notoriously inaccurate with models based on the local energy. However, accurate calculation of impact ionization rates in macroscopic transport models is becoming more and more important due to the ongoing feature size reduction of modern semiconductor devices. Conventional models which use the average carrier energy as main parameter fail because impact ionization is very sensitive to the shape of the distribution function, in particular to the high-energy tail.

Based on the analytic description of the distribution function we have proposed a new macroscopic impact ionization model which has proven to deliver accurate results for the homogenous case and inhomogeneous cases down to nanoscale devices. In particular, the tail of the impact ionization rate inside the drain area is correctly predicted, which is not possible with models based on the average carrier energy only. The additional accuracy is provided by the kurtosis of the distribution function. As the model involves only state variables of the equation system, it is well suited for the implementation into conventional device simulators.

Tibor Grasser was born in Vienna, Austria, in 1970. He studied communications engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' and the doctoral degree in technical sciences in 1995 and 1999, respectively. He joined the 'Institut für Mikroelektronik' in 1996 where he is currently employed as an Assistant. In 2002 he received the 'venia docendi' on Microelectronics. Since 1997 he has been heading the MINIMOS-NT development group, working on the successor of the highly successful MINIMOS program. His current scientific interests include circuit and device simulation, device modeling, physical and software aspects in general.

Transport Modeling for SOI-MOSFETs

Markus Gritsch

In integrated circuits, SOI technology improves performance over bulk CMOS technology by 25% to 35%, equivalent to two years of bulk CMOS advances. SOI technology also gives 1.7 to 3 times less power consumption. Therefore SOI technology will result in faster processor chips that also require less power, a key requirement for extending the battery life of small, handheld devices that will be pervasive in the future.

To develop and design integrated circuits using SOI technology, it is necessary to be able to properly simulate their behavior using dedicated simulation programs. However, the simulation tools currently available are not capable of predicting a reasonable output characteristics when applying the hydro-dynamic (HD) transport model. Instead, an anomalous decrease of the drain current with increasing drain-source voltage has been observed.

Nevertheless, the applicability of the HD model is desirable, because in contrast to the drift-diffusion (DD) model it takes nonlocal effects into account, which gain importance in the regime of the ever-decreasing minimum feature size of today's devices.

The main difference between the HD and the DD transport models is the presence of the additional energy balance equation. The benefit of the increased computational effort is that the carrier temperature can differ from the lattice temperature. Since the diffusion of the carriers is proportional to their tem-

perature, the diffusion can be significantly higher when using HD transport.

When simulating SOI MOSFETs, this increased diffusion has a strong impact on the body potential, because the hot electrons of the pinch-off region have enough energy to overcome the energy barrier towards the floating body region and thus enter into the sea of holes. Some of these electrons in the floating body are sucked-off from the drain-body and source-body junctions, but most recombine. The holes removed by recombination cause the body potential to drop. A steady state is obtained when the body potential reaches a value which biases the junctions enough in reverse direction so that thermal generation of holes in the junctions can compensate this recombination process. The decrease in the output characteristics is directly connected to the drop of the body potential via the body-effect.

By comparing the HD model with results obtained by Monte-Carlo simulations, an overestimation of the hot carrier diffusion predicted by the HD model has been shown. A modified HD transport model has been developed to overcome this problem, and it has been used successfully to simulate different SOI transistors using the general-purpose device simulator MINIMOS-NT.

Markus Gritsch was born in Zams, Austria, in 1974. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1999. He joined the 'Institut für Mikroelektronik' in May 1999, where he is currently working for his doctoral degree. His scientific interests include circuit and device simulation, device modeling, and physical and software aspects in general.

Inductance Calculation in Interconnects

Christian Harlander

Conventional design techniques were focused primarily on minimizing the chip size. Thus the influence of the interconnects cannot be neglected anymore. Signal delay, inductive and capacitive crosstalk, attenuation of the signal and reliability are becoming important issues. Because of the increasing frequencies and the usage of new materials like copper and low-κ dielectrics, inductive effects gain significance especially for lines, which provide power supply or global busses. A necessary, but not sufficient condition is that the inductive part is of the same order of magnitude as the resistance of the line. In addition, several inequalities describe the area, where inductive effects are not negligible and have to be considered in the design.

For this purpose the Smart Analysis Programs (SAP) can be used to extract inductances. Besides methods based on a numerical solution of Neumann's formula for a precalculated stationary current density distribution, a method based on the magnetic vector potential has been implemented. A frequently used choice for the evaluation of multiple integrals is the Monte-Carlo method because of its simple applicability and the treatment of general integration regions. Associated with this method is a fairly high effort on CPU time, because the search for the associated element of the random point coordinates is time consuming. To reduce the error a high number of function evaluations have to be carried out, where for each evaluation the aligned element with the precalculated current density must be found. The big advantage of the implemen-

tation used is that it bypasses the high computational effort for the element location despite the use of unstructured grid elements. Therefore, first the element is determined from the probability function, followed by localizing the point inside the tetrahedron. Hence, the performance of the Monte-Carlo method is only weakly influenced by the total number of the elements (n), because the effort for the applied binary search algorithm to find the associated element grows with $\log(n)$. Furthermore, the Monte-Carlo method offers a convenient and efficient way of error estimation.

The second method is deterministic and requires the computation of the current density for the right hand side, whereby the magnetic vector potential is obtained by solving the Poisson equation for each coordinate axis separately. This is possible because the three solutions of the Poisson equation are independent and the uniqueness of the magnetic vector potential is guaranteed by the boundary conditions and the assurance of the Coulomb gauge.

Christian Harlander was born in Taxenbach, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1997. He joined the 'Institut für Mikroelektronik' in December 1997, where he is currently working for his doctoral degree in the field of three-dimensional interconnect simulation of multilevel wired VLSI circuits. In winter 2000 he held a visiting research position at Sony, Atsugi, Japan.

Topography Simulation for Etching and Deposition Processes Using the Level Set Method

Clemens Heitzinger

Etching and deposition of Silicon trenches are important semiconductor manufacturing steps for state-of-the-art memory cells and other semiconductor devices such as power MOSFETs. Understanding and simulating the transport of gas species and surface evolution enables to achieve void-less filling of deep trenches, to predict the resulting profiles, and thus to optimize the process parameters with respect to manufacturing throughput and the resulting devices.

When simulating etching and deposition processes for semiconductor manufacturing, an accurate description of moving boundaries is crucial in addition to the proper treatment of chemical and physical processes. In these applications the moving boundary is the surface of the wafer. One approach is to use a cellular format, where the simulation domain is divided into cubic or cuboid cells and each cell either belongs to the exterior vacuum above the wafer or to its interior. Disadvantages of this method are the limited resolution and the fact that computing surface normals and tangents leads to accuracy problems.

The level set method provides an interesting alternative and a solution to the above-mentioned problem. This method is a relatively new one for describing boundaries that can be curves, surfaces or hypersurfaces in arbitrary dimensions, and their

evolution in time. It requires the solution of a partial differential equation and the extraction of the zero level set of its solution.

Using this approach, a general simulator for etching and deposition processes has been developed. It consists of three independent modules, namely the level set module, a surface reaction module, and a module for particle transport, which are used for simulating all common deposition and etching processes. Two strategies for increasing the accuracy of radiosity simulations have been developed. The first method is an algorithm which performs three level set computations in parallel: calculating the signed distance function via a fast marching algorithm, extending the speed function, and moving the narrow band according to the new zero level set. The second method is a coarsening algorithm which ensures fine resolution of the surface in parts of the boundary where it is needed most and lowers the demand on computational resources significantly.

In cooperation with industrial partners, various deposition processes have been simulated and compared to measurements. The good agreement of experiment and simulation validates the models and the applicability of the simulator.

Clemens Heitzinger was born in Linz, Austria, in 1974. He studied Technical Mathematics at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1999. He joined the 'Institut für Mikroelektronik' in February 2000, where he is currently working for his doctoral degree. From March to May 2001 he held a position as visiting researcher at the Sony Technology Center in Hon-Atsugi (Tokyo, Japan). His scientific interests include optimization of semiconductor devices and mathematical modeling for device and process simulation.

Full Three-Dimensional Process Simulation

Andreas Hössinger

With shrinking dimensions of semiconductor devices, more and more effects arise which cannot be analyzed by two-dimensional simulations, since a two-dimensional simulation is not able to describe the influence of corners or other three-dimensional structures. In very small devices, which are already used in modern standard technologies, almost all regions of the devices are located close to corners. Especially these critical devices require three-dimensional simulations to be able to understand their behavior.

This statement applies not only to the simulation of the electrical behavior of the devices, but also to the simulation of the production processes because corner effects or shadowing effects can significantly change the final structure of a semiconductor device.

Several three-dimensional process simulation tools have been developed during the last years. Due to the complexity of modern production processes it is no longer sufficient to look at a single process step, since the individual steps have a strong influence on each other. The problem is that all the process simulation tools use their individual optimized data structures which are not compatible with each other. To solve this problem, the so-called WAFER STATE SERVER has been developed during the last three years at the 'Institut für Mikroelektronik'. It holds the complete information describing the

simulation domain in a volume mesh discretized format, and it provides convenient methods to access these data. The idea was that the simulators make use of these access methods to initialize their internal data structure, and that the simulators report their modifications of the wafer structure to the WAFER STATE SERVER. Thereby a consistent status of the wafer structure can be sustained during the whole process flow with minor activities of the simulators.

During the last year the activities have been focused on the integration of the WAFER STATE SERVER with several three-dimensional process simulators used for topography, ion implantation and annealing simulations. In the course of the integration of the WAFER STATE SERVER into the process simulators most of the access methods to the WAFER STATE SERVER and especially the reporting methods have been designed and implemented.

Andreas Hössinger was born St. Pölten, Austria, in 1969. He studied Technical Physics at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in January 1996. He joined the 'Institut für Mikroelektronik' in June 1996. In 1998 he held a visiting research position at Sony in Atsugi, Japan. In September 2000 he finished his Ph.D. degree at the 'Institut für Mikroelektronik' where he is currently enrolled as a post-doctoral researcher. In 2001 he held a position as visiting researcher at LSI Logic in Santa Clara, CA, USA within the scope of a cooperate research project on three-dimensional process simulation. His research interests include process simulation with special emphasis on three-dimensional applications.

Simulation of Thermal Oxidation

Christian Hollauer

In thermal oxidation the wafer surface of a silicon substrate is converted into silicon dioxide in an oxidizing atmosphere. The chemical reaction starts at room temperature, and the resulting very thin oxide film is called native oxide.

The oxidation rate can be accelerated by subjecting the wafer to various ambients at elevated temperatures. Gases that are typically used are water steam (wet oxidation), oxygen (dry oxidation) or mixtures of both. Dry oxides are commonly used as gate oxides for the Metal Oxide Semiconductor (MOS) technology. The slow growth at moderate oxidation temperatures allows an accurate adjustment of the final thickness. Compared to dry oxidation, wet oxides grow faster. Thus one can find the typical application of wet oxides in isolation structures where thick oxide buffers are needed to suppress electric currents or to ensure high threshold voltage of parasitic transistors.

The growth rate of the thermally grown oxide depends not only on the temperature, but also on the pressure, the crystal orientation, the doping level and the impurity contamination of the silicon substrate as well as on the stress due to a nonplanar wafer surface.

The thermally grown silicon dioxide has excellent mechanical and electrical properties. It is commonly used to provide isolation between single devices, as gate dielectrics in MOS devices and as a mask against dopant implantation.

The ability of silicon to form a high quality silicon dioxide is still a crucial factor in the development of ICs.

The oxidation process can be subdivided into several single steps. At first the oxidants diffuse into the existing oxide. Then the oxidants diffuse through the oxide to the silicon/oxide interface. The reaction at the silicon/oxide interface is a further step. In the final step the newly formed oxide and motion layer is expanded.

The oxidation process can be simulated with different models which can be implemented and tested in the Finite Element Diffusion and Oxidation Simulator (FEDOS). FEDOS is able to solve three-dimensional partial differential equations and is used as a process simulator for diffusion and oxidation.

Due to the increase in volume during the conversion from silicon into silicon dioxide, thermal oxidation is one of the main sources of mechanical stress and strain in semiconductor device processing. These effects must be taken into account as an important part of the oxidation model. Current work is devoted to the development of a stress-strain-model combined with the finite element method.

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Three-Dimensional Device Simulation with MINIMOS-NT

Robert Klima

Within the last two years MINIMOS-NT has been extended to a fully three-dimensional device simulator. The PIF-based (Profile Interchange Format) libraries which support two-dimensional structures have been replaced by a more flexible library which supports one-, two-, and three-dimensional structures. A separate module called quantity server provides scalar quantities and vector-valued quantities which may be one-, two-, or three-dimensional according to the dimensionality of the device. For vector quantities, all necessary vector operations are defined. In the implementation of physical models these vector operations are used to ensure that the code works for different dimensionalities.

Any reader or writer can be applied to the quantity server. MINIMOS-NT uses a new file format especially for three-dimensional structures as a native file format and is still able to read PIF input files. Due to the lack of a standardized, general device description format we have decided to use the so-called WAFER STATE SERVER library which supports a reader and a writer module for several available device description formats.

MINIMOS-NT is now able to read any kind of grid such as tensor product grids, triangular grids, tetrahedral grids, or hybrid grids. Grids are handled via a standard interface independently from the their type and the dimensionality. The

libraries for geometry support and grid generation are completely separated from the simulator. Using this approach, the implementation of the simulator and its physical models are independent from the libraries which store the simulation input and output data.

In three-dimensional simulations the equation systems to be solved are very large. The computational costs increase dramatically, which makes optimum performance one of the main issues. Therefore, performance analyses over all modules have been performed to determine the critical issues. Various algorithms have been optimized. To guarantee reasonable simulation times, appropriate data structures have been developed to reduce access time to the data used most frequently.

Three-dimensional simulations are mandatory for the investigation of realistic three-dimensional structures because they cannot be described by two-dimensional cuts. Furthermore, three-dimensional simulations have to be performed when feature sizes become so small that the three-dimensional shape of geometries cannot be neglected and results of two-dimensional simulations are no longer reliable. Typical examples for this are thermal distributions, devices like FinFET, Super-Junction power devices, Trench-Gate structures, or MagFETs, all of which have been successfully simulated using MINIMOS-NT.

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Physical Modeling of Advanced Semiconductor Devices

Hans Kosina

A project on improved energy transport simulation has been completed. When simulating partially depleted SOI MOSFETs the standard energy transport model yields erroneous results. The predicted output characteristics show an anomalous decrease in drain current, which is clearly in contradiction to measured data. This simulation effect is caused by an overestimation of the diffusion of channel hot carriers into the floating body. An improved energy transport model has been developed, which describes hot carrier diffusion more realistically by taking into account the anisotropy of the distribution function and its deviation from the Maxwellian shape. The model has been evaluated using MINIMOS-NT. The free parameters in the models for the anisotropy of the carrier temperature and for the kurtosis of the distribution function have been determined from Monte-Carlo simulations. The predicted carrier distribution in the MOSFET now follows the Monte-Carlo results very closely, indicating that the spuriously enhanced carrier diffusion into the substrate has been suppressed.

A project on particle simulation of far-from equilibrium transport in nano-structures has been continued. A Monte-Carlo algorithm for the solution of the Wigner equation, augmented by the Boltzmann collision operator, has been developed and implemented in our Monte-Carlo device simulator. As opposed to semiclassical transport, where all particles have a positive weight, in quantum transport the weight is subjected to sign

changes. This so-called "negative sign problem" gives rise to a rapidly growing variance in the Monte-Carlo estimators. Therefore, various variance reduction techniques have been implemented and tested. A GaAs/AlGaAs resonant tunneling diode serves as a benchmark device for which experimental data is available within this joint project.

A new project on physical modeling of strained Si/SiGe device properties has been started. Our Monte-Carlo device simulator has been extended to account for the strain dependence of the electronic band structure and the scattering rates. Besides the range of Silicon-like alloys, special focus has been put on the correct treatment of Germanium rich alloys. The Monte-Carlo model can thus be used for transport calculations in strained SiGe layers on unstrained SiGe substrates over the whole composition range. A previously developed model for ionized impurity scattering has been modified to accommodate strain induced changes in the Fermi level and the screening parameters.

Hans Kosina was born in Haidershofen, Austria, in 1961. He received the 'Diplomingenieur' degree in electrical engineering and the Ph.D. degree from the 'Technische Universität Wien' in 1987 and 1992, respectively. For one year he was with the 'Institut für flexible Automation', and in 1988 he joined the 'Institut für Mikroelektronik' at the 'Technische Universität Wien'. In summer 1993 he held a visiting research position at the Advanced Products Research and Development Laboratory at Motorola, Austin, in summer 1999 a research position at the TCAD department at Intel, Santa Clara. In March 1998 he received the 'venia docendi' in the field of 'Microelectronics'. His current interests include device simulation, modeling of carrier transport and quantum effects in semiconductor devices, new Monte-Carlo algorithms, and computer aided engineering in VLSI technology.

A Stochastic Approach to the Simulation of Nanoscale Devices

Mihail Nedjalkov

The description of quantum phenomena in terms of particle trajectories is a promising approach to the modeling of transport in nanoscale electronic devices. A quantum equation which accounts for the coherent part of the transport via the Wigner potential $V_{\rm w}$ and for dissipation processes via the Boltzmann collision operator is considered. The equation is derived from our quantum model for the nanometer and femtosecond transport regime. Deterministic methods can solve the coherent Wigner equation or include dissipation in a relaxation time approximation. The particle approach is motivated by the Monte-Carlo method for classical device simulation, where the collision operator is treated in an exact manner, while the coherent part is treated within the classical limit. This limit leads to a classical force term transforming the considered equation into the Boltzmann equation. How to account for the non-local potential term is the main concern of the particle method.

A stochastic approach is proposed, where the action of the Wigner potential is interpreted in terms of scattering events. The basis is the separation of the antisymmetric function $V_{\rm w}$ into two parts: $V_{\rm w} = V_{\rm w}^+ - V_{\rm w}^-$. Here $V_{\rm w}^+ = V_{\rm w}$ if $V_{\rm w} > 0$ ($V_{\rm w}^- = -V_{\rm w}$ if $V_{\rm w} < 0$) and $V_{\rm w}^\pm = 0$ otherwise. Then a unique function $\gamma(x) = \int dk_x V_{\rm w}^\pm(x, k_x)$ can be introduced. γ has the meaning of a potential out-scattering rate in strict analogy with the phonon out-scattering rate λ.

The derived stochastic method retains the basic features of the weighted Single Particle Monte-Carlo method. The algorithms for injection from the boundary distribution, the build-up of the classical trajectory by consecutive drift and scattering events, the accumulation of the weight over the trajectory and the recording of the physical averages remain unchanged. The selection of the free-flight time follows the classical Monte-Carlo scheme with an out-scattering rate given by the sum $(\gamma+\lambda)$. The quantum character of the transport mainly affects the scheme for the after-scattering state selection. The sources considered are scattering events due to $V_{\rm w}^{+}$, a self-scattering rate γ which contributes to the weight, and $V_{\rm w}^{-}$ which causes a sign change of the accumulated weight.

The method has been used to simulate coherent low energy electron tunneling through a potential barrier. It is a tool for investigating the effect of phonon dissipation on the behavior of nanoscale devices.

Mihail Nedjalkov was born in Sofia, Bulgaria. He received the M.S. degree in semiconductor physics at the Sofia University 'St. K.Ohridski' and the Ph.D. degree at the Bulgarian Academy of Sciences (BAS). For twelve years he worked at the Departments of Physical Analysis and Theoretical Research at the 'Institute of Microelectronics', Sofia. His permanent position is with the Central Laboratory for Parallel Processing, BAS, Sofia. He was visiting researcher at the Universities of Bologna, 1992, Modena, 1994 and 1995, and Frankfurt 1997. Since 1998 he has been holding a visiting research position at the 'Institut für Mikroelektronik' at the 'Technische Universität Wien'. Besides the national research projects, he participated in INFM (Italy) and FWF (Austria) projects. Currently he is supported by the EC project NANOTCAD. His research interests include numerical theory and application of the Monte-Carlo method, physics and modeling of Boltzmann and quantum transport in semiconductor devices.

Analysis and Simulation of Advanced Heterostructure Devices

Vassil Palankovski

Communication and information systems are subject to rapid and highly sophisticated changes. In this development semiconductor heterostructure devices, such as Heterojunction Bipolar Transistors (HBTs) and High Electron Mobility Transistors (HEMTs), are among the fastest and most advanced high-frequency devices. They fulfill the requirements for low-power consumption, medium integration, low cost in large quantities, and high-speed operation capabilities in high-frequency circuits.

The use of technology, device, and circuit simulation tools reduces expensive technological efforts and aids improving the device performance. Physics-based analytical models for the lattice, thermal, band-structure, and transport properties of various semiconductor materials, as well as models for important high-field and high-doping effects are derived and implemented into our two- and three-dimensional device simulator MINIMOS-NT. Special attention is paid to the modeling of the properties of SiGe with respect to material composition and strain conditions due to lattice mismatch. The quality of these models is decisive for the predictive capabilities of the simulation tool, which must capture both process and device physics.

Two-dimensional DC and AC simulations of different types of bipolar devices, such as SiGe and InGaP/GaAs HBTs, show

very good agreement with measured data in a wide range of application temperatures. Especially for high-power devices, reliability investigations confirm the usefulness of device simulation for practical applications. A methodology for the characterization and optimization of SiGe HBTs in an integrated BiCMOS technology, with emphasis on the high frequency performance and reliability, is developed. Simulation results for devices from three different foundries show excellent agreement with measured DC and RF data.

Recent driver applications for the HEMT device concept include high-power amplifiers using the AlGaN/GaN material system. New device concepts emerge, such as double heterostructure GaAsSb/InP HBTs and GaN-based HBTs. The proper physical modeling of new materials and material systems will allow the creation of complete simulation models, which are useful for addressing unsolved device and optimization issues.

The continuous industrial demand for improved devices, which can be supported by the analysis of advanced heterostructure devices through numerical simulations, is a source of high motivation.

Vassil Palankovski was born in Sofia, Bulgaria, in 1969. He received the diploma degree in electronics from the Technical University of Sofia in 1993. Afterwards he worked in the telecommunications field for three years. In 1997 he joined the 'Institut für Mikroelektronik' at the 'Technische Universität Wien', where he received the doctoral degree in technical sciences and is currently employed as a post-doctoral researcher. In summer 2000 he held a visiting research position at LSI Logic Corporation, Milpitas, California. His scientific interests include device and circuit simulation, heterostructure device modeling, and physical aspects in general.

Simulation of Smart Power Devices with Novel Device Concepts

Jong Mun Park

Lateral double diffused MOS transistors (LDMOSFETs) are widely used as smart power devices in automotive and consumer applications. The main performance parameters for these devices are the on-resistance (R_{on}), the breakdown voltage (V_{b}), and the switching characteristics. R_{on} and V_{b} are inversely related to each other. Reducing R_{on} while maintaining the V_{b} rating has been the main issue of the smart power device design.

Recently, new concepts such as super-junction and lateral trench gate have been proposed to improve the on-state characteristics of MOSFETs. Most of the super-junction devices assume complete charge balance. It can be achieved by introducing alternating n and p columns in the drift region, and the doping in this region can be increased drastically. It is inversely related to the width of the n and p columns. Even the current conduction area is reduced by additional p columns which do not contribute to on-state conduction. This results in a significant reduction of the on-resistance.

A lateral trench gate super-junction (SJ) SOI-LDMOSFET has been studied to minimize the on-resistance. Contrary to the conventional vertical trench MOSFET, the gate is formed laterally on the side wall of a trench and the channel current flows laterally through the trench side walls. This allows the channel area to be increased, while it decreases the on-state re-

sistance of the device. To increase the on-state conduction area in the drift region, an unbalanced structure is examined where the width of the n column is larger than that of the p column. Three-dimensional numerical simulations with MINIMOS-NT have been performed to investigate the influence of device parameters on the on-state characteristics, breakdown voltage, and the sensitivity of the charge imbalance. By making the width of the n column larger than that of the p column in the drift region, it is possible to lower the doping of the n column without degrading the on-resistance. As a result, the sensitivity of the V_b to the charge imbalance is reduced compared to that of the standard SJ SOI-LDMOSFET. A lower specific on-resistance is obtained in the suggested structure.

Jong Mun Park was born in Seoul, Korea, in 1961. He studied electronics engineering at the 'Hanyang University', where he received the degree of 'Master of Science' in 1985. Afterwards he was a senior researcher at the Power Semiconductor Group at KERI, National Laboratory in Korea, where he carried out several projects for developing power semiconductor devices. He joined the 'Institut für Mikroelektronik' in March 2001, where he is currently working on his doctoral degree. His scientific interests include optimization and modeling of power semiconductor devices, Silicon Carbide (SiC) power devices, smart power ICs and Intelligent Power Modules (IPMs).

Magnetic Effects in Silicon

Rodrigo Rodríguez-Torres

Solid-state sensors play an important role in industrial applications. They are cheap to produce and the control circuitry is integrated on the same substrate the sensor is built on. From the process point of view, the sensor must not modify the standard process and it must take advantage of the process steps to be built. Because sensors are designed to sense physical variables such as temperature, pressure, light, or magnetic field, they are designed so as to maximize the effect of sensing the physical variable, making simulation in full device simulators a complicated task.

Device simulators are usually focused on solving a set of standard equations such as the Poisson and continuity equations. The more accurate the simulator should be, the more complex are the equations. Except for the temperature in self-heating simulators, none of the physical variables to be sensed are present in the above equation systems. Modifications have to be made in order to consider the new physical variables, and the resulting equations have to be solved. Taking into account the presence of a magnetic field in the device equations is simple from an algebraic viewpoint. When solving this equation numerically, a vector product must be computed.

Discretization of the equations in the presence of a magnetic field has been successfully implemented in MINIMOS-NT. The analysis of a two-drain MAGFET has been carried out in three-dimensional simulations.

A MAGFET is a MOS-based magnetic sensor. The Lorentz force can deflect the carriers of an inversion layer, and then the device is able to detect a magnetic field. In the case of a two-drain MAGFET, a differential current is included which is proportional to the magnetic field strength.

This differential current can be improved if the MAGFET is operated at cryogenic temperatures. At liquid Nitrogen temperature the MAGFET gives a differential current up to four times higher at the same magnetic field strength, according to experimental data. The MAGFET is able to detect smaller magnetic fields only if the device is cooled down.

Those facts have been studied with three-dimensional simulations using MINIMOS-NT. However, we must be aware of the used models. Some mobility models do not take into account low temperature effects properly. Improvement in these directions must be made in order to reproduce data at such low temperatures using MINIMOS-NT.

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Accurate Three-Dimensional Interconnect Simulation

Rainer Sabelka

As integrated circuit technology is scaled down into the deep submicron regime, the problems associated with interconnect lines are ever more pressing and could potentially become the roadblock to progress. While downscaling generally results in faster semiconductor devices, the performance of the metal interconnect lines is limited by various parasitic effects such as attenuation caused by resistive voltage drops, self-heating due to losses, delay times, crosstalk, reflections incurred by discontinuities, skin-effect, and eddy currents. The progression to copper metalization and low-κ dielectrics improves reliability and reduces parasitic effects to a certain degree, but cannot eliminate them. Hence, interconnect parasitics must be taken into account during the design process at an early stage and highly accurate models are required.

Therefore the Smart Analysis Programs (SAP) have been developed and applied to interconnect simulation successfully for several years. This simulation package contains tools for highly accurate parasitics (RLC) extraction, quasi-electrostatic and quasi-magnetostatic simulations using time- and frequency-domain methods, and investigations of the thermal behavior of interconnect stacks. Special attention has been directed at an efficient implementation concerning both run time and memory consumption. Compared with other (commercial) tools the simulator has the ability to perform calculations with anisotropic dielectric materials and coupled

electro-thermal simulations with temperature-dependent material properties. The finite element method (FEM) is used for the numeric solution of the partial differential equations.

For highly accurate simulations it is essential to model the simulation domain geometrically as exactly as possible. Two- and three-dimensional solid modelers are used to either construct the simulation geometry directly with an input deck, generate it automatically from a layout, or to use the output of a lithography and/or topography simulation. The simulation grid is generated either by a layer-based technique or with a fully unstructured Delaunay mesher.

A three-dimensional visualization program has been developed to display the calculated distributed scalar and vector fields, such as potential, temperature, current density by means of contour faces, stream lines, cuts, and surface representation.

Recent improvements in the Smart Analysis Programs include the implementation of anisotropically conductive materials, various enhancements to the visualization tool, an interface to the DF-ISE data format, the implementation of a module for solving electrical problems in the frequency domain and a couple of bug fixes.

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Numerical Methods for Etching and Deposition Topography Evolution

Alireza Sheikholeslami

Within topographic evolutions of etching and deposition for silicon trenches, which are important manufacturing steps for semiconductor devices, a number of typical problems require attention. These problems include the formation of sharp corners, the effect of angle-dependent flux functions on propagation rates, topological change due to splitting and merging, and complexities in three spatial dimensions. By the simulation of etching and deposition for semiconductor manufacturing a variety of numerical algorithms are available to advance fronts. Roughly speaking, they fall into three general categories: marker/string methods, cell–based methods, and characteristic methods.

The first method uses a discrete parameterized version of the boundary which is described by marked particles or a nodal triangularization in two or three dimensions. This method can be quite accurate, but topological changes are difficult to handle, and significant instabilities in the front may result. The second method divides the computational domain into a set of cells which contain volume fractions between 0 and 1 and represent the fraction of each cell containing the physical material. This method easily handles topological changes and can be used in three dimensions, but the determination of geometric quantities such as surface normals and curvature can be inaccurate. Within the third method, a 'ray trace' like method is used. This method handles looping problems more naturally,

but may be complex in three dimensions and requires adaptive adding or removing of rays, which may result in instabilities.

Level Set Methods, introduced by Osher and Sethian, offer a highly robust and accurate method for tracking interfaces performing complex motions. Their most beneficial quality is that they naturally construct the fundamental weak solution to surface propagation. They work in any number of space dimensions, handle topological merging and breaking naturally. The central mathematical idea is to view the moving front as a particular level set of a higher dimensional function. In this setting, sharp gradients are easily tracked and the effects of curvature can be accurately incorporated. The key numerical idea is to borrow the technology from the numerical solution of hyperbolic conservation laws and transfer these ideas to the Hamilton–Jacobi setting, which then guarantees that the correct entropy solution will be obtained.

In cooperation with several industrial partners, the application of the Level Set Method for tracking interfaces in semiconductor manufacturing has been studied. The goal is to follow the changing surface topography of a wafer as it is etched, layered, and shaped during the manufacturing process.

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Monte-Carlo Bulk Simulation of Strained Silicon and Silicon-Germanium

Sergey Smirnov

The mobility of free carriers in strained Si/SiGe devices strongly depends on the band structure parameters. The different band structures of strained and unstrained SiGe layers lead to a change in the kinetic properties. For example, it is possible to increase the perpendicular component of the electron mobility in SiGe HBTs or the in-plane component in an n-MOS channel when using a SiGe substrate. On the other hand, there are possibilities to reduce the mobility in those regions where it is necessary.

To investigate the kinetic properties of strained SiGe it is necessary to have a proper description of the band structure and the kinetic mechanisms which take place in the material. The Boltzmann transport equation serves as a basis for the investigation of such phenomena. A widely used numerical method for the solution of this equation is the Monte-Carlo method. This method requires a good description of the relevant scattering rates including the strain dependence. There are two representations of the bands: the analytic band structure and the full-band one. The former is suitable for a low-field regime while the latter is required for high-field transport.

Several attempts have been made to include the strain effects in Monte-Carlo simulations both for the analytical band structure and the full-band description. However, difficulties have to be overcome when implementing these effects within the full

physical picture of the kinetic phenomena. One such problem is ionized impurity scattering which combines various physical effects and gets more complex when strain is present. As a consequence, many authors have been using simpler and more efficient models from a computational point of view: the Ridley model, or the plain Brooks-Herring model, which neglect some essential features of the kinetics in semiconductors.

We have added strain effects to the electron transport both for the undoped and doped materials in our Monte-Carlo simulator, which employs an analytical band structure. The effective masses are functions of Ge mole fraction both in the substrate and in the active layer. The splittings of the valleys are calculated by linear deformation potential theory for the uniaxial strain along [001]. The shifts of the conduction band at Δ are taken into account. Alloy scattering acts as an additional mechanism. Finally all scattering mechanisms involving X-valleys have been modified properly. For doped cases, we have considered the majority and minority electron transport. The Pauli exclusion principle, momentum-dependent screening, the multi-ion scattering, the second Born approximation and the plasmon scattering may be specified independently by the user.

Sergey Smirnov was born in Skhodnya, Moscow region, Russia, in 1976. He studied Electrical Engineering at the Moscow State Institute of Electronic Technology (MIET) where he received the degree of Master of Science in 1999. Afterwards he has been a research fellow at MIET where he studied the numerical simulation of semiconductor devices. He joined the 'Institut für Mikroelektronik' in January 2002, where he is currently working on his doctoral degree. His scientific interests include physical modeling of strained Silicon/Silicon-Germanium devices, and solid-state physics in general.

The MINIMOS-NT Small-Signal Analysis Mode

Stephan Wagner

Originally two simulation modes have been provided by MINIMOS-NT: the basic steady-state DC mode and the transient simulation mode that takes all time derivatives into account. Using the transient mode small-signal analysis is very inconvenient and costly, which was the basic motivation to consider development of a small-signal or AC analysis mode.

Basically, three main steps of that development can be outlined: firstly, the linear solver module has been upgraded to solve complex-valued linear systems since differentiating a function in the time domain corresponds to multiplying its Fourier transform by $j\omega$, according to the time differentiation property of the Fourier transform. Secondly, all relevant models and interaction structures had to be modified to take the complex-valued coefficients into account. Thirdly, a set of features based on the small-signal simulation mode has been implemented.

Two core modules of MINIMOS-NT are responsible for assembling and solving the linear systems created during each Newton iteration. The assembling system has to meet several requirements of the simulation process and has to apply some measures to improve the condition of the system matrix. The completely assembled linear system is then passed on to the solver system which is responsible for the calculation of the solution vector using either a direct Gaussian solver or — more

efficiently — an iterative linear solver algorithm. The existing modules were restricted to real-valued systems, so two new modules providing all these features also for complex-valued systems have been coupled to the simulator. In addition, the new modules provide a more convenient user interface and the synchronization between the preconditioner and the iterative solver is deterministic.

The basic functionality of the AC simulation has been implemented by modifying all time-dependent models to add their complex-valued contributions to the linear system. The integration took advantage of the correspondence between transient and small-signal analysis, which yields extensive implementation synergies. In addition, several keywords had to be added to the internal structures and the standard output interfaces had to be adapted for complex-valued quantities.

One of these new features provides direct S-parameter extraction. After the calculation of a DC bias point, the subsequently started AC mode delivers the Y-matrix of the device. That matrix can be directly transformed to the intrinsic (deembedded) S-matrix. Alternatively, a standard equivalent circuit of parasitics can be specified to extract the extrinsic Y- and S-parameters that are frequently required for measurement data comparisons.

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