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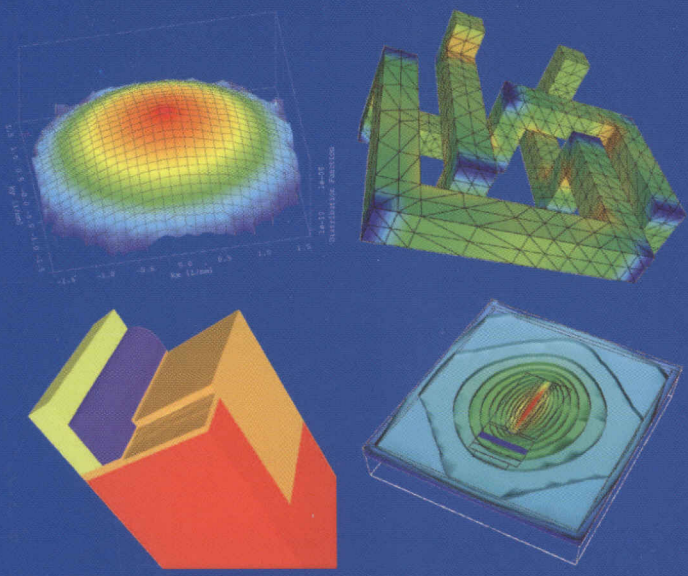

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INSTITUT FÜR MIKROELEKTRONIK
Technische Universität Wien
Gußhausstraße 27 – 29
A – 1040 Wien
AUSTRIA

http://www.iue.tuwien.ac.at/
Tel: +43/1/58801/36001
Fax: +43/1/58801/36099

Staff

Tesfaye Ayalew	Dipl.-Ing.	(August 1, 2002–)
Hajdin Ceric	Dipl.-Ing.	
Johann Cervenka	Dipl.-Ing.	
Klaus Dragosits	Dipl.-Ing., Dr.techn.	
Peter Fleischmann	Dipl.-Ing., Dr.techn.	(–January 31, 2003)
Andreas Gehring	Dipl.-Ing.	
Tibor Grasser	Ao.Univ.Prof., Dipl.-Ing., Dr.techn.	
Markus Gritsch	Dipl.-Ing., Dr.techn.	(–January 31, 2003)
Christian Harlander	Dipl.-Ing., Dr.techn.	(–January 31, 2003)
Ewald Haslinger		
Clemens Heitzinger	Dipl.-Ing., Dr.techn.	
Andreas Hössinger	Dipl.-Ing., Dr.techn.	
Christian Hollauer	Dipl.-Ing.	
Stefan Holzer	Dipl.-Ing.	(February 1, 2003–)
Manfred Katterbauer		
Robert Klima	Dipl.-Ing., Dr.techn.	
Robert Kosik	Dipl.-Ing.	(May 1, 2003–)
Hans Kosina	Ao.Univ.Prof., Dipl.-Ing., Dr.techn.	
Erasmus Langer	Ao.Univ.Prof., Dipl.-Ing., Dr.techn., Head	
Mihail Nedjalkov	Dr.phys.	(–June 30, 2003)
Vassil Palankovski	Dipl.-Ing., Dr.techn.	
Jong Mun Park	MSc	
Rodrigo Rodriguez-Torres	M.C., Dr.techn.	(–March 31, 2003)
Rainer Sabelka	Dipl.-Ing., Dr.techn.	
Siegfried Selberherr	O.Univ.Prof., Dipl.-Ing., Dr.techn., Dean	
Alireza Sheikholeslami	Dipl.-Ing.	
Sergey Smirnov	MSc	
Enzo Ungersböck	Dipl.-Ing.	(July 1, 2002–)
Stephan Wagner	Dipl.-Ing.	
Wilfried Wessner	Dipl.-Ing.	(August 1, 2002–)
Robert Wittmann	Dipl.-Ing.	(July 1, 2002–)
Renate Winkler		

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Preface

Erasmus Langer and Siegfried Selberherr

This brochure is the fifteenth annual research review of the Institute for Microelectronics. The staff financed by the Austrian Federal Ministry of Education, Science, and Culture consists of ten full-time employees: the dean of the Faculty of Electrical Engineering and Information Technology, the head of the institute, two additional professors, three scientists, a secretary, and two technical assistants. Nineteen additional scientists are funded through scientific projects supported by our industrial partners, by the Austrian Science Fund (FWF), and by the EC Framework Programme.

Regarding the status of the EC projects, the two projects MAGIC-FEAT and NANOTCAD have been completed successfully, the project MULSIC is continuing, and two new projects within the "Information Society Technologies (IST)" program, named UPPER+ and NESTOR, have been started. The institute is involved in several applications for projects within the 6th Framework Programme, and we have hopes for a positive evaluation. We are very happy to be able to report that our industrial partners have continued the cooperation. Furthermore, the Christian Doppler Gesellschaft has established a "Christian Doppler Laboratory for Technology CAD in Microelectronics" at our institute.

Despite the unknown future organizational structure due to a change in Austria's law, our institute is entering the next year with high expectations.

Erasmus Langer was born in Vienna, Austria, in 1951. After having received the degree of 'Diplomingenieur' from the 'Technische Universität Wien' in 1980 he was employed at the 'Institut für Allgemeine Elektrotechnik und Elektronik'. In 1986 he received his doctoral degree and in 1988 he joined the 'Institut für Mikroelektronik'. In 1997 he received the 'venia docendi' in microelectronics. Since 1999 Dr. Langer is head of the 'Institut für Mikroelektronik'. His current research topic is the simulation of micro-structures using high performance computing paradigms.

Siegfried Selberherr was born in Klosterneuburg, Austria, in 1955. He received the degree of 'Diplomingenieur' in electrical engineering and the doctoral degree in technical sciences from the 'Technische Universität Wien' in 1978 and 1981, respectively. Dr. Selberherr has been holding the 'venia docendi' in computer-aided design since 1984. From 1988 to 1999 he was the head of the 'Institut für Mikroelektronik' and since 1999 he has been dean of the 'Fakultät für Elektrotechnik und Informationstechnik'. His current topics are modeling and simulation of problems for microelectronics engineering.

Renate Winkler was born in Vienna, Austria, in 1960. She joined the 'Institut für Mikroelektronik' in November 1993. Since that time she has been responsible for organizational and administrative work of the institute.

Ewald Haslinger was born in Vienna, Austria, in 1959. He joined the 'Institut für Mikroelektronik' in December 1991. Since that time he has been responsible for organizational, administrative and technical work of the institute.

Manfred Katterbauer was born in Schwarzach St.Veit, Austria, in 1965. He joined the 'Institut für Mikroelektronik' in February 1995. Since that time he has been in charge of all technical hardware and software work of the institute.

Numerical Analysis of SiC-based Semiconductor Devices

Tesfaye Ayalew

Silicon has long been the dominant semiconductor for electronic device applications. However, wide bandgap semiconductors, particularly silicon-carbide (SiC), have attracted much attention because they offer tremendous benefits over other semiconductor materials in a large number of industrial and military applications. The physical and electronic properties of SiC make it the foremost semiconductor material for short wavelength optoelectronic, high temperature, radiation resistant, and high-power/high-frequency electronic devices.

SiC-based electronic devices can operate at extremely high temperatures without suffering from intrinsic conduction effects because of the wide energy bandgap of 2.3 – 3.5 eV. Devices formed in SiC can withstand an electric field five to twenty times greater than silicon or gallium arsenide without undergoing avalanche breakdown. SiC is an excellent thermal conductor with a three to thirteen times higher thermal conductivity than silicon. SiC devices can operate at high frequencies (RF and microwave) because of the larger saturated electron drift velocity, which is two to three times higher than in silicon.

Continuous improvement of SiC material quality has led to published experimental work from several groups covering a broad field of applications. To date, theoretical work has been largely limited to simple calculations of basic material param-

eters, due to the absence of a comprehensive set of TCAD (Technology CAD) models for SiC. This has resulted in uncertainty as to whether real device applications would benefit from the superior material properties of SiC. Therefore, the use of appropriate physical models is fundamental for any comparative study that involves numerical analysis.

We have implemented realistic material-specific physical models in our general-purpose device simulator MINIMOS-NT to account for the following effects: mobility degradation due to surface scattering; high field mobility that incorporates the effect of the saturation velocity caused by increasing optical phonon gas against which the carriers are accelerated; the influence of temperature and electric field on the impact ionization rate; and, finally, the temperature and doping dependence of incomplete ionization of dopants in SiC. We utilized published material data to drive physical models by adjusting model parameters to obtain close agreement with experimental data.

Tesfaye Ayalew was born in Addis Ababa, Ethiopia in 1966. He earned his BSc. degree in electrical engineering from Addis Ababa University in 1989. Afterwards he served for five years at the National Scientific Equipment Center in Ethiopia. In 1995 he was a visiting researcher at the Institute for Biomedical Engineering at the University of Vienna. In the same year he enrolled at the 'Technische Universität Wien' where he studied electrical engineering and received the degree of 'Diplomingenieur' in March 2000. He joined the 'Institut für Mikroelektronik' in May 2000, where he is currently working on his doctoral degree. His research interest is focused on modeling and simulation of wide bandgap semiconductor devices.

Simulation of Dopant Diffusion Based on Non-Equilibrium Point Defect Models

Hajdin Ceric

The kinetics of point defects are crucial for the understanding and modeling of dopant diffusion in silicon. During thermal oxidation, injection of point defects from the growing oxide causes oxidation-enhanced diffusion (OED) which forms the dopant concentration profile. The diffusion of substitutional dopants occurs via a dual mechanism. Substitutional dopants are assumed to move via both vacancy-assisted and interstitial-assisted diffusion. During the dopant diffusion process the point defects are generally not in equilibrium, a fact which is proven by experimental results. In the presence of oxidizing surfaces the vacancy and interstitial concentrations depart even more from their equilibrium values, exhibiting complex kinetics. Although the non-equilibrium kinetics of point defects has been theoretically well-studied, its implementation in simulation tools has been restricted to one- and two-dimensional models. However, the technology of modern devices requires simulative prediction of the explicitly three-dimensional point defect profiles.

The advanced models of dopant diffusion are described by a system of non-linear partial differential equations (PDE). Finite element discretization of such equations produces large systems of non-linear algebraic equations which can be solved by means of the Newton-Raphson method. However, the complete discretization of non-equilibrium PDEs is very costly and demands long assembling times. Additionally, the structure of

the algebraic system leads to very poor convergence of the Newton-Raphson scheme. That is why physically-based simplifications of the original PDE system are needed.

Consequently, in the case of OED we have to deal with two models which describe non-equilibrium diffusion in bulk silicon. Both of these models are combined with the point defect surface model, which describes oxidizing conditions. The first model handles low dopant concentration and slow point defect dynamics; the second one is applicable in the cases of more pronounced non-equilibrium dynamics of point defects.

Both models have been implemented in FEDOS (Finite Element Diffusion and Oxidation Simulator) for three-dimensional geometries. Reasonable linearization of non-linear terms and computationally efficient approximation of the derivatives significantly reduces assembling times. The physical soundness of the resulting model implementations is evaluated through comparison of the simulation with appropriate analytical models and simulation results obtained by two-dimensional simulation tools. All realized simulations exhibit good agreement with the reference examples.

Hajdin Ceric was born in Sarajevo, Bosnia and Hercegovina, in 1970. He studied electrical engineering at the Electrotechnical Faculty of the University of Sarajevo and at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 2000. He joined the 'Institut für Mikroelektronik' in June 2000, where he is currently working on his doctoral degree. His scientific interests include interconnect and process simulation.

Three-Dimensional Mesh Generation for Electronic Device Simulation

Johann Cervenka

The simulation of processes and physical effects is vital for the development of today's electronic devices. With shrinking device dimensions, effects arise which cannot be described by two-dimensional models alone. Particularly at corners, parasitic effects can dominate the device behavior and change the device characteristics significantly. To analyze these effects the process and device simulators have to be extended to three dimensions. However, the simulation results should be delivered in tolerable calculation times and within memory limits. Specially adapted grid generators must be used to achieve accurate results.

For three-dimensional device simulation usually tetrahedral grids are used. A big advantage of these meshes is that they are not limited by the geometry of the simulation structures. However, although the grid density can be varied independently when using ortho-product grids, this is not possible using tetrahedral grids. Furthermore, with complex and non-planar device structures, the amount of grid points increases dramatically. Therefore a new method was developed which combines the benefits of both approaches.

The simulation domain is treated as a resistor, with two electrodes at the top and at the bottom, where a voltage is applied. After the discrete Laplace equation inside the resistor area is calculated, the grid points are placed at the intersections of

selected equipotential lines and field lines. Then the point set gets tetrahedrized.

For device simulation it is necessary to approximate the doping profiles in the device areas. A tool for the implantation and diffusion in simple three-dimensional device structures has been developed. Starting from a one-dimensional doping profile, the diffusion parameters are calculated assuming only a simple and linear diffusion model. Based on these parameters the three-dimensional diffusion process is started. Then the geometry information and doping profiles are delivered to the device simulator.

State-of-the-art layout, process, and device simulation tools have been applied to the three-dimensional simulation of a complex high voltage MOS transistor. Because of the complexity of such device structures, the geometry data were approximated by layers of different materials. With LAYGRID these layer-based data were assembled and converted to a three-dimensional structure. By applying the diffusion tool, the essential doping profiles were imported. After the conversion of the grid data to the device simulator's data format, device simulation was performed and the electrical characteristics of the device could be obtained.

Johann Cervenka was born in Schwarzach, Austria, in 1968. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1999. He joined the 'Institut für Mikroelektronik' in November 1999, where he is currently working on his doctoral degree. His scientific interests include three-dimensional mesh generation as well as algorithms and data structures in computational geometry.

Analysis of Ultra-Short Channel Devices with High-k Gate Dielectrics

Klaus Dragosits

CMOS oxide thicknesses in the nanometer range lead to the development of TCAD models which take the quantum mechanical effects at the semiconductor/insulator interface into account. Various approximation models for quantum mechanical effects exist and reasonable results are obtained for C/V characteristics, but no mobility model which considers these effects has been developed up to now.

It is obvious that the quantum distribution of carriers will not fit existing mobility models which were empirically developed employing a classical profile, where the charge is concentrated at the semiconductor/insulator interface. In particular, the terms which account for surface scattering are expected to need modifications.

For an accurate approximation of the carrier concentration profile near the interface we utilize an approximation model which was recently developed and implemented into the device simulator MINIMOS-NT. This model makes two modifications to the classical model. Firstly, the carrier concentration near the interface is reduced utilizing an exponential shape function. Secondly, the bandgap near the surface is replaced by the lowest eigenvalue.

To develop a suitable mobility model which can be applied jointly with the quantum confinement approximation, two series of conjugate CMOS from two different technology nodes,

with channel lengths ranging from 130 nm to 1 μm, were investigated. These investigations were carried out using the optimization framework SIESTA.

Running the optimization with our quantum approximation leads to remarkable results. As for the classical model, very good agreement with the measured data is obtained, whereby the mobility model is significantly modified. The classical model utilized a set of three fitting parameters to account for surface-related effects, whereas the new model requires only one parameter to account for the different properties of the interface. This not only makes calibration to new technology nodes easier but also allows a physical interpretation: this parameter can be regarded as surface mobility and thus serves as a suitable and easily extractable parameter for the characterization of semiconductor/insulator interfaces.

Klaus Dragosits was born in Bruck an der Mur, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the 'Diplomingenieur' and the Ph.D. degrees in 1996 and 2001, respectively. He joined the 'Institut für Mikroelektronik' in September 1997. He held visiting research positions at Philips Research, Eindhoven, in March 2000, at the Samsung Advanced Institute of Technology, Seoul, in June 2000, and at the European Center of Excellence at the Bulgarian Academy of Science, Sofia, in August 2001. His scientific interests include device simulation with special emphasis on nonvolatile memory cells, ferroelectrics, high-k dielectrics, quantum effects and polymere-based devices.

Optimization of Dielectric Stacks with MINIMOS-NT

Andreas Gehring

To allow further device scaling below a 100 nm channel length it is necessary to reduce the MOSFET effective oxide thicknesses to below 2 nm. This is not possible using SiO_2 due to an exponential increase in gate leakage current: a gate current density of $1\,A/cm^2$ is usually regarded as an upper limit for proper functioning CMOS circuits, while low-power devices may require even stricter limitations. Gate dielectric stacks consisting of high-k dielectric layers such as Si_3N_4, Al_2O_3, Ta_2O_5, HfO_2, or ZrO_2 have been suggested as alternative dielectrics.

Unfortunately, these materials show a pronounced trade-off between permittivity and barrier height, so it is not possible to simply choose a material with high permittivity and a high energy barrier. Furthermore, at the interface to the underlying silicon substrate, an interface layer exists which is either created unintentionally during processing or is intentionally deposited to improve the interface quality. Due to this layer, the energy barrier is not linear but shows a kink. Thus, simulation of gate leakage requires the calculation of tunneling current through non-triangular energy barriers. To get a clear picture of the transmission through the stack, a rigorous solution of Schrödinger's equation in the dielectric region is necessary.

A solution of Schrödinger's equation with open boundary conditions can be found using the transfer-matrix method. It is

based on the approximation of an arbitrarily shaped energy barrier by a series of constant or linear segments. Each segment is described by a transfer matrix, and the transfer matrix of the whole barrier is found by subsequent matrix computations. During the matrix multiplications, however, exponentially growing and decaying states have to be multiplied, leading to rounding errors which eventually exceed the amplitude of the wave function itself.

An alternative method for solving Schrödinger's equation with open boundary conditions is based on the quantum transmitting boundary method. Here, the closed-boundary Hamiltonian is coupled to reservoirs at the contacts. This yields a complex-valued linear system, which can be solved for the values of the wave function. The transmitting-boundary method has been implemented into MINIMOS-NT, together with an interface for the definition of stacked segments. To assure self-consistency, the electron concentration in the stack is calculated from the wave function in the dielectric, and the tunneling current is considered in the continuity equation of neighboring segments. Further work will concentrate on the coupling of the Schrödinger solver with MINIMOS-NT for the calculation of channel quantization and related effects.

Andreas Gehring was born in Mistelbach, Austria, in 1975. He studied communications engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in March 2000. He joined the 'Institut für Mikroelektronik' in April 2000, where he is currently working on his doctoral degree. In summer 2001 he held a visiting research position at the Samsung Advanced Institute of Technology in Seoul, South Korea. His scientific interests include the modeling of tunneling effects in thin dielectrics, quantum device simulation, and computational electronics.

Modeling of Mobilities and Relaxation Times in Macroscopic Transport Models

Tibor Grasser

Since the proposal of hydrodynamic models over forty years ago, the modeling of transport parameters such as mobilities and relaxation times has been a hot topic of research. These parameters are of fundamental importance because they determine the carrier current and the higher order fluxes. One of the most accurate physics-based models for the carrier mobility so far has been proposed by Hänsch. In this model the energy relaxation time is assumed to be constant. Although the energy relaxation time can be more accurately modeled as a function of the average carrier energy by fitting Monte Carlo data, this is not possible for the mobilities which are not single-valued functions of the average carrier energy. Similar difficulties are observed for the energy flux mobility, which is frequently modeled as being equal to the carrier mobility.

In addition to these difficulties, hydrodynamic models suffer from further limitations. Most of them are related to the fact that these models do not provide enough information about the distribution function. Hence, a heated and drifted Maxwellian approximation is frequently assumed. It has been shown that this is not sufficient to model hot carrier processes like impact ionization and that much more accurate results can be obtained by including the next two equations of the moment hierarchy, which results in a six moments transport model. This approach requires accurate models for the higher order mobilities and relaxation times.

Since the mobilities and relaxation times are functionals of the distribution function, which is reproduced well by a six moments description, we can directly evaluate the scattering integral appearing in Boltzmann's transport equation. Assuming that the diffusion approximation holds and that the scattering operator is linear, the moments of the scattering integral can be given as a linear combination of the fluxes. Conventionally these moments are rearranged by introducing flux-dependent mobilities. Since these flux dependencies are difficult to handle in two- and three-dimensional implementations, it is generally assumed that the ratios of the fluxes behave like those in homogeneous samples. This transforms the flux dependence into an energy dependence but impairs the quality of the model. Instead, we reformulate the moments of the scattering integral in terms of the fluxes of the equation system. As a result, all fluxes occurring in the final equation system depend only on the even moments of the distribution function.

Tibor Grasser was born in Vienna, Austria, in 1970. He received the 'Diplomingenieur' degree in communications engineering, the Ph.D. degree in technical sciences, and the 'venia docendi' in microelectronics from the 'Technische Universität Wien', in 1995, 1999, and 2002, respectively. He is currently employed as an Associate Professor at the 'Institut für Mikroelektronik'. Since 1997 he has headed the MINIMOS-NT development group, working on the successor of the highly successful MINIMOS program. He was a visiting research engineer at Hitachi Ltd., Tokyo, Japan, and at the Alpha Development Group, Compaq Computer Corporation, Shrewsbury, USA. In 2003 he was appointed head of the Christian Doppler Laboratory for TCAD in Microelectronics, an industry-funded research group embedded in the 'Institut für Mikroelektronik'. His current scientific interests include circuit and device simulation, physical modeling, and software development.

Topography Simulation, Backend Stacks, and Grid Generation

Clemens Heitzinger

The current challenge for TCAD is the prediction of the performance of groups of devices, backends, and large parts of the final IC in contrast to the simulation of single devices and their fabrication. This enables one to predictively simulate the performance of the final device depending on different process technologies and parameters.

Hence, the work on the feature scale topography simulator ELSA was continued and its abilities expanded to enable the simulation of interconnect capacitance and time delays. The simulation flow starts *ab initio* with silicon surfaces and takes into account etching, deposition, and CMP steps. From these the complex structures of interconnect lines are built, resulting in many combinations depending on metal combination, line-to-line space, and line width. The interconnect structures serve as input to the field solver whose capacitance simulations are stored in a database. The circuit designer accesses the results of this simulation flow and uses them in circuit simulations.

The simulations show very good agreement with charge-based capacitance measurements (CBMs). These simulations were used during the development of a 100 nm CMOS process and proved to be of great help for circuit design. The work on topography simulation was performed in cooperation with Cypress Semiconductor (San Jose, CA, USA), Infineon Technologies (Villach, Austria), and Toshiba (Kawasaki, Japan).

Furthermore, the level set algorithm developed for the topography simulator ELSA was used as part of a new grid generation algorithm. Generating structurally aligned grids is important for accurate device simulations, since the quality of the numeric approximation particularly depends on the underlying mesh. In addition to generating structurally aligned triangulations, including anisotropy if desired, it is possible to enforce quality criteria on the final mesh, such as the minimum angle criterion or the Delaunay criterion.

Although a technique based on the level set method was proposed by others for generating structurally aligned grids, that method cannot generate anisotropic grids and no condition concerning the quality of the grid can be enforced. Grids were generated for the simulation of a 120 V trench gate MOSFET by the device simulator MINIMOS-NT, which showed the advantages of this algorithm.

Clemens Heitzinger was born in Linz, Austria, in 1974. He studied Technical Mathematics at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1999. He joined the 'Institut für Mikroelektronik' in February 2000. From March to May 2001 he held a position as a visiting researcher at the Sony Technology Center in Hon-Atsugi (Tokyo, Japan). He received the doctoral degree in technical sciences from the 'Technische Universität Wien' in 2002. In January 2003 he was awarded an Erwin Schrödinger Fellowship by the Austrian Science Fund (FWF) for the project entitled *Mathematical Models for Nanoscale Semiconductor Device Engineering*. In March 2003 he held a position as visiting researcher at Cypress Semiconductor in San Jose (CA, USA). His scientific interests include applied mathematics for process and device simulation.

Full Three-Dimensional Process Simulation

Andreas Hössinger

With shrinking dimensions of semiconductor devices, more and more effects arise which cannot be analyzed by two-dimensional simulations, since two-dimensional simulations fail to describe the influence of corners or other three-dimensional structures. In the very small devices which are used in standard modern technologies, almost all regions of the devices are located close to corners. These critical devices require three-dimensional process and device simulations for their behavior and the impact of processing steps to be understood.

Within the last year several tools have been developed for the three-dimensional simulation of semiconductor process steps. Among them are TOPO3D, a simulator for etching, deposition and mask transfer process steps; MCIMPL-II, an ion implantation simulator; and FEDOS, a simulator for annealing and oxidation processes. Since all these simulators have been designed around the WAFER STATE SERVER library, they are fully compatible with each other, even though different data-structures are used internally by the simulators.

Due to the integration with the WAFER STATE SERVER , advanced simulation concepts could be implemented for the topography simulator TOPO3D. While the simulation domain is discretized in a polygonal format, the surface motion is modeled by a cellular-based algorithm. At the end of the simulation the moving front and the original structure are merged. Thus,

the drawback of cellular-based simulators – that the cellular discretization modifies the complete simulation domain – can be overcome, while the stability of the cellular-based algorithm is maintained.

A rigorous object-oriented design concept has been chosen for the WAFER STATE SERVER as well as for the process simulation tools. Convenient model interfaces have been developed, which is especially relevant for FEDOS, since a large number of models had to be, and still have to be, developed and integrated to cover all the requirements on diffusion and oxidation simulation.

In addition to the fundamental process simulators, tools have been developed on the basis of the WAFER STATE SERVER which allow a convenient design of three-dimensional semiconductor devices. It is possible to define a three-dimensional structure and add analytically defined doping distributions and grid refinement regions.

Andreas Hössinger was born St. Pölten, Austria, in 1969. He studied technical physics at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in January 1996. He joined the 'Institut für Mikroelektronik' in June 1996. In 1998 he held a visiting research position at Sony in Atsugi, Japan. In September 2000 he finished his Ph.D. degree at the 'Institut für Mikroelektronik' where he is currently enrolled as a post-doctoral researcher. In 2001 he held a position as visiting researcher at LSI Logic in Santa Clara, CA, USA within the scope of a cooperate research project on three-dimensional process simulation. In 2001 he also received a grant from the Austrian Academy of Science within the scope of the Austrian Program for Advanced Research and Technology for his work on three-dimensional process simulation.

Three-Dimensional Simulation of Thermal Oxidation of Silicon

Christian Hollauer

Thermal oxidation of silicon is one of the most important steps in the fabrication of highly integrated electronic circuits. Silicon dioxide is mainly used for efficient isolation of adjacent devices from each other.

If a surface of a silicon body has contact with an oxidizing atmosphere, the chemical reaction of the oxidant (oxygen or steam) with silicon results in silicon dioxide. This reaction consumes silicon and the newly formed silicon dioxide has more than twice the volume of the original silicon. If a silicon dioxide domain already exists, the oxidants diffuse through the oxide domain and react at the interface of oxide and silicon to form new oxide so that the dioxide domain grows.

Thermal oxidation is a complex process in which three subprocesses, oxidant diffusion, chemical reaction, and volume increase, occur simultaneously. The volume increase is the main source of mechanical stress and strain, and these cause displacement.

From the mathematical point of view, the problem can be described by a coupled system of partial differential equations, one for the diffusion of the oxidant through the oxide, the second for the conversion of silicon into silicon dioxide at the interface, and the third for the mechanical problem of the Si–SiO_2–body, which can be modeled as an elastic, viscoelastic, or viscous body.

For a realistic and accurate oxidation simulation, the three subproblems should be coupled. However, most oxidation models decouple them into a sequence of quasi-stationary steps.

During the last year a new oxidation model has been designed and implemented. Our model takes into account that the diffusion of oxidants, the chemical reaction, and the volume increase occur simultaneously in a so-called reactive layer. This reactive layer has a spatial finite width, in contrast to the sharp interface between silicon and dioxide in the convential formulation. The oxidation process is numerically described by a coupled system of equations for reaction, diffusion, and displacement. In order to solve the numerical formulation of the oxidation process, the finite element scheme is applied.

Although the model delivers qualitatively correct results, there is a lack in time reality. Because of this fact, we are currently working on the adjustment of the parameters in our model so that the result of the simulation agrees with the output of a real oxidation process.

Christian Hollauer was born in St.Pölten, Austria, in 1975. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in March 2002. He joined the 'Institut für Mikroelektronik' in April 2002, where he is currently working on his doctoral degree. His scientific interests include modeling and simulation of oxidation processes and software engineering.

Optimization and Inverse Modeling in TCAD Applications

Stefan Holzer

Optimization problems in TCAD applications have become steadily more complex due to the increasing complexity of interconnects and devices in microelectronic structures. Thus, simulations, and therefore optimizations, become more time-consuming, especially if three-dimensional structures are considered. Since current workstations offer increased performance at steadily decreasing costs, they can be included as computational nodes in existing simulation and optimization clusters. This enables new approaches that use genetic algorithms for optimizations which otherwise would be too time-consuming.

These new approaches require tools that are able to manage the available network resources efficiently and to avoid inconsistencies and overloads of certain simulation nodes. Therefore, SIESTA (Simulation Environment for Semiconductor Technology Analysis) has been developed at the Institute for Microelectronics to integrate a global network resource management, optimizers, and simulators and to combine the advantages of gradient-based and genetic optimizers. The software concept of SIESTA has been redesigned to improve and extend the interfaces to graphical user interfaces (GUIs), optimizers, and simulators, which enable a loosely-coupled system with only minor restrictions for external tools. Additionally, fault tolerance was included in the interface concepts to provide a stable main program.

With this variety of tools, the simulation framework SIESTA can be used to investigate and optimize parameters for semiconductor process and device simulation. Furthermore, it allows inverse modeling of devices and technology processes, which is useful for the extraction of specific material and process parameters. The required information includes measured data and an appropriate base model which allows SIESTA to optimize the chosen parameters automatically. This technique has already produced excellent results.

Currently, thermal effects in polycrystalline semiconductors for integrated fuses are being investigated using the program STAP, with which critical temperatures in some parts of the semiconductor can be predicted. At high temperatures, however, conventional models do not predict the change of the electrical behavior correctly. Therefore it is necessary to include advanced models in device simulators which are valid in these temperature ranges. SIESTA can be used to develop simple analytical models to include them in device and circuit simulators.

Stefan Holzer was born in Vienna, Austria, in 1976. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in April 2002. He joined the 'Institut für Mikroelektronik' in January 2003, where he is currently working on his doctoral degree. His scientific interests include optimizations, software aspects of TCAD applications, and distributed computing.

Three-Dimensional Device Simulation with MINIMOS-NT

Robert Klima

The fast-growing market for semiconductor devices and the high costs for fabricating the devices give rise to ongoing miniaturization. The three-dimensional properties of the device structures become more pronounced, and the device geometries noticeably influence the electrical characteristics and the behavior of the device. On the other hand, advances in process technology and increasing demands on the electrical and thermal characteristics of the devices lead to complex structures. Therefore, three-dimensional device simulations have to be performed to predict the behavior of semiconductor devices and to be able to influence the process line in the very first steps. Examples for devices which require three-dimensional simulations are FinFETs or superjunction LDMOSFETs.

Within the past three years MINIMOS-NT has been extended to a three-dimensional device simulator, where the old PIF-based (Profile Interchange Format) libraries have been replaced by more flexible ones which support one-, two-, and three-dimensional grids and attributes. Due to the lack of a standardized commonly-used general device-description format, and to enhance the interoperability with other TCAD tools the WAFER STATE SERVER has been coupled with MINIMOS-NT. It supports a reader and a writer module for several available device description formats. MINIMOS-NT provides a powerful quantity server, which is independent from libraries used for reading and writing the input files and which

supports one-, two-, and three-dimensional attributes and operations. Any kind of grid and arbitrary geometries can be supplied.

For effective mixed-mode simulations, information about the dimensionality of a device is hidden. Therefore, an object-oriented design has been used to handle information about devices being simulated. This approach enables the use of one-, two-, and three-dimensional devices within a circuit at the same time.

In three-dimensional simulations the equation systems to be solved are very large and the computational effort increases dramatically. Thus, one of the main issues is to keep the computational overhead as small as possible. Therefore, performance analyses for all modules have been carried out to determine the crucial parts. Various algorithms have been optimized and the data management has been improved.

In each phase of the simulation flow, MINIMOS-NT is controlled with an object-oriented database designed with respect to the requirements of TCAD applications. An interactive mode which allows the adjustment of simulation parameters during runtime has been implemented particularly for three-dimensional simulation with hardly predictable simulation times.

Robert Klima was born in Vienna, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien' where he received the degree of 'Diplomingenieur' in 1997. In the same year he joined the 'Institut für Mikroelektronik'. He received the doctoral degree in technical sciences in 2003. He is currently working as a senior researcher. His scientific interests include device and circuit simulation, visualization and software technology.

NanoTCAD

Robert Kosik

Modern ultra-small devices are mesoscopic systems with a physical dimension on the scale of the electron coherence length. When designing such devices it is mandatory to take quantum mechanical effects into account.

The Wigner-formulation of quantum mechanics is a powerful tool for modeling, because it provides a mathematical description in close analogy to the classical case. The Wigner equation is the quantum analogue of the Liouville equation; the Wigner function is the analogue of a phase-space distribution. Like a classical distribution function, the Wigner function is real, but in general it also takes on negative values and hence cannot be naively interpreted as a probability distribution.

Alternatively to the description in Wigner space, it is possible to formulate the model as a mixed-state Schrödinger equation with open boundary conditions. This approach is also known as the quantum transmission boundary method (QTBM). For purely coherent transport, the Schrödinger and the Wigner formulation describe exactly the same model.

In the simulation of resonant tunneling diodes, we get sharp resonances in the transmission probabilities. In a very simple picture these resonances can be attributed to the eigenenergies in the quantum well. To resolve these resonances we need a very fine mesh in k-space. However, the standard Wigner formulation uses an equispaced mesh in k, and resolution of the resonances becomes, in practice, impossible due to very

high computational costs. Comparing simulation results for coherent transport with the QTBM, we find that the difference is essential and cannot be ignored.

For self-consistent simulation, the Schrödinger equation was coupled to the Poisson equation. To achieve convergence, the Gummel procedure was applied. However, we found that the resulting algorithm lacked robustness and often failed to converge for higher bias. To improve this, a full Newton method was implemented and parallelized on a cluster of Linux workstations. This enhanced the convergence properties of the simulator. However, robustness is still an issue which is continuously investigated.

In a second line of research, a study of the numerics of transport models using higher order moments has been started. These methods are used to describe hot-carrier effects in modern semiconductor devices. The six moments model, which was investigated, was introduced by our colleague Tibor Grasser. It uses a semi-empirical nonlinear closure.

The proposed models will be implemented and tested and their numerical performance and applicability to various conditions and structures will be investigated.

Robert Kosik was born in Eisenstadt, Austria, in 1969. He studied technical mathematics at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 1996. After his community service he joined the 'Institut für Mikroelektronik' in October 1998, where he is currently working on his doctoral degree. His scientific interests include computational physics and applied mathematics.

VMC: A Monte Carlo Simulator for Non-Equilibrium Quantum Transport

Hans Kosina

A project on particle simulation of far-from-equilibrium transport in nano-structures has been completed. A novel Monte Carlo (MC) method for the solution of the Wigner-Boltzmann equation has been integrated into the one-dimensional device simulator VMC (Vienna Monte Carlo code). This equation describes both quantum interference and dissipation effects due to carrier scattering with equal accuracy. The MC method is derived starting from the integral form of the Wigner-Boltzmann equation. The kernel of the adjoint equation is decomposed into a linear combination of conditional probability densities. The latter represent the transition density used for the construction of numerical trajectories. The properties of the transition density allow a particle picture to be introduced. In this picture dissipation and interference phenomena are taken into account by two alternative processes involving particles. Interaction with the classical force field and with various scattering sources is taken into account by drift and scattering processes corresponding to the semi-classical Boltzmann transport picture. Interference effects due to the Wigner potential are associated with a generation process of particle pairs carrying the statistical weights ± 1.

The challenge of employing such a method is to handle the avalanche of numerical particles properly. The problem has been solved for stationary conditions: particles of opposite weight and a sufficiently small distance in phase space are con-

tinuously removed in the course of a simulation. The novel MC method has been validated by comparison with NEMO-1D, where different types of resonant tunneling diodes have been used as benchmark devices.

A project on physical modeling of strained Si/SiGe device properties has been continued. The dependence of the carrier mobility on technologically relevant parameters such as substrate orientation, transport direction, Ge mole fraction, strain, and doping concentration has been studied. VMC has been extended to allow for a flexible variation of these parameters in a wide range. The physical model covers the whole Ge composition range and takes into account substrates of general orientation and the splitting of both X and L-valleys. In-plane strain, effective masses, and scattering parameters are functions of the Ge mole fraction. A physically-based ionized impurity scattering model accounts for the splitting of the effective density of states and the screening function. To calculate the mobility tensor in the zero-field limit and for degenerate conditions a specific MC algorithm has been developed.

Hans Kosina was born in Haidershofen, Austria, in 1961. He received the 'Diplomingenieur' degree in electrical engineering and the Ph.D. degree from the 'Technische Universität Wien' in 1987 and 1992, respectively. For one year he was with the 'Institut für flexible Automation', and in 1988 he joined the 'Institut für Mikroelektronik' at the 'Technische Universität Wien'. In summer 1993 he held a visiting research position at the Advanced Products Research and Development Laboratory at Motorola, Austin, and in summer 1999 a research position at the TCAD department at Intel, Santa Clara. In March 1998 he received the 'venia docendi' in the field of microelectronics. His current interests include device simulation, modeling of carrier transport and quantum effects in semiconductor devices, new Monte Carlo algorithms, and computer aided engineering in VLSI technology.

Particle Model of the Wigner-Boltzmann Transport Equation

Mihail Nedjalkov

The Wigner-Boltzmann equation provides a relevant description of the carrier transport in nanoscale devices. Coherent processes are accounted for at a rigorous quantum-mechanical level, while dissipation phenomena due to interaction with phonons are described by the Boltzmann scattering operator. A quantum Monte Carlo (QMC) method for solving the equation has been recently proposed. The method, based on a scattering interpretation of the Wigner operator, computes averages of physical quantities by using a statistical weight which is accumulated during the simulation. When real quantum devices are considered, the accumulated weight leads to a large variance of the simulation results – the so-called sign problem in stochastic simulations of quantum-mechanical processes.

The QMC method has been modified in a way which avoids this problem. Dissipation and interference phenomena are associated by two alternative processes of transport of quasi-particles. Dissipation caused by phonons is accounted for by drift and scattering processes corresponding to semi-classical Boltzmann transport. Interference effects due to the Wigner potential are associated with the generation of couples of particles having a statistical weight of ± 1. The classical force term is separated from the Wigner potential and included in the Liouville operator. With this modification, the developed model corresponds to a Boltzmann equation augmented by a generation term. The challenge of employing such a model is

to handle the avalanche of numerical particles properly. The problem has been solved by storing the generated particles in the phase space. Particles of opposite weight and with a sufficiently small distance in phase space are continuously removed in the course of a simulation. Indeed, positive and negative states make opposite contributions to the statistics. They have the same probabilistic future if located close together, and thus can be canceled. The active cancellation reduces the time for simulation of these states, which leads to a variance reduction.

Simulations of resonant tunneling diodes have been successfully carried out with this approach. The resulting effects of tunneling and dissipation are in agreement with those of other simulation tools. The method allows an easy integration with the existing Monte Carlo (MC) codes, since it simplifies gradually to the classical MC method when the classical limit is approached. Thus, a seamless transition between classical and quantum transport calculations is achieved.

Mihail Nedjalkov was born in Sofia, Bulgaria. He received the M.S. degree in semiconductor physics at the Sofia University 'St. K. Ohridski' and the Ph.D. degree at the Bulgarian Academy of Sciences (BAS). He worked for twelve years at the Departments of Physical Analysis and Theoretical Research at the 'Institute of Microelectronics', Sofia. His permanent position is with the Central Laboratory for Parallel Processing, BAS, Sofia. He was a visiting researcher at the Universities of Bologna, 1992; Modena, 1994 and 1995; and Frankfurt, 1997. Since 1998 he has been holding a visiting research position at the 'Institut für Mikroelektronik' at the 'Technische Universität Wien'. Besides the national research projects he participated in INFM (Italy) and FWF (Austria) projects. Currently he is supported by the European Commission project NANOTCAD. His research interests include numerical theory and application of the Monte Carlo method, physics and modeling of Boltzmann and quantum transport in semiconductors and devices.

Analysis and Simulation of Advanced Heterostructure Devices

Vassil Palankovski

Technology Computer-Aided Design (TCAD) methodologies are extensively used in development and production. Several questions during device fabrication, such as performance optimization and process control, can be addressed by simulation. The choice of a given simulation tool or a combination of tools depends to a large extent on the complexity of the particular task, on the desired accuracy of the problem solution, and on the available human, computer, and time resources.

Optimization of geometry, doping, materials, and material compositions targets high output power, high breakdown voltage, high speed, low leakage, low noise, and low power consumption. This is a challenging task that can be significantly supported by device simulation. While DC simulation is sufficient for optimization of breakdown voltages, turn-on voltages, or leakage currents, AC simulation is required for speed, noise, and power issues.

There are several challenges which are specific for modeling and simulation of heterostructure devices. The characterization of the physical properties of SiGe and III-V compounds is required for wide ranges of material compositions, temperatures, doping concentrations, etc. Physics-based analytical models for the lattice, thermal, band-structure, and transport properties of various semiconductor materials, as well as models for important high-field and high-doping effects taking

place in the devices, are derived and implemented in our three-dimensional device simulator MINIMOS-NT. Special attention is paid to modeling of the properties of SiGe with respect to material composition and strain due to lattice mismatch. Another interesting aspect is the modeling of novel materials and devices. For example, the GaSb or the GaN material systems enable advanced devices such as InP/GaAsSb/InP or AlGaAs/InGaAsN/GaAs Heterojunction Bipolar Transistors.

Heterojunction Bipolar Transistors (HBTs) and High Electron Mobility Transistors (HEMTs) are among the most advanced high-frequency devices. The most recent achievements in numerical simulation for industrial heterostructure devices, together with relevant applications (GaAs, InP, and SiGe HBTs; GaAs, InP, and GaN-based HEMTs) are presented in the new book *Analysis and Simulation of Heterostructure Devices* by Palankovski and Quay in the Springer-Verlag series 'Computational Microelectronics'.

Vassil Palankovski was born in Sofia, Bulgaria, in 1969. He received the diploma degree in electronics from the Technical University of Sofia in 1993. Afterwards he worked for three years in the telecommunications field. In 1997 he joined the 'Institut für Mikroelektronik' at the 'Technische Universität Wien', where he received the doctoral degree in technical sciences in 2000 and is currently employed as a post-doctoral researcher. In summer 2000 he held a visiting research position at LSI Logic Corporation, Milpitas, California. His scientific interests include device and circuit simulation, heterostructure device modeling, and semiconductor physics. In 2003, Dr. Palankovski and Dr. Quay published the book *Analysis and Simulation of Heterostructure Devices* in the Springer-Verlag series 'Computational Microelectronics'.

Simulation of Smart Power Devices with Novel Device Concepts

Jong Mun Park

Lateral double diffused MOS transistors (LDMOSFETs) and lateral insulated-gate bipolar transistors (LIGBTs) on SOI (Silicon on Insulator) have attracted much attention in a wide variety of applications such as automotive applications, consumer electronics, and industrial applications. Advantages of SOI technology are the superior isolation, reduced parasitic capacitances, and the superior high temperature performance compared to the junction isolation. These advantages allow efficient monolithic integration of multiple power devices and low-voltage control circuitry on a single chip. The main issues in the development of these devices are to obtain the best trade-off between the on-resistance and the breakdown voltage (BV), and to shrink the feature size without degrading device characteristics.

New structures such as super-junctions (SJ) and hybrid SOI LDMOS-IGBTs have been proposed. The SJ can be achieved by introducing alternating n and p columns in the drift region, allowing the doping in this region to increase drastically. This results in a significant reduction of the on-resistance of the devices. Lateral IGBTs on SOI simultaneously handle a high voltage and a large current. The practical maximum current rating is limited by chip area consumption. Thus, it is extremely important to increase operating current density in order to reduce chip size as well as chip cost in high-voltage power-ICs.

To obtain the best trade-off between on-resistance and BV, we suggest a SJ SOI-LDMOSFET. The extra p-column is doped to achieve a balanced charge condition at the drift region. The trench oxide in the drift region helps to reduce the drift length. The on-resistance of the proposed structure is effectively reduced by the SJ concept together with the trench oxide. SJ helps to increase the doping concentration of the n-drift layer, and the trench oxide in the drift region allows the device size to be reduced. Lowering on-resistance without degrading the BV gives rise to a reduction in silicon area, and it makes the economic fabrication of smart power devices possible.

We describe new shorted-anode lateral insulated-gate bipolar transistors (SA-LIGBTs) on SOI. The trench oxide at the drain/anode region effectively suppresses the snap-back voltage inherent in the conventional SA-LIGBT without increasing the anode length of the device. A weak negative differential resistance region is observed in the proposed device. The SA-LIGBT on SOI allows a large current density compared to the SOI-LDMOSFET, and the shorted-anode helps to achieve a faster turn-off time compared to the conventional SOI-LIGBT.

Jong Mun Park was born in Seoul, Korea, in 1961. He studied electronics engineering at the 'Hanyang University', where he received the degree of Master of Science in 1985. Afterwards he was a senior researcher at the Power Semiconductor Group at KERI, National Laboratory in Korea, where he carried out several projects for developing power semiconductor devices. He joined the 'Institut für Mikroelektronik' in March 2001, where he is currently working on his doctoral degree. His scientific interests include optimization and modeling of power semiconductor devices, Silicon Carbide (SiC) power devices, smart power ICs, and Intelligent Power Modules (IPMs).

Accurate Three-Dimensional Interconnect Simulation

Rainer Sabelka

As integrated circuit technology is scaled into the deep submicron regime, the problems associated with on-chip interconnects are ever more pressing and could potentially become the roadblock to progress. While downscaling generally results in faster semiconductor devices, the performance of the metal interconnect lines is limited by various parasitic effects such as crosstalk, delay times, self-heating due to losses, skin-effect and eddy currents, or degradation due to electromigration. The progression to copper metalization and low-k dielectrics improves reliability and reduces parasitic effects to a certain degree, but cannot eliminate them. Hence, interconnect parasitics must be taken into account during the design process at an early stage, and highly accurate models are required.

For this reason the Smart Analysis Programs (SAP) have been developed. This simulation package contains tools for highly accurate parasitics (RLC) extraction, quasi-electrostatic and quasi-magnetostatic simulation using time- and frequency-domain methods, and investigation of the thermal behavior of interconnect stacks. Special attention has been given to an efficient implementation concerning both run time and memory consumption. The finite element method (FEM) is used for the numeric solution of the partial differential equations.

For highly accurate simulations it is essential to model the simulation domain geometrically as exactly as possible. Two- and

three-dimensional solid modelers are used either to construct the simulation geometry directly with an input deck or to generate it automatically from a layout file in CIF or GDS2 format. The simulation grid is either generated by a layer-based technique or with a fully unstructured Delaunay mesher.

Back-end process steps (lithography, etching, deposition, CMP) are far from being ideal, resulting in deviations of the fabricated structures from the layout geometry. To investigate the influence on electrical interconnect parameters and reliability behavior we have successfully coupled the Smart Analysis Programs to process simulators based on cellular or surface displacement algorithms.

Recent enhancements to the simulation package include the adoption of the WAFER STATE SERVER file format to improve the interoperability with other simulation tools and an optimized two-dimensional inductance calculation module including skin-effect visualization. A heuristic model for the estimation of electromigration lifetime based on the distributions of current density and temperature is currently under development.

Rainer Sabelka was born in Vienna, Austria, in 1969. He studied electrical engineering at the 'Technische Universität Wien', where he received the 'Diplomingenieur' and Ph.D. degrees in 1994 and 2001, respectively. He joined the 'Institut für Mikroelektronik' in January 1995. He held visiting research positions at Digital Equipment Corporation, Hudson, USA, in 1996; Sony, Atsugi, Japan, in 1997; and HP Invent, Shrewsbury, USA, in 2002. His scientific interests include three-dimensional interconnect simulation of multilevel wired VLSI circuits, visualization, and software technology.

A General Topography Simulator for Deposition and Etching Processes

Alireza Sheikholeslami

Deposition and etching of silicon trenches are crucial processes in semiconductor manufacturing for state-of-the-art memory cells, power MOSFETs, and other advanced devices. Simulation of these processes enables the prediction of resulting profiles and eventually voids, and thus optimizing the process parameters depending on electrical characteristics of the device. In backend processes for memory cells, interlayer dielectric (ILD) materials and processes result in void formation. Voids lower the intermetal capacitance and thereby reduce the time delay. This is becoming more and more important with shrinking design rules. Therefore, void formation may be used in a controlled manner to substitue low-k materials.

For simulating the above mentioned processes, one always needs to describe a moving boundary (usually the surface of the wafer), which requires the proper treatment of the chemical and physical processes.

The level set method provides spatial grid resolution which is higher than the resolution of the original grid. In contrast to other methods, such as the cellular format, the level set method does not have the accuracy problems caused by the surface normals.

Using this method, we have developed a general topography simulator called ELSA (Enhanced Level Set Applications), which consists of three modules: a module for transport of

particles by radiosity, a chemical surface reaction module, and a level set module. It can be used for all common deposition and etching processes. Its main advantages are an efficient and precise level set algorithm, which significantly reduces the computational demands, while ensuring high resolution in critical areas. Furthermore, we have used the level set method to generate structurally aligned grids whose elements fulfill desirable requirements, such as Delaunay triangulation and the minimum angle criterion, which can well control the shape of the grid. This technique was used to generate a grid for a trench gate MOSFET, which very finely resolves the junction areas as required.

In cooperation with Cypress Semiconductor Corporation, USA, Infineon Technologies, Villach, Austria, and Toshiba, Kawasaki, Japan, the application of level set methods to tracking different structures of trenches under different process conditions in the semiconductor manufacturing of electronic components was studied and simulated. Good overall agreement between measurements and simulations was obtained.

Alireza Sheikholeslami was born in Babol, Iran, in 1971. He studied electrical engineering at the University of Science and Technology in Tehran and at the 'Technische Universität Wien', where he received the degrees of 'Engineer in Electronics' and 'Diplomingenieur' in 1994 and 2002, respectively. He joined the 'Institut für Mikroelektronik' in April 2002, where he is currently working on his doctoral degree. His scientific interest is focused on the numerical simulation of semiconductor process technologies.

Monte Carlo Modeling of Strained SiGe Grown on Arbitrarily Oriented SiGe Substrates

Sergey Smirnov

Strain induced by lattice mismatch is a widely studied option to enhance transport properties of advanced semiconductor devices. One of the strain effects is the degeneracy reduction of band states with different quasi-momentum which are degenerate in the relaxed material due to the symmetry of a crystal. This reduction depends on the relative orientations of the quasi-momentum for a given band state and the stress direction.

To calculate the behavior of the low-field mobility, the one-particle Monte Carlo algorithm is usually applied at a very low magnitude of the electric field. However, this approach has several disadvantages. The main problem is a high variance in the results at low magnitudes of the electric field. Another drawback of the conventional approach is that it yields the mobility component only in the direction of the electric field. To avoid these problems we have modified a zero-field Monte Carlo algorithm which gives the whole mobility tensor. This is important when strain is present, since in this case there is no need to perform several simulations.

To take the influence of the substrate orientation into account, we have introduced Euler's angles to specify this orientation. Linear deformation-potential theory is used to calculate conduction band minima splitting of different valleys. The trans-

formation of the coordinate system is performed by two successive rotations. In addition to biaxial in-plane strain, the condition of zero perpendicular stress is implied to calculate the strain tensor elements. The strain tensor is not diagonal for a general substrate orientation, which leads to the splitting of different valleys.

To investigate the behavior of the low-field mobility we have developed a new zero-field Monte Carlo algorithm. This algorithm differs from the previous one by taking into account the quantum mechanical Pauli exclusion principle in the scattering operator. We have found that the total scattering rate turns out to be a linear combination of the forward and backward scattering rates for inelastic processes. It has been shown that at high degeneracy the backward scattering rate is dominant, which means that the kinetics is reversed. The physical reason is that the scattering to lower energy levels is quantum-mechanically forbidden. The method has been extended to the small-signal analysis of high-field transport, where a new rejection technique has been developed to solve a Boltzmann-like kinetic equation with an arbitrary shape of the stationary distribution function.

Sergey Smirnov was born in Skhodnya, Moscow Region, Russia, in 1976. He studied physics and technology of VLSI at the Moscow State Institute of Electronic Technology (MIET), where he received the degree of Master of Science in 1999. Afterwards he was a research fellow at MIET, where he studied the numerical simulation of semiconductor devices. He joined the 'Institut für Mikroelektronik' in January 2002, where he is currently working on his doctoral degree. His scientific interests include physical modeling of strained silicon/silicon-germanium devices, Monte Carlo methods, and solid-state theory.

Simulation of Carbon Nanotube FETs with MINIMOS-NT

Enzo Ungersböck

Carbon nanotubes (CNTs) belong to the most promising candidates for future nanoelectronic applications. Experiments and theory have shown that the tubes can either be metals or semiconductors. Their electrical properties can rival, or even exceed, the best metals or semiconductors known. The electrical behavior is a consequence of the electronic band structure which depends on the exact position of the carbon atoms forming the tube. Semiconducting nanotubes can be used as active elements in field-effect transistor (FET) designs.

Recently models to describe the transport properties of carbon nanotubes have been developed. It was shown that carbon nanotubes act as unconventional Schottky barrier transistors. Transistor action is achieved by varying the contact resistance rather than the channel conductance. Transport through the nanotube is ballistic, so the current predominately depends on energy barriers between the source and drain contacts. Since the shape of this energy barrier and, hence, the operation of the transistor depend crucially on the device geometry, device simulation becomes necessary to predict device performance.

The device simulator MINIMOS-NT was used to simulate transistors with laterally and axially aligned carbon nanotubes. It was shown that transport through carbon nanotube devices can be understood as either tunneling or thermionic emission, depending on the device geometry.

Transport in axial CNT-FETs can be described assuming thermionic emission. Compared to lateral CNT-FETs, they show worse device characteristics while being more suitable for large-scale integration. A compact model for axial CNT-FETs has been implemented in MINIMOS-NT and was used to study the electrical behavior of memory cells and memory arrays of CNT-FETs on a circuit level.

Lateral CNT-FETs allow good coupling between gate and tube, enabling output characteristics with good $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratios. A distributed model for lateral CNT-FETs has been developed and implemented in MINIMOS-NT. Simulations show that for lateral CNT-FETs the dominant process is tunneling through the Schottky barriers at source and drain. Simulation results exhibit good agreement to experimental data; however, the model has to be enhanced in order to account for the linear increase of the drain current I_{d} at high drain voltages of fully turned-on devices.

Further work will concentrate on three-dimensional device simulations and the simulation of tunneling to and from the CNT using MINIMOS-NT.

Enzo Ungersböck was born in Vienna, Austria, in 1977. He studied physics at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in May 2002. He joined the 'Institut für Mikroelektronik' in June 2002, where he is currently working on his doctoral degree. His scientific interests include simulation of carbon nanotubes, Monte Carlo methods, and quantum mechanical confinement in submicron MOSFETs.

The MINIMOS-NT Small-Signal Analysis Mode

Stephan Wagner

The previous versions of MINIMOS-NT provided only two simulation modes: the basic steady-state DC mode and the transient simulation mode that takes all time derivatives in the time domain into account. Using the transient mode, small-signal analysis is very inconvenient and costly. This was the basic motivation for considering the development of a small-signal or AC analysis mode which provides the capability to simulate directly in the frequency domain. In addition to the single device simulator, the circuit simulator of MINIMOS-NT has been equipped with small-signal capabilities.

Basically, three main steps of this development can be outlined. First, the linear solver module was upgraded to solve complex-valued linear systems, since differentiating a function in the time domain corresponds to multiplying its Fourier transform by $j\omega$, according to the time differentiation property of the Fourier transform. Second, all relevant models and interaction structures had to be modified to take the complex-valued coefficients into account. Third, a set of additional features based on the small-signal simulation mode was implemented.

Two core modules of MINIMOS-NT are responsible for assembling and solving the linear systems created during each Newton approximation iteration. The assembly system assures the fulfillment of several requirements of the simulation process and applies measures to improve the condition of the system

matrix. The completely assembled linear system is then passed to the solver system, which is responsible for the calculation of the solution vector using either a direct Gaussian solver or, more efficiently, one of the iterative linear solver algorithms.

At the moment, two non-stationary iterative methods are provided in combination with an incomplete factorization preconditioner: the Biconjugate Gradients Stabilized (BI-CGSTAB) method and a restarted version of the Generalized Minimal Residual (GMRES) method. To also meet future requirements, such as the efficient solving of huge linear equation systems arising from three-dimensional device or process simulation, alternative solver systems have been evaluated and plugged into the solver module.

Several features for small-signal simulations are now provided by the device and circuit simulator, for example calculation of the admittance and scattering matrices and the efficient extraction of various small-signal parameters (Y-, Z-, S- and H-parameters) or related figures of merit (cut-off frequency f_{T}, maximum oscillating frequency $f_{\max}$, etc.). In order to take parasitics introduced by the measurement setup into account, single devices can be embedded in a standard two-port circuit, which easily allows the extraction of the extrinsic parameters.

Stephan Wagner was born in Vienna, Austria, in 1976. He studied electrical engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 2001. He joined the 'Institut für Mikroelektronik' in November 2001, where he is currently working on his doctoral degree. His scientific interests include device and circuit simulation and software technology.

Three-Dimensional Mesh Adaption

Wilfried Wessner

The generation of locally adapted conforming tetrahedral meshes is an important component of many modern algorithms in the finite element solution of partial differential equations. Typically, such meshes are produced by starting with a coarse initial tetrahedral mesh followed by mesh adaption on demand over space and time. During the calculation of a time step a combination of error estimation and refinement is necessary to deliver higher accuracy, if needed, by increasing the spatial resolution. Features for refinement based on different kinds of error estimations and refinement methods applied to an initial mesh have been added to the three-dimensional Finite Element Diffusion and Oxidation Simulator FEDOS.

Using strict isotropic meshes for three-dimensional process simulation is not practicable. The need for calculation time and the limitation of memory tends to result in anisotropic adapted meshes which are more manageable. The idea is to create tetrahedral elements with special geometric qualities by manipulation of an initial coarse mesh. The basic manipulation step in our work is tetrahedral bisection. When bisecting a tetrahedron, a particular edge – called the refinement edge – is selected for the new vertex. As new tetrahedra are constructed by refinement, their refinement edges must be selected carefully to take an anisotropic shape into account and not to produce degenerately shaped elements. Different kinds of refinement methods have been implemented, investigated, and added to FEDOS.

In the numerical solution of practical problems of semiconductor device and process simulation, one often encounters the difficulty that the overall accuracy of the numerical approximation is deteriorated by local singularities. An obvious remedy is to refine the discretization in the critical regions. The question is how to identify these regions and how to obtain a good balance between the refined and unrefined regions such that the overall accuracy is optimum. These considerations clearly show the need for error estimators which can be extracted *a posteriori* from the computed numerical solution and the given data of the problem. The error should be local and should yield reliable upper and lower bounds. The global upper bounds are sufficient to obtain a numerical solution with an accuracy below a prescribed tolerance. Local lower bounds are necessary to ensure that the grid is correctly refined to obtain a numerical solution with a prescribed tolerance using a (nearly) minimum number of grid points. Several error estimators have been implemented in FEDOS. An interface which supports an error-driven refinement has been added in order to provide powerful and flexible coupling between error estimation and mesh refinement.

Wilfried Wessner was born in Horn, Austria, in 1977. He studied computer engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 2002. He joined the 'Institut für Mikroelektronik' in summer 2002, where he is currently working on his doctoral degree. His scientific interests include three-dimensional mesh generation, anisotropic mesh adaption, computational geometry, and data visualization.

Accurate Three-Dimensional Monte Carlo Simulation of Ion Implantation

Robert Wittmann

Ion implantation is still the most important doping technique in the manufacturing of modern semiconductor devices. The small dimensions of deep-submicron MOS devices in ULSI circuits have led to simulation applications which require a highly accurate and fully three-dimensional implantation treatment. Since the process of ion implantation has a statistical nature, it is straightforward to use statistical methods to imitate it on computers. The Monte Carlo method, which is based on applying random behavior at an atomistic level, is used to calculate the distribution of implanted dopants and generated point defects. The application of this stochastic simulation model is computationally expensive but produces realistic and accurate doping profiles.

The Monte Carlo ion implantation simulator MCIMPL has been developed over numerous years. MCIMPL is an object-oriented, multi-dimensional simulator, embedded in a process environment. The simulator is based on a binary collision algorithm and can handle arbitrary three-dimensional device structures consisting of several amorphous materials and crystalline silicon.

Without a proper statistical analysis of the simulation output data, it is not possible to assess the statistical accuracy of three-dimensional Monte Carlo simulation results. The statistical accuracy is basically determined by the number N of

simulated ion trajectories. It also depends on the variation of the ion concentration up to several orders of magnitude in the simulation domain. The theoretical simulation error is of the order $1/\sqrt{N}$, as verified by simulation experiments. The evaluation of the accuracy of three-dimensional applications has been performed by using statistical methods such as calculating the standard deviation or the confidence interval of the output data.

The statistical fluctuation of the predicted doping profile can be significantly reduced by smoothing the raw Monte Carlo simulation output data in a postprocessing step. The smoothing algorithm has been extended by calculating the gradient of the ion concentration in order to enhance the results. The impact of the advanced postprocessing procedure on the accuracy of three-dimensional applications has been analyzed.

In the near future it is intended to extend the simulator to include compound materials, such as GaAs. In addition, it is planned to speed up the simulator by parallel processing so that it will be possible to accomplish highly accurate three-dimensional applications within reasonable time.

Robert Wittmann was born in Vienna, Austria, in 1966. He studied computer engineering at the 'Technische Universität Wien', where he received the degree of 'Diplomingenieur' in 2002. From 1989 to 1997 he worked as an engineer in the Development Department at the company Kapsch, Vienna. He joined the 'Institut für Mikroelektronik' in June 2002, where he is currently working on his doctoral degree. His scientific interests include simulation of ion implantation, statistical analysis of Monte Carlo simulations, parallel processing, and software technology.

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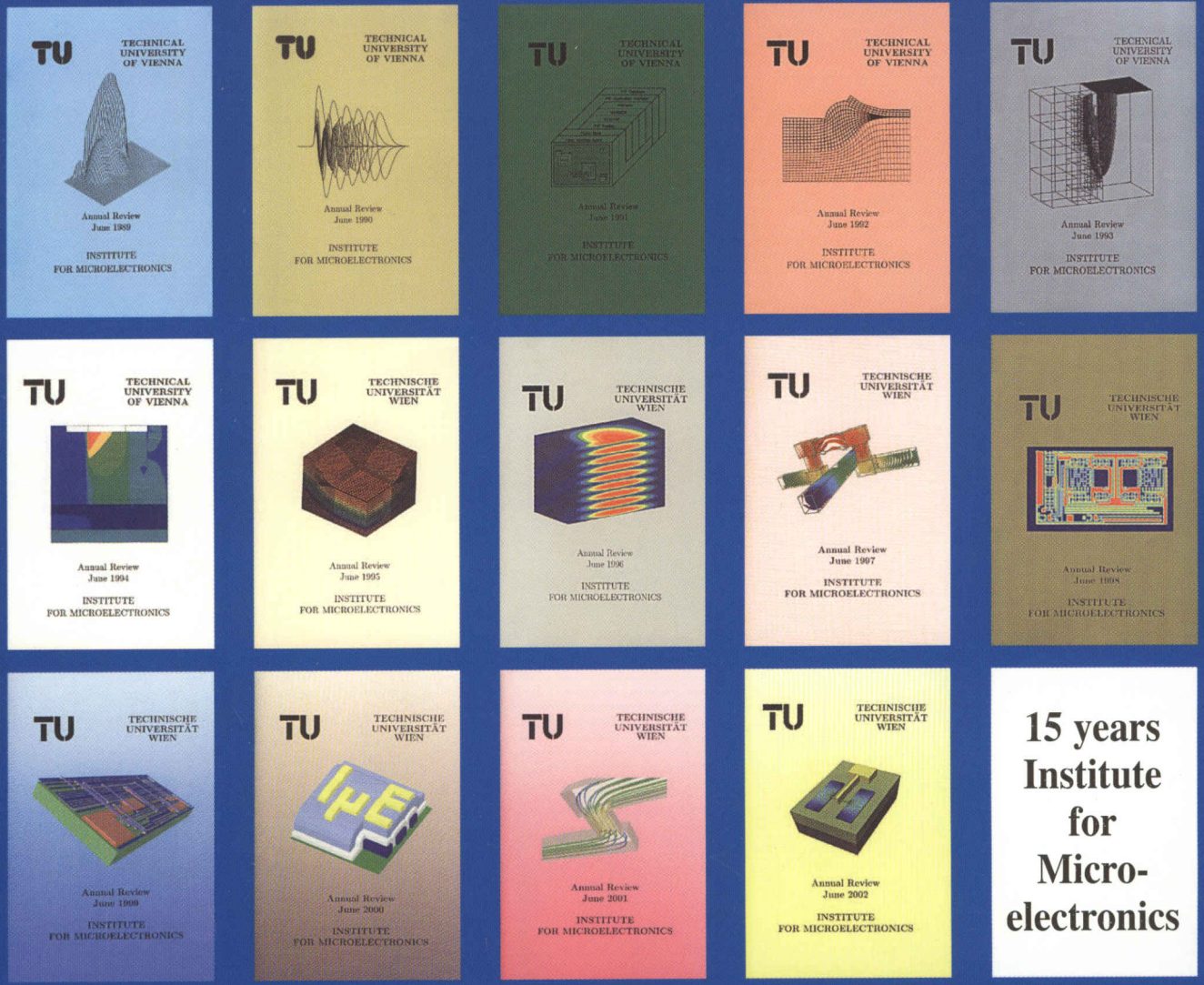
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