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1 The Failure of the Hydrodynamic Transport Model

1.1 Introduction

Using the standard hydrodynamic (HD) transport model for simulation of partially depleted SOI MOS-FETs, an anomalous decrease of the drain current with increasing drain-source voltage has been observed (Fig. 1). The anomalous effect has been reproduced using the two different device simulators MINIMOS-



Figure 1: Output characteristics obtained by standard HD simulations; verified by using two different device simulators.

NT [1] and DESSIS [2], and can be explained by an enhanced diffusion of channel hot carriers into the floating body [3] [4]. It is believed that this decrease in drain current is an artifact because experimental data do not show this effect, nor can it be observed when using the drift-diffusion (DD) transport model. One exception is given in [5], where a weak decrease of the measured drain current of a p-MOS SOI is reported.

However, applicability of the HD model to the ever down-scaled devices is desirable, because in contrast to the DD model it takes non-local effects into account. Empirical measures provided by DESSIS, such as weighting heat flow and thermal diffusion, have only little influence on the current drop. This paper presents a revision of the HD model which enables proper simulation of SOI MOSFETs.

1.2 Cause of the Effect

The main difference between the HD and the DD transport model is given by the energy balance equation. The benefit of the increased computational effort of solving an additional equation is that the carrier temperature can differ from the lattice temperature. Since the diffusion of the carriers is proportional to their temperature, the diffusion can be significantly higher with the HD transport model. Fig. 2 clearly shows the enhanced vertical diffusion of electrons as compared with the DD result in Fig. 3.

When simulating SOI MOSFETs this increased diffusion has a strong impact on the body potential, because the hot electrons of the pinch-off region have enough energy to overcome the energy barrier towards the floating body region and thus enter into the sea of holes. Some of these electrons in the floating body

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Figure 2: Electron concentration in an SOI MOSFET obtained by a HD simulation.



Figure 3: Electron concentration in an SOI MOSFET obtained by a DD simulation.

are collected by the drain-body and source-body junctions, but most recombine. The holes removed by recombination cause the body potential to drop. A steady state is obtained when the body potential reaches a value which biases the junctions enough in reverse direction so that thermal generation of holes in the junctions can compensate this recombination process. The decrease in the output characteristics is directly connected to the drop of the body potential via the body-effect.

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1.3 Weight Factors

Our first attempt to avoid the anomalous current decrease was to tune the empirical weight factors of thermal diffusion and heat flow, as provided by the HD model of DESSIS. Within this parameter-space only minor improvements in the IV characteristics were possible. Therefore, our investigations continued with more physically motivated modifications using MINIMOS-NT.

1.4 Modifications

In Monte-Carlo (MC) simulations the spreading of hot carriers away from the interface is much less pronounced than in HD simulations. If we assume that the BOLTZMANN equation does not predict the hot carrier spreading, and if the HD equations derived from the BOLTZMANN equation do so, the problem must be introduced by the assumptions made in the derivation of the HD model. Relevant in this regard is the approximation of tensor quantities by scalars and the closure of the hierarchy of moment equations.

In order to capture more realistically the phenomenon of hot carrier diffusion we derived a HD equation set from the BOLTZMANN equation permitting an anisotropic temperature and a non-MAXWELLian distribution function:

$$J_{n,\xi} = \mu_n \left(\mathbf{k}_{\mathrm{B}} \, \nabla_{\xi} \left(n \, T_{\xi\xi} \right) + \mathbf{q} \, E_{\xi} \, n \right) \tag{1}$$

$$S_{n,\xi} = -\frac{5}{2} \frac{\mathbf{k}_{\mathrm{B}}}{\mathbf{q}} \mu_{S} \left(\mathbf{k}_{\mathrm{B}} \nabla_{\xi} \left(n \beta_{n} T_{\xi\xi} \Theta \right) + \mathbf{q} E_{\xi} n \Theta \right)$$
(2)

with
$$\nabla_{\xi} = \frac{\partial}{\partial \xi}$$
 and $\Theta = \frac{3T_n + 2T_{\xi\xi}}{5}$ (3)

 $T_{\xi\xi}$ denotes the diagonal component of the temperature tensor for direction \vec{e}_{ξ} . Off-diagonal components are neglected. β_n is the normalized moment of fourth order.

By setting $T_{\xi\xi} = T_n$ and $\beta_n = 1$ the conventional HD model is obtained. The solution variable is still the carrier temperature T_n , whereas the tensor components and β_n are modeled empirically as functions of T_n . First empirical modeling of $T_{\xi\xi}$ was performed by distinguishing between directions parallel and normal to the current density:

$$T_{\xi\xi} = T_{xx} \cos^2 \varphi + T_{yy} \sin^2 \varphi , \ T_{xx} = \gamma_x T_n , \ T_{yy} = \gamma_y T_n \tag{4}$$

$$\gamma_{\nu}(T_n) = \gamma_{0\nu} + \left(1 - \gamma_{0\nu}\right) \exp\left(-\left(\frac{T_n - T_L}{T_{\mathrm{ref},\gamma}}\right)^2\right), \ \nu = x, y \tag{5}$$

The anisotropy functions $\gamma_{\nu}(T_n)$ assume 1 for $T_n = T_L$ and an asymptotic value $\gamma_{0\nu}$ for large T_n (Fig. 4), ensuring that only for sufficiently hot carriers the distribution becomes anisotropic, whereas the equilibrium distribution stays isotropic (Fig. 5). With respect to numerical stability the transition should not be too steep. $T_{ref,\gamma} = 600$ K appeared to be appropriate.

Another effect observed in MC simulations is that in most parts of the channel the high energy tail is less populated than that of a MAXWELLian distribution, which gives $\beta_n < 1$ (Fig. 6).

$$\beta_n(T_n) = \beta_0 + \left(1 - \beta_0\right) \, \exp\left(-\left(\frac{T_n - T_L}{T_{\text{ref},\beta}}\right)^2\right) \tag{6}$$

Again, this expression ensures that only for sufficiently large T_n the distribution deviates from the MAXWELLian shape.



Figure 4: Shape of the function used to model γ and β .



Figure 5: MC simulation of an *nin*-structure showing the x-component of the temperature compared to the mean temperature $T_{n,MC}$. The analytical T_{yy} uses $\gamma_{0\nu} = 0.75$.

1.5 Results

The modified flux equations have been implemented in MINIMOS-NT using a straight forward extension of the Scharfetter-Gummel discretization scheme. Numerical stability does not degrade as compared to standard HD simulations. Parameter values were estimated from MC results for one-dimensional test structures.

As a first example simulations were performed on a device with an assumed effective gate-length of 130 nm, a gate-oxide thickness of 3 nm, and a silicon-film thickness of 200 nm. With a p-doping of $N_A = 7.5 \cdot 10^{17} \text{ cm}^{-3}$ the device is partially depleted. The Gaussian-shaped n-doping under the electrodes has a maximum of $N_D = 6 \cdot 10^{20} \text{ cm}^{-3}$.

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Figure 6: MC simulation of a *nin*-structure showing the normalized moment of fourth order $\beta_{n,MC}$ compared to the analytical β_n with $\beta_0 = 0.75$.



Figure 7: Output characteristics of the SOI obtained by anisotropic HD simulations without closure modification ($\beta_0 = 1$).

Fig. 5 indicates that $\gamma_{0y} = 0.75$ is a realistic value for the anisotropy parameter. Fig. 7 shows the influence of γ_{0y} on the output characteristics. By accounting for a reduced vertical temperature it is possible to reduce the spurious current decrease, but only to a certain degree and by assuming a fairly large anisotropy. MC simulations yield values close to $\beta_0 = 0.75$ for the non-MAXWELLian parameter in the channel region (Fig. 6). This parameter shows only a weak dependence on doping and applied voltage.

By combining the modifications for an anisotropic temperature and a non-MAXWELLian closure relation the artificial current decrease gets eliminated (Fig. 8). Parameter values roughly estimated from MC simulations can be used, e.g. $\gamma_{0y} = 0.75$ and $\beta_0 = 0.75$. In the parameter range where the current drop is eliminated the output characteristics are found to be rather insensitive to the exact parameter values.



Figure 8: Output characteristics of an SOI-MOSFET with analytical doping profile assuming an anisotropic temperature ($\gamma_{0y} = 0.75$) and a modified closure relation. $V_{GS} = 1 V$.

To verify the modified hydrodynamic transport model, a second device has been investigated. Basically this SOI has been modeled after the 90 nm "Well-Tempered" MOSFET [6] using the doping profiles available online, including the SSR channel doping and source/drain halo. To achieve a partically depleted device a substrate doping of $N_A = 7.5 \cdot 10^{17} \text{ cm}^{-3}$ has been assumed and the substrate thickness has been limited to 200 nm.

By using the standard HD transport model the drop in the drain current is also present in this device $(\beta_0 = 1.0, \gamma_{0y} = 1.0 \text{ in Fig. 9})$. Applying the modified model using the same parameters as before the output characteristics obtains its normal shape.

The different order of magnitude of the drain currents seen with Device 1 and Device 2 mainly stems from the rather high threshold voltage of Device 1.

1.6 Conclusion

Standard HD simulations of SOI MOSFET give anomalous output characteristics. To solve this problem, an improved HD transport model has beed developed. By including two distinct modifications, namely an anisotropic carrier temperature and a modified closure relation, the spurious diffusion of hot electrons in the vertical direction has been sufficiently reduced. The improved hydrodynamic transport model has successfully been used to simulate different SOI devices.



Figure 9: Output characteristics of the "Well-Tempered" SOI. $V_{GS} = 1 V$.

2 Topography Simulation of Deposition and Etching Processes

Etching and deposition of Silicon trenches is an important semiconductor manufacturing step for state of the art memory cells and other semiconductor devices like, e.g., Power MOSFETs. Understanding and simulating the transport of gas species and surface evolution enables to achieve void-less filling of deep trenches, to predict the resulting profiles, and thus to optimize the process parameters with respect to manufacturing throughput and the resulting memory cells.

An accurate and fast method for surface evolution has been combined with the simulation of the transport of gas species above the wafer surface and applied to a SiO₂ deposition process. In experiments a SiO₂ layer was deposited into trenches roughly $4\mu m$ deep and $2\mu m$ wide, where the final layer thickness was in the range of $1\mu m$ for the flat wafer surface. Simulation results are discussed and compared to scanning electron microscope pictures, where all effects were reproduced in the simulation and good quantitative agreement was achieved as well.

2.1 Introduction

When simulating etching and deposition processes for semiconductor manufacturing, an accurate description of moving boundaries is crucial in addition to proper treatment of the chemical and physical processes. In these applications the moving boundaries usually are the surface of a wafer or the surfaces between wafers and deposited layers. One approach is to use a cellular format, where the simulation domain is divided into cubic or cuboid cells and each cell either belongs to the exterior vacuum above the wafer or to its interior [7, 8]. One disadvantage of this method is that computing surface normals and tangents leads to accuracy problems. Surface normals are, e.g., crucial for computing fluxes to the surface for simulating transport phenomena via the radiosity approach.

The level set method [9] provides an interesting alternative and a solution to the above mentioned problem. This method is a relatively new method for describing boundaries, i.e., curves, surfaces or hypersurfaces in arbitrary dimensions, and their evolution in time. Applying this method means solving a certain partial differential equation and extracting the zero level set of its solution.

Firstly, the basic ideas of the level set method are presented. Next extending the so called speed function and a narrow banding algorithm for accelerating simulations are discussed. The two seemingly unconnected concepts are combined in our implementation in order to enable efficient surface evolutions. For the case of radiosity simulations an algorithm for coalescing certain surface elements is presented. Its purpose is to increase accuracy where it is needed most and reduce simulation time by reducing the size of the radiosity matrix.

Secondly, mass transport in the diffusion and radiosity regimes above the wafer is shortly discussed and the modeling approach is described.

Finally, an example where SiO₂ is deposited from TEOS (Tetraethoxysilane) is presented. Simulation results are shown and discussed comparing with SEM (scanning electron microscope) pictures of fabricated test structures. In the experiments a SiO₂ layer was deposited into trenches roughly 4μ m deep and 2μ m wide, where the final layer thickness was in the range of 1μ m for the flat wafer surface. Simulation results for the diffusion and the radiosity regime are presented and discussed, and the algorithms mentioned at the beginning of the paper are illustrated as well.

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2.2 The Level Set Method

The level set method [10, 9] provides means for describing boundaries, i.e., curves, surfaces or hypersurfaces in arbitrary dimensions, and their evolution in time, where the evolution is caused by forces or fluxes normal to the surface. The basic idea is to view the curve or surface in question at a certaim time t as the zero level set (with respect to the space variables) of a certain function $u(t, \mathbf{x})$, the so called level set function [11, 12, 13]. Thus the initial surface is the set $\{\mathbf{x} \mid u(0, \mathbf{x}) = 0\}$.

Each point on the surface is moved with a certain speed normal to the surface and this determines the time evolution of the surface. The speed normal to the surface will be denoted by $F(t, \mathbf{x})$. For points on the zero level set it is usually determined by physical models and in our case by the etching and deposition processes, or more precisely by the fluxes of certain gas species and subsequent surface reactions. The speed function $F(t, \mathbf{x})$ generally depends on time and the space variables, and we assume for now that it is defined on the whole simulation domain and for the time interval considered.

The surface at a later time t_1 shall also be considered as the zero level set of the function $u(t, \mathbf{x})$, namely $\{\mathbf{x} \mid u(t_1, \mathbf{x}) = 0\}$. This leads to the level set equation

$$u_t + F(t, \mathbf{x}) \| \nabla_{\mathbf{x}} u \| = 0,$$

 $u(0, \mathbf{x})$ given

in the unknown variable u, where $u(0, \mathbf{x})$ determines the initial surface. Having solved this equation the zero level set of the solution is the seeked curve or surface at all later times.

Now in order to apply the level set method a suitable initial function $u(0, \mathbf{x})$ has to be determined first. There are two requirements: first it goes without saying that its zero level set has to be the surface given by the application, and second it should essentially be a linear function so that in the final surface extraction step linear interpolation can be applied. A beneficial choice is the signed distance function of a point from the given surface. This function is the common distance function multiplied by minus or plus one depending on which side of the surface the point lies in. The common distance function of a point x from a set M is then defined by $d(x, M) := \inf_{y \in M} d(x, y)$, where d is a metric, usually the Euclidean distance.

In summary, first the initial level set grid is calculated as the signed distance function from a given initial surface. Then the speed function values on the whole grid are used to update the level set grid in a finite difference or finite element scheme. Usually the values of the speed function are not determined on the whole domain by the physical models and therefore have to extrapolated suitably from the values provided on the boundary, i.e., the zero level set. This will be discussed in the next section. In the last step, the surface extraction step, the curve or surface is reconstructed from the function values on the grid, where the zero level set is approximated by lines or triangles using linear interpolation along grid lines.

Of course the use of linear interpolation seems arbitrary and must be justified. It can be shown that if the extension velocity F satisfies $\nabla F \cdot \nabla u = 0$, then the level set function u remains the signed distance function for all time. Hence it has to be ensured that the speed function used fulfills this condition. This is the case with the implementation developed. Now since u remains the signed distance function, which is essentially a linear function, linear interpolation is indeed the best method. Consequently, small changes in the level set function result in small movements of the surface, whereas in the case of a cellular format a cell is either part of the material or not. Thus, although in the numerical application the level set function is eventually calculated on a grid, the resolution achieved is in fact much higher than the resolution of the grid, and hence higher than the resolution achieved using a cellular format on a grid of same size.

The advantages of the level set method are twofold: the resolution achieved is higher than the resolution of the grid where the calculations take place (cf. [14, 15]) and calculating surface normals, crucial for radiosity simulations, is straightforward and much more precise than when using a cellular format.



Figure 10: Overview of the simulation flow combining transport by diffusion and surface evolution using the level set (LS) method. The simulation stops when a prescribed time is reached on when a layer of prescribed thickness has been deposited.

2.3 Extending the Speed Function and Narrow Banding

Before discussing the details of the various simulation steps, the outline of topography simulations for semiconductor processes is given in Fig. 10.

In applications linking to physical models the speed function is not known on the whole simulation domain, but only at the surface. In order to use the level set method it has to be suitably extended from the known values to the whole simulation domain. This can be done iteratively by starting from the points nearest to the surface. Mathematical arguments show that the signed distance functions can by maintained from on time step to the next by choosing a suitable extension.

The idea leading to fast level set algorithms stems from observing that only the values of the level set function near its zero level set are essential, and thus only the values at the grid points in a narrow band around the zero level set have to be calculated. As the zero level set moves, the signed distance function in the narrow band must be maintained.

Both, extending the speed function and narrow banding require constructing the distance function from the zero level set in the order of increasing distance. But calculating the exact distance function from a curve or surface consisting of a large number of small line segments or triangles is computationally expensive and can only be justified for the initialization. An approximation to the distance function can be computed by a special fast marching method [9].



Figure 11: The figures show the surface evolution of a typical trench structure during a deposition processes. The concentration of the diffusing particles above the wafer is between 0 and 1 and it is constantly 1 at the top of the simulatin domain.

For the first time narrow banding and extending the speed function were combined into one algorithm. This algorithm provides several benefits. First, the speed function is retained as the signed distance function throughout the simulation, which assures good accuracy till the end of the simulation. Second, narrow banding reduces the number of active points that have to be updated from $O(n^2)$ to O(n). By retaining the signed distance function the width of the narrow band can be kept down to two points on each side (cf. Fig. 15) without decreasing accuracy. Third, time consuming calculations (cf. [12]) are reduced to a minimum by intertwining the computations necessary for narrow banding and extending the speed function. Finally the width of the narrow band can be adjusted if desired.

An outline of the algorithm is as follows. First the initial points near the zero level set, where the speed function is known, and the neighboring trial points are determined. In the main loop it is checked if there is still a trial point to be considered in the narrow band. All trial points are stored in a heap ordered by their distance to the zero level set. If there is a point to be considered, both its distance is approximated and its extension speed calculated, and its neighbors are updated accordingly. Finally after the main loop, bookkeeping information for the narrow band points is updated using distance information just computed. The computation time consumed by this algorithm is negligible compared to that required for the physical models, while it provides high accuracy.

By intertwining both, extending the speed function and narrow banding, in our implementation expensive calculations are kept to a minimum. Although the level set method is a seemingly computationally expensive method, since it requires solving a partial differential equation for describing surface evolutions, the computation time consumed for the surface evolution by narrow banding is negligible compared to that required for the physical models, e.g., diffusion.

2.4 Transport

In an integrated simulation of transport phenomena and surface evolution the transport phenomena above the wafer surface specify the etch and deposition rates. They can broadly be divided into two classes according to the mean free path length, although this distinction is only a rough classification and the suitable model in each case depends on other considerations as well:

- If the mean free path length is much larger than the diameter of the simulation domain, the collision of single particles can be neglected and the transport can be simulated using the radiosity approach.
- If, on the other hand, the mean free path length is much smaller than the simulation domain, the collisions between single particles play a major role and their concentration is determined by the diffusion equation.

Of course, the question which case to choose for a certain deposition process depends on the conditions of the deposition or etching process to be simulated and more details cannot be presented here. In order to provide a general purposes simulator, both approaches are indispensable.

In the following the modeling of both cases as used in the simulations presented later is described.

2.4.1 Transport in the Diffusion Regime

Here transport is governed by the well-known diffusion equation

$$\frac{\partial c}{\partial t} = \nabla \cdot (D\nabla c),$$

where c is the concentration and D the diffusion coefficient. The boundary conditions (cf. Fig. 11) are usually as follows: at the top of the simulation domain a Dirichlet boundary condition is assumed, i.e., a constant concentration is supplied by the reactor; on the left and right hand side a Neumann boundary concentration is assumed, i.e., the fluxes are zero; and finally the fluxes on the wafer surface are determined by the deposition rates.

2.4.2 Transport in the Radiosity Regime

In this case particles are injected into the simulation domain from sources above the wafer and their way is traced according to reflections from the surface until it attaches itself at a certain location or leaves the simulation domain. How particles are reflected mostly depends on their energy. This model is similar to ray tracing in computer graphics.

A formulation of the radiosity method for the transport of particles of low energy only, where luminescent reflection is assumed, which excludes the case of high energetic particles (i.e., ions), can be found, e.g., in [9]:

Flux =
$$\frac{\beta - \beta_0}{1 - \beta} I_S + + \frac{\beta(1 - \beta_0)}{1 - \beta} \underbrace{L^{-1}(L^{-1} - (1 - \beta)\Psi)^{-1}}_{T:=} I_S,$$

where I_S is the vector of fluxes coming from the sources to the surface elements, β_0 the sticking coefficient for particles coming directly from the source, β the one for secondary bounces, L the diagonal matrix containing the lengths of the surface elements, and

$$\Psi_{ij} = \frac{n_i \cdot (t_j - t_i)n_j \cdot (t_i - t_j)}{\pi |t_j - t_i|^3} [i \text{ visible } j],$$

where t_i are the centroids of the surface elements, n_i their unit normal vectors, and [i visible j] is 1 or 0 if surface element j is visible from i respectively not.

In the case of multiple, low energy species the calculation of the visibility matrix and the inverse T only depends on topographic information and thus does not have to be repeated for each species.



Figure 12: Illustration of the coalescing algorithm. Since the angles at A, B, and C are above the threshold value, no replacement takes place here. The angle at D is below the threshold value, and thus the segments CD and DE are replaced by a new segment CE.

Coarsening	Visibility	Flux	
Steps	Test	Calculation	
0	1	1	
1	0.29	0.10	
2	0.12	0.02	

Table 1: Comparison of the speed of the visibility test and of the calculation of the fluxes on surface elements by radiosity both with the coalescing algorithm and without. The computation time relative to the conventional algorithm, equaling 1, is shown.

2.5 Coalescing Surface Elements

When using radiosity models for simulating the transport of particles above the wafer in the case where the length of the mean free path is greater than the size of the feature, two operations consume most of the computation time. The first operation is determining the visibility between all surface elements, which is an $O(n^2)$ operation where n denotes the number of surface elements extracted from the level set grid. The second operation is solving a certain system of linear equations, which leads to calculating the inverse of a matrix with n^2 elements, which is an $O(n^3)$ operation.

Obviously increasing the number of surface elements is not a remedy in cases where high resolution is required. High resolution is needed, e.g., near the trench opening, and the bottom of the trench, and for the simulation of microtrenching and side wall push back. One approach is to devise a refinement and coarsening strategy for unstructured grids on which the level set equation is numerically solved. This, however, complicates the fast marching algorithm necessary for extending the speed function. A different approach was taken in this work by coarsening the surfaces after having been extracted from the level set grid.

The algorithm works by walking down the list of surface elements extracted as the zero level set and calculating the angle α between two neighboring surface elements. Whenever $|\pi - \alpha|$ is below a certain threshold value of a few degrees, the neighboring elements are coalesced into one. After one sweep through the list, the algorithm can be reapplied for further coarsening. After k coarsening sweeps, at most 2^k surface elements are coalesced into one. The resulting longer surface elements are used for the radiosity calculation, after which the fluxes are translated back from the coarsened elements to the original ones.



(a) SEM image.

(b) Simulated trench.

(c) Zero level sets.

Figure 13: (a): SEM (scanning electron microscope) image of a cross section through a trench about $4 \,\mu m$ deep and $2 \,\mu m$ wide. (b): Simulation result showing the final trench geometry. The TEOS concentration above the wafer in the boundary layer is shown as well. (c): Some intermediate zero level set of the simulation shown in (b).

2.6 Simulation Results

2.6.1 Example of Deposition in the Diffusion Regime

Before discussing the simulations and the effects of the speeding up strategies, the physical modeling approach is shortly described.

In order to calculate the thickness Δd of the film deposited during a time interval of length Δt , we observe that Δd is proportional to Δt , to an Arrhenius term, and to the deposition rate R_i corresponding to the deposition model chosen. This implies $\Delta d = \Delta t \cdot k_e e^{-E/kT} \cdot R_i$. Here $k_e e^{-E/kT}$ is the Arrhenius term with activation energy E, absolute temperature T, and preexponential constant k_e . R_i is the deposition rate of the deposition model chosen, where two heterogeneous deposition models, a homogeneous intermediate-mediated deposition model, and a heterogeneous deposition with byproduct inhibition model are available [16]. This setup also provides a way to determine the actual chemical reaction, which is a non-trivial problem and can only be solved indirectly by comparing measurements and simulation results.

As noted from the characteristic shape of the measurements provided (cf. Fig. 13) and the process conditions employed, the transport of TEOS in the boundary layer above the wafer happens in the diffusion regime and thus is governed by the diffusion equation. The boundary conditions are as follows: at the top of the simulation domain a Dirichlet boundary condition is assumed, i.e., a constant concentration is supplied from the convective zone in the reactor; on the left and right hand side a Neumann boundary concentration is assumed, i.e., the fluxes are zero; and finally the fluxes at the wafer surface are determined by the amount of particles deposited.

The simulation flow for arriving at the results shown in Fig. 11 is depicted in Fig. 10. In Fig. 11 the results of SiO_2 deposition from TEOS are shown. The initial structures are roughly rectangular trenches $4\mu m$

deep and $2\mu m$ wide. Initially the TEOS concentration equals 1 everywhere and the boundary conditions from the previous section were applied, where the concentration at the top was constantly 1.

The depletion of TEOS during the deposition can clearly be seen. This leads to the narrowing of the upper part of the trench, where TEOS is still supplied. Furthermore the stronger depletion in the corners at the bottom of the trench causes the edges to become concave, although they were initially convex. Finally at the upper corners the deposited layer becomes thicker than on the flat layer surface, which might not seem intuitive at first, but is also observed in the SEM pictures.

2.6.2 Example of Deposition in the Radiosity Regime

In experiments SiO_2 was deposited under different process conditions in a different set of trenches for Power MOSFETs with a higher aspect ratio than the trench shown in the SEM image in Fig. 13. For the following simulation results, the radiosity module of the topography simulator was employed.

For adjusting the parameters of the model the topography simulator was used in combination with the optimization framework SIESTA [17, 18]. Hence extracting the model parameters is performed automatically and can be immediately applied to different measurements and structures produced under different process conditions.

A simulation result is shown in Fig. 14, where the surface coalescing algorithm described above was employed. First, the computation time of the level set algorithm with narrow banding as described above (cf. Fig. 15, 16, and 17) is negligible compared to the computation time of the physical models. This, however, is not the case when narrow banding is not employed. Table 1 lists the relative computation time of testing for visibility and the actual radiosity calculation both with and without the coalescing algorithm. The simulation result with coarsening in Fig. 14 is nearly identical to the one yielded when no coarsening was applied. Accuracy is hardly affected, but the simulation time considerably decreased.

2.7 Conclusion

State of the art algorithms for surface evolution processes like etching and deposition processes used for manufacturing semiconductor components have been developed and implemented. The simulator developed consists of three independent modules, namely the level set module, a reaction module, and a diffusion module, which can be used for simulating all common deposition and etching processes as well. Step coverages measured in several SEM images were used for extracting model parameters, where good quantitative agreement was achieved. Hence the process conditions have been optimized with respect to the quality of the trenches and manufacturing throughput.

Two strategies for increasing the accuracy of radiosity simulations are presented and compared to measurements of a deposition process. The first method is an algorithm which performs three level set computations in parallel: calculating the signed distance function via a fast marching algorithm, extending the speed function, and moving the narrow band according to the new zero level set. This gives rise to a fast and accurate level set algorithm.

The second method is a coarsening algorithm which ensures fine resolution of the surface in parts of the boundary with relatively high curvature, i.e., where it is needed most. These parts are typically the opening of the trench, its bottom, and places where microtrenching and side wall push back take place. At the same time the resolution is lowered where possible which reduces the demand on computational resources significantly.

In order to verify the models and simulator developed it was applied to the deposition of SiO_2 from TEOS in different Silicon trenches under different process conditions. All observed effects match well comparing the SEM pictures and the simulation results.



Figure 14: A simulation result showing initial, intermediate, and final surfaces. The resolution of the underlying level set grid was 80 · 160. The coarsening algorithm was applied twice, coalescing at most four surface elements into one, and the threshold angle was 3°. This result is nearly identical to the one achieved when no coarsening was applied.



Figure 15: The level set function after the last step of the simulation whose result is shown in Fig. 14. The active narrow band around the zero level set retains the signed distance function, whereas other grid points have not been updated.



Figure 16: The extended speed function in the narrow band in the last step of a simulation. In this simulation, no coarsening was performed, but apart from that it is identical to the one leading to Fig. 14.



Figure 17: The extended speed function in the narrow band in the last step of the simulation leading to Fig. 14. The coarsening can clearly be seen at the side walls of the trench.

3 High-Voltage Lateral Trench Gate SOI LDMOSFETs

We present a lateral trench gate SOI LDMOSFET which uses narrow trenches as channels. The lateral trench gate which allows the channel current to flow laterally on the trench side walls decreases its on-resistance, because it increases the current spreading area of the device. The specific on-resistance (R_{sp}) strongly depends on the trench depth. The R_{sp} of the suggested devices as a function of the lateral trench depth and the space between the trenches is studied. Three-dimensional numerical simulations with MINIMOS-NT have been performed to investigate the influence of device parameters on the R_{sp} and breakdown voltage. The improvement in the current handling capability of the suggested device is about 8.3% compared to the conventional SOI LDMOSFET.

3.1 Introduction

Smart power integrated circuits have become popular for automotive applications, consumer electronics, telecommunications, and industrial control. These ICs improve the reliability, reduce the volume and weight, and increase the efficiency of the system [19], [20]. Considerable effort has been spent on the development of smart power devices. SOI (Silicon on Insulator) lateral double diffused MOS transistors (LDMOSFETs) are increasingly used as output power devices in smart power applications. Advantages of SOI technology are the superior isolation, reduced parasitic capacitances and leakage currents, and the superior high temperature performance compared to the traditional junction isolation. These advantages allow monolithic integration of multiple power devices and low-voltage control circuitry on the same chip. The conventional SOI LDMOSFET has the channel regions on the surface. The channel is obtained by a double diffusion process. It has been shown that by proper choice of n-drift doping and length, optimal on-resistance can be achieved for a given breakdown voltage circuitry. New structures such as buried gate oxide devices [21], LUDMOSFETs [22], super-junction [23], and lateral trench gate [24] are proposed to improve the performance of the conventional lateral devices. Most of these structures are focused on the improvement of trade-off between the on-resistance and breakdown voltage.

We present a lateral trench gate SOI LDMOSFET which uses narrow trenches as channels. Contrary to the conventional vertical trench MOSFETs, the lateral trench gate is formed laterally on the side wall of a trench and the channel current flows to the lateral direction through the trench side walls. This gives an increased channel area compared to that of conventional SOI LDMOSFETs. Three-dimensional numerical simulations with MINIMOS-NT [25] have been performed to investigate the influence of device parameters on R_{sp} and breakdown voltage.

3.2 Device Structures and Operations

Fig. 18 and Fig. 19 show the schematic structures of a conventional LDMOSFET on SOI and a proposed lateral trench gate SOI LDMOSFET which are used for simulation of breakdown voltage and on-resistance, respectively. Generally, the breakdown voltage of the conventional SOI LDMOSFET is limited by the buried oxide thickness, SOI thickness, and drift layer length. Fig. 18 shows a cross-sectional view of a conventional n-channel SOI LDMOSFET designed for breakdown voltage of 100 V with an SOI thickness t_{soi} of 1.5 μ m, and with a buried oxide thickness t_{ox} of 1.0 μ m. The drift region of the device is doped according to the RESURF principle [26], [27] to achieve a maximum breakdown voltage. To obtain a better trade-off between the breakdown voltage and on-resistance a highly doped n⁺ buffer is added at the drain. As shown in Fig. 19, the proposed lateral trench gate SOI LDMOSFET has a similar structure as that of a conventional SOI LDMOSFET except that it has a trench gate on the side wall. Together with the

channel on the top of the SOI this gives an increased channel area, and an effective n-drift area (near the gate edge) which contribute current conduction during on-state is increased. From Fig. 19 it is clear that the channel current flows on the side wall of the trench. With the increased channel area and the effective n-drift area the reduction of the channel resistance can be achieved. The width, space, and depth of the lateral trench gate are 0.4 μ m, 1.1 μ m and from 0.5 to 1.5 μ m, respectively. Simulations are performed for the 100 V lateral trench gate SOI LDMOSFETs with an n-drift length $L_d = 5.5 \,\mu$ m and doping $N_D = 1.0 \times 10^{16} \text{ cm}^{-3}$. The other structure parameters are the same as that in Fig. 18.



Figure 18: Conventional LDMOSFET on SOI.



Figure 19: Proposed lateral trench gate SOI LDMOSFET and current flow iso-lines at $V_{\text{GS}} = 12$ V and $V_{\text{DS}} = 2.0$ V.

3.3 Simulation Results and Discussion

Optimum trade-off between breakdown voltage and R_{sp} has been the main issue of these devices. R_{sp} and breakdown voltage are inversely related to each other. Fig. 20 shows the potential distribution of the fully resurfed lateral trench gate SOI LDMOSFET at drain-source voltage $V_{DS} = 110$ V. It exhibits similar potential distribution as that of the conventional device, the lateral trench does not affect the RESURF condition. With the same breakdown voltage as the conventional device it helps to decrease the on-resistance by increasing the current spreading area at the channel region. Three-dimensional numerical

simulations with MINIMOS-NT have been performed to investigate the breakdown voltage, R_{sp} , and self-heating effects as a function of the lateral trench depth, and the space between the trenches.



Figure 20: Potential distribution of a lateral trench gate SOI LDMOSFET at $V_{\rm DS} = 110$ V.

3.3.1 Off-State Characteristics and Self-Heating

Fig. 21 shows the electric field of the conventional SOI LDMOSFET at $V_{\rm DS} = 110$ V, higher electric field can be seen at the drain and gate edge near the surface of the SOI. Fig. 22 shows the electric field of the lateral trench gate SOI LDMOSFET at $V_{\rm DS} = 110$ V. Contrary to the conventional RESURF SOI LDMOSFETs a higher electric field can be seen at the drain edge and middle of the lateral trench gate. With the n⁺ buffer at the drain the position of the electric field is moved toward extended drain edge (Fig. 23). At the gate the peak electric field moved from the surface to the middle of the bulk by the lateral trench gate, but it does not affect significantly the RESURF condition of the device. It helps to decrease the peak electric field near the gate edge on the top of the SOI.



Figure 21: Electric field of the conventional SOI LDMOSFET at $V_{DS} = 110$ V. A higher electric field can be seen at the drain and gate edge near the surface of the SOI.

3 HIGH-VOLTAGE LATERAL TRENCH GATE SOI LDMOSFETS



Figure 22: Electric field of the lateral trench gate SOI LDMOSFET at $V_{DS} = 110$ V. A higher electric field can be seen at the drain edge and middle of the lateral trench gate.



Figure 23: Comparison of the electric field in the lateral trench gate SOI LDMOSFET along the surface of the SOI and along the middle of the lateral trench gate.



Figure 24: Breakdown voltage versus lattice temperature of the lateral trench gate SOI LDMOSFET.



Figure 25: Comparison of the temperature by self-heating between the conventional and lateral trench gate SOI LDMOSFET near the surface of the SOI.

25

With the n-drift width of 5.5 μ m, the maximum breakdown voltage of the lateral trench gate structure is 117 V with $N_{\rm D} = 1.0 \times 10^{16}$ cm⁻³. The breakdown voltage of the conventional SOI LDMOSFET is 112 V with the same doping and structure parameters. Fig. 24 shows the leakage currents of SOI LDMOSFETs versus drain voltage as a function of the lattice temperature up to 573 K. The leakage current increases nearly exponentially with increasing temperature, because the space charge generation rate follows the intrinsic carrier density n_i . The increase of breakdown voltage is caused by the reduction of the mean free path of the carriers due to lattice scattering, requiring higher field for the carriers to initiate impact ionization. The temperature distribution inside a device due to self-heating is determined by the heat generation profile and the thermal conduction inside the SOI LDMOSFETs. In majority carrier devices such as MOSFETs, heat generation is mainly caused by Joule heating. It is proportional to the local resistances of the n-drift and channel region. But the channel resistance of the high-voltage devices (generally over 100 V) is not dominant in the on-resistance. Fig. 25 shows the temperature distributions near the SOI surface of the conventional and lateral trench gate SOI LDMOSFETs with an applied gate voltage V_{GS} = 12 V and a drain-source voltage $V_{\rm DS}$ = 2 V. The bottom of the devices is assumed to be isothermal at 300 K. Because of the lower on-resistance (by increasing the current) of the lateral trench gate structure a higher temperature is obtained at the n-drift region of the lateral trench gate SOI LDMOSFET.

3.3.2 On-State Characteristics

Fig. 26 and Table 1 show the results of the on-state characteristics of a conventional and a lateral trench gate SOI LDMOSFET. From this figure it becomes clear that the lateral trench gate SOI LDMOSFET has enhanced current handling capability. The on-state characteristics strongly depend on the trench depth and weakly depend on the space between the trenches. The specific on-resistance rapidly decreases with increasing the trench depth, but it does not strongly depend on the space between the trenches. With a trench depth of 0.5 μ m and space between the trenches of 0.5 μ m the $R_{\rm sp}$ has similar value as that of conventional device. With a trench depth of 1.5 μ m the $R_{\rm sp}$ of the device is 264 m Ω mm⁻² at $V_{\rm GS}$ = 12 V and $V_{\rm DS}$ = 0.5 V. It is about 8.3% smaller than the corresponding $R_{\rm sp}$ value of a conventional SOI LDMOSFET (about 288 m Ω mm⁻²).



Figure 26: Comparison the specific on-resistance among the conventional and lateral trench gate SOI LDMOSFETs at $V_{\text{GS}} = 12$ V and $V_{\text{DS}} = 0.5$ V.

 Table 2: DC performance comparison between the conventional and the lateral trench gate SOI LDMOS-FET.

	Conventional LDMOSFET on SOI	Lateral trench gate SOI LDMOSFET
$N_{ m D}, { m cm}^{-3}$	1.0×10^{16}	1.0×10^{16}
$L_{ m d}, \mu{ m m}$	5.5	5.5
$R_{ m sp},{ m m}\Omega{ m mm}^{-2}$	288	264
BV, V	112	117

3.4 Conclusion

A lateral trench gate LDMOSFET transistor on SOI is proposed. A lower specific on-resistance is obtained in the suggested structure compared to that of a conventional SOI LDMOSFET. With a lateral trench gate our three-dimensional simulations confirm that it is possible to get the best trade-off between the BV and $R_{\rm sp}$ of the LDMOSFET on SOI. The specific on-resistance strongly depends on the trench depth. It decreases with increasing the trench depth, but the space between the trenches dose not affect the onresistance. Simulations are performed for the 100 V lateral trench gate SOI LDMOSFETs with an n-drift length $L_{\rm d} = 5.5 \ \mu {\rm m}$ and doping $N_{\rm D} = 1.0 \times 10^{16} {\rm cm}^{-3}$. With a lateral trench depth of 1.5 $\ \mu {\rm m}$ a lower $R_{\rm sp}$ of 264 m $\Omega {\rm mm}^{-2}$ is obtained.

4 Control System of the Device Simulator MINIMOS-NT

State-of-the-art TCAD applications like the multi-dimensional device and circuit simulator MINIMOS-NT require a huge amount of information in addition to the device input data to control several different complex modules and tasks. This information is normally hierarchically structured containing arbitrary cross-relations and dependencies that include, e.g., material properties, circuit descriptions, models and model parameters, or simulation parameters. Therefore, the control system for such TCAD applications must be able to handle this data and to allow simulation control in an efficient and comfortable manner. To obtain a maximum of flexibility and controllability a new specialized object-oriented dynamic database is used.

4.1 Introduction

Device simulation has emerged as a flexible and powerful tool to aid design and optimization of semiconductor devices. State-of-the-art three-dimensional device simulators like MINIMOS-NT [28] are complex software tools and challenging to control. The simulated device is usually loaded from a file containing the geometric definition, the grid, and the input quantities defined on the grid. Nevertheless, this information is not sufficient. To perform a simulation additional information is needed to describe the device, its segments, and an eventually connected circuit. Moreover, adjustment of models, model parameters, material properties, circuit descriptions, simulation modes, iteration schemes, or input/output definitions must be possible. Thus, a sophisticated control system is required to allow control of each part of the simulator.

Nevertheless, even for such complex control systems the user-interface must be easy to learn and the user must be able to set up the specification files to describe a simulation in a straight forward and flexible way. The types of the additional information needed for device simulation are usually manifold:

- Values are the simplest kind of information. They may be, e.g., model parameters, quantities, contact values, limits, or just names and strings.
- Expressions are mandatory to describe dependencies between different parameters. These expressions may be mathematical formulas or logical relations and conditions.
- Sequences describe the order in which a given set of elements is processed.
- Hierarchies map the structures of hierarchical information. Hierarchies are used on the one hand side to describe relations between structures and on the other hand side to define the contents of a structure.

In the past years an object-oriented dynamic database called Input Deck database [29, 30] has been developed to meet the requirements of state-of-the-art TCAD applications. This database has been used to control several TCAD tools like the device simulator MINIMOS-NT, the Wafer State Library [31, 32], and the simulator FEDOS (Finite Element Diffusion and Oxidation Simulator) [33]. In this work we present the complex control-system of the device-simulator MINIMOS-NT.

4.2 The Input Deck Database

The Input Deck database [29, 30] is a new kind of database and works rather differently compared to common databases. The most important items stored are variables and sections. Variables queried by the

simulator are called keywords. Variables do not act like variables known from common programming languages. In fact, they represent states and act similar to cells known from spreadsheet tools. Variables contain expressions to describe dependencies to other variables. Sections hold an arbitrary set of variables and an arbitrary number of nested subsections to build any desired kind of hierarchies.

Expressions are evaluated at runtime when a value of a variable is queried by the simulator. Inside the database expressions are stored very efficiently as a special kind of forest [29] which enables both low memory consumption and a very fast evaluation of expressions.

The main advantage of the dynamic evaluation during runtime is that the values of all variables change virtually when the value of a variable they refer to is modified. Virtually means that recalculation of depending variables only happens when their values are queried. Thus, no calculation overhead occurs when values are changed by the simulator. Another feature of the Input Deck database and the control mechanism of MINIMOS-NT is that the simulator is allowed to change certain variables which are marked writable, thus feedback loops are possible (see Section 4.8).

The Input Deck uses a powerful inheritance scheme [29] called explicit-inheritance scheme to pass complex hierarchies of nested sections and their variables to other sections. This approach is used, e.g., for the material database of MINIMOS-NT (see Section 4.5), for the definition of circuits (see Section 4.6), and for the defaulting system of the simulator (see Section 4.4).

The Input Deck database has its own database description language, the Input Deck description language [28] (IDL). The syntax of the IDL has been defined similarly to that of the C++ programming language because C++ is one of the most popular programming languages. Nevertheless, the IDL is not a sequential programming language as it describes the entries of a database.

The Input Deck database offers an extensive application interface (API). The simulator can query variables and sections by their name or by means of iterators. Iterators are well suited to explore hierarchies and sequences. Application specific functions like the stepping functions (see Section 4.7) can be applied to extend the functionality of the database.

The default settings of MINIMOS-NT consist of approximately 2, 400 keywords and 1,000 sections defined in the MINIMOS-NT default files. Reading and parsing of these files requires 20ms CPU time on a 1GHz Pentium Linux computer. Due to inheritance approximately 30,000 keywords and about 8.000 sections exist. Evaluation of all keywords requires 1.5s.

4.3 The Simulation Flow

MINIMOS-NT is controlled by the Input Deck database in each phase of the simulation flow. Depending on the phase of the simulation the database performs different tasks. For instance, simulation modes, iteration schemes, or parameters for the solving process have to be chosen. Since state-of-the-art device simulators are very complex a multitude of decisions are imaginable for the user to influence the simulation flow.

Fig. 27 shows a schematic outline of the structure of the device simulator MINIMOS-NT. Each phase describes a complex process which must be controlled. The dashed arrow-lines indicate the direction of the communication with the Input Deck database.

At the beginning of the initialization phase the Input Deck database is initialized. After the initialization of the database, MINIMOS-NT is controlled by means of the database. The basic structures and all modules



Figure 27: Schematic structure of a device simulator.

and libraries are initialized, the device and circuit definitions and additional information like material properties (see Section 4.5) are loaded.

In the next step the device or the circuit and its embedded devices are loaded and analyzed. For each segment of each device the material is determined, the corresponding definitions are loaded from the database, and the input quantities are loaded. Contact definitions are read from the lnput Deck database. Depending on the simulation mode, the segment material, and the models to use which are set in the database the simulation quantities are initialized. Initial quantities like the interface distances or the net impurity concentration are calculated.

MINIMOS-NT provides a powerful stepping mechanism (see Section 4.7). This stepping allows to step arbitrary parameters and enables to run simulations for all permutations of a given set of parameters.

Within the main simulation loop three important phases are processed. In the preprocessing step the necessary quantities are calculated either from the initial state, the previous iteration, or the previous simulation point.

In the solving step the linear equation system is assembled. The iteration scheme and the solving procedure (see Section 4.9) are controlled by the Input Deck database. Runtime information on the state of the solving process is written back to the database which causes other expressions to change (see Section 4.8).

In the postprocessing step the output quantities are calculated from the computed solution. Moreover, several decisions are imaginable to influence the simulation loops (in Fig. 27 only the outer simulation loops are shown). Some of these approaches are depicted in Section 4.9.

4.4 Defaulting System

To provide default values for all possible keywords, MINIMOS-NT extensively uses the inheritance scheme of the Input Deck database. The default values are stored in separate sections. By convention, the names of these sections end with Defaults. For instance, the default iteration schemes are defined in the section IterateDefaults, the default settings for devices are stored in the section DeviceDefaults.

To use the default values the corresponding global default sections are inherited to the sections needed by the simulator, the standard sections of MINIMOS-NT. For instance, to use the standard settings for a device, the Device section is inherited from the DeviceDefaults section which holds all the default information. Also, those sections and the default inheritance schemes are predefined.

To modify the settings, the user can simply change the standard sections by locally overriding the default values. The Input Deck database assists the user by applying a checking mechanism when local modifications are performed in sections. Only those items defined in the parent sections which are inherited to the standard sections may be overloaded. Otherwise an error message is thrown to avoid misspelling of names. New items can be added but they have to be marked explicitly. If this checking mechanism is not desired, it can be turned off for each section.

4.5 Material Database

MINIMOS-NT uses a variety of physical models which are managed by a separate module of the simulator, the model server [34]. This model server allows the user to define customized models. Since the models to use depend on the type of the material, efficient material handling becomes an important issue. MINIMOS-NT uses only abstracted classes of the material, which are Semiconductor, Insulator, Conductor, and IdealConductor. The properties of the material classes are described via a model set, for instance the mobility or relaxation times of semiconductors. These models are defined as black boxes using a set of input and output parameters. Each black box is replaced by a certain implementation of this model which calculates the output values. Several implementations are available, each with the same set of model-parameters.

The material database manages all materials known by the simulator. The materials are hierarchically structured (see Fig. 28). To handle common material properties, real materials like Si or SiO_2 are inherited from abstract materials like semiconductor and insulator. Later on, the material properties of the derived material classes are extended and specialized.



Figure 28: Material Database.

Each material is represented by a section which provides the parameter values for all available physical models which are hierarchically structured. For each model class (e.g. the mass density or the band edge energy) and for each material (e.g. Si or SiGe) certain model instances can be chosen with so called model-specializer keywords.

For each geometric region in a device all physical models to use and their parameters must be specified in a special section. By inheriting the global material database the default settings are loaded which can be locally overridden.

The advantages of this hierarchical approach are:

- As MINIMOS-NT only deals with abstract material classes new materials can easily be added by inheriting them from the existing material classes.
- New models can be easily tested and calibrated by overriding the default values for these models.
- The material and model defaults can be easily customized by changing or adding new entries in the global material database.
- Maintenance of the default settings is much easier compared to hard coded default values in the simulator.

4 CONTROL SYSTEM OF THE DEVICE SIMULATOR MINIMOS-NT

4.6 Mixed-Mode

MINIMOS-NT has been equipped with circuit simulation capabilities [35]. The circuit may consist of an arbitrary number of compact and distributed devices. Default compact devices are, e.g., several kind of sources, resistances, conductors, capacitors, inductors, diodes, or transistors. Any number of distributed devices may be added to the circuit, each of them described by a separate section in the database. Instead of applying voltages or currents at the contacts as it is the case for single mode simulations the contacts are connected to nodes in the circuit. Thus, the semiconductor transport equations are solved together with the compact models in one circuit.

For the description of circuits the inheritance feature of the Input Deck is extensively used. The basic idea is that circuits consist of subcircuits which consist of subsubcircuits and so on. Each circuit is defined as a self-contained circuit and forms a black box. Black boxes and devices can again be used to form another circuit.

A circuit is described within a section. Its components may be subcircuits, devices, or compact devices. Each component is described by a section. The components of a circuit are usually inherited from the black boxes defined before. Variables inside a circuit definition form the contacts. There are two types of contacts: Inner contacts which are only used within the current circuit and outer contacts which form the input and output ports. To connect the components of a circuit, their outer contacts are assigned the names of the contacts of the circuit. The global circuit to be simulated is defined in the section called Circuit. This approach allows the definition of circuits of any complexity.

4.7 Stepping Functions

Stepping of keywords is also handled in a very flexible way. Nearly every keyword in the Input Deck database can be stepped by either providing minimum and maximum values, tables or lists of values, or values read from a data file. The latter feature is very useful when measured data has to be resimulated because the bias conditions can be directly fetched from the data file.

Stepping can be used to validate models as MINIMOS-NT allows physical models to be tested for a given set of parameters. Stepping these parameters enables to analyze models very effectively.

The stepped values are updated after each successful simulation of a given point. The stepping functions are implemented in MINIMOS-NT and made available in the Input Deck database as application specific functions. Thus, when the stepped values are changed user-defined feedback loops emerge.

4.8 Extern Section

In the so called Extern section several internal states of MINIMOS-NT are stored during simulation. Most of these states are parameters which show the progress of the solving procedure, e.g. the right hand side norm, the update norm, the CPU time, or the iteration counter. This information is needed to formulate the while and the failure condition for the iteration blocks which allows a user-defined feedback loop.

4 CONTROL SYSTEM OF THE DEVICE SIMULATOR MINIMOS-NT

4.9 Iteration Schemes

Due to the complex interaction between the coupled partial differential equations the idea of iteration schemes is relatively old. Instead of solving the fully coupled equation system by a Newton method, the equations are solved consecutively in suitable blocks until convergence is reached. A classic example is Gummel's algorithm [36], for other examples see e.g. [37, 38, 39]. Each of these schemes has its advantages under specific circumstances, e.g. the bias conditions and the type of the device. As it is impossible to implement all useful schemes, a different solution has been sought in MINIMOS-NT which makes heavy use of its powerful input language. Iteration schemes are defined to consist of iteration blocks. These blocks can be arbitrarily nested. For each block the user can specify:

- Which equation assembly models to use: This offers a flexible way to create suitable equation sets.
- Which quantities of the equation set should be used as solution variables.
- A convergence criterion: This can be formulated using information about the full or partial update norms, the residuum of the complete equation set or of a suitable subset of equations, the iteration counters, ore other parameters.
- A failure criterion: This is needed to trigger time-step and stepping control.
- An enter criterion: This allows to use the block under certain circumstances only, e.g. for the first time step or when the norm of the last iteration block was smaller than a certain value.
- The damping scheme to use: Depending on the equation type or the bias condition a different damping scheme or a different parameter set might be advantageous.

The iteration blocks are processed in order. Before each iteration the convergence condition which is explained above called while-condition and the failure criterion of the active block are tested. If the failure condition evaluates to true the execution is terminated with an error state. If not and the convergence condition evaluates to true another iteration will be performed otherwise the iteration block is terminated successfully and the next block is processed. The conditions can be arbitrary expressions. Normally the runtime information the simulator writes back to the database is used (see Section 4.9) to formulate the conditions. An iteration block does not need to specify an equation set in which case they are used as grouping constructs. With these features an individual iteration scheme can be tailored to solve even such complex problems as electro-thermal mixed-mode simulations [40].

4.10 Interactive Mode

In the past two years MINIMOS-NT has been extended to a fully multi-dimensional device simulator which is able to simulate arbitrarily shaped two- and three-dimensional structures. Due to the increased computational costs which occur especially in three-dimensional simulations it becomes necessary to control the simulation flow during simulation.

Therefore, MINIMOS-NT now provides an interactive mode which can be entered by pressing the control-sequence control-C during simulation. The user is prompted a menu and may change entries in the database directly using simple commands similar to Unix shell commands, e.g., 1s to list the contents of a section or set to set a variable. This new powerful mode of MINIMOS-NT enables, for instance, to change the parameters of the iteration scheme, to choose a different one, or to change the stepping behavior during runtime.

5 Three-Dimensional Analysis of a MAGFET at 300 K and 77 K

5.1 Introduction

A MAGFET is a MOSFET device with a split drain [41] designed in such a way that it is able to detect a magnetic field. When this magnetic field is applied perpendicular to the surface of the device, a current deflection appears as a result of the Lorentz force. If the MAGFET is a two-drain structure, then a differential current can be observed at those drains. This differential current is directly related to the sensitivity of the device, defined as

$$S = \frac{|I_{D1} - I_{D2}|}{(I_{D1} + I_{D2})|\vec{B}|}$$
(7)

where I_{D1} and I_{D2} are the currents at drain 1 and drain 2, and \vec{B} the magnetic field strength.

To improve the magnetic sensitivity, two approaches are possible. The first one is to adapt the geometry, so the (W/L) and separation between the two drains gives a maximum sensitivity, and the second one is to cool the device down to 77 K, which increases the mobility upon which the carrier deflection ΔZ (See Fig. 29) depends on



Figure 29: A view of the simulated MAGFET.

5.2 Discretization Scheme

In a series of papers by Wachutka *et al.* [42, 43] the current equation comprising the magnetic field in the isothermal approximation for electrons reads

$$\vec{J}_n = -\sigma_n (\nabla \phi_n) - \sigma_n \frac{1}{1 + (\mu_n^* \vec{B})^2} \{ \mu_n^* \vec{B} \times \nabla \phi_n \} - \sigma_n \frac{\mu_n^* \vec{B}}{1 + (\mu_n^* \vec{B})^2} \{ \mu_n^* \vec{B} \times (\vec{B} \times \nabla \phi_n) \}$$
(9)

(8)

where σ_n is the electric conductivity of the electrons, $\nabla \phi_n$ the gradient of the electron quasi-Fermi potential, μ_n^* the hall mobility related to the normal mobility as $\mu_n^* = r_n \mu_n$ with r_n the Hall scattering factor, and \vec{B} the magnetic field.

Along with the Poisson and continuity equations, a device under the presence of a magnetic field can be properly simulated under the driff- difussion approximation. The discretization of equation (9) was carried out following the general strategy depicted by Gajewski and Gärtner [44]. The vectorial product between the current density and the magnetic field is computed by considering a local coordinate system and the neighboring points. The discretization reads

$$J_B = \frac{s_k^T (I + N^T (\beta \beta^T + \beta_{\times}) N^{-T}) J_0}{1 + \beta^2}$$
(10)

where J_B are the projection currents along the meshing lines in the local coordinate system with the magnetic field, J_0 are the projection currents along the meshing lines in the local coordinate system without magnetic field, s_k the distance ratios, I the unitary matrix, β the dimensionless product between magnetic field and hall mobility, β_{\times} is a linear operator that combined with the $\beta\beta^T$ gives the matrix representation of a vectorial product, and N the matrix composed with the unitary vectors of the local coordinate system. This discretization scheme was successfully implemented in MINIMOS-NT.



Figure 30: Drain Currents for different gate voltages with and without magnetic field.

5.3 Simulated Structure

Fig. 29 depicts the actual simulated structure. It is an N-channel MAGFET with a substrate doping of 1×10^{15} cm⁻³, an oxide thickness of 60 nm. The device width is 100 μ m and the length is 125 μ m. The separation between the drains is 10 μ m. Fig. 30 shows the electrical behavior of the device with and without a magnetic field (50 mT), and a simulation at the same operating conditions (0.5 V drain to source voltage). The simulation results fit very well the experimental data. At 4.96 V, the magnetic field is turned



Figure 31: Differential Current at 300 K.

off and because of the hysteresis present in the magnetic field generator, the simulation does not reproduce this part of the measurements. The Hall scattering factor used for electrons was set to 1.15 [45].

The Lorentz force acts on the moving charges. So it is expected that the current distribution inside the MAGFET device changes when a magnetic field is applied.



Figure 32: Differential Current at 77 K.

5 THREE-DIMENSIONAL ANALYSIS OF A MAGFET AT 300 K AND 77 K

$$\Delta I_D = |I_{D1} - I_{D2}| = \frac{I_{D1} + I_{D2}}{L} \Delta Z = (I_{D1} + I_{D2})\mu |\vec{B}|$$
(11)

In order to *see* such a change, the MAGFET is simulated with a gate to source voltage of 4.95 V and a drain to source voltage of 1 V. The Hall scattering factor used for electrons was set to 1.15 [45]. Fig. 33, 34, and 35 show the current density in cuts at 30 μ m, 60 μ m, and 90 μ m from the source without magnetic field. It is clear from these figures that the current is equally distributed in both drains when no magnetic field is present.

A magnetic field of 40 mT normal to the surface and perpendicular to the channel current, flowing from the substrate up to the gate, is used in the simulations. At x=30 μ m and 60 μ m a current deflection is not easily visualized (Figs. 36 and 37). However, at 90 μ m (Fig. 38) the charge deflection is easily observed. These results confirms that, with a same device width, carrier deflection is more pronounced in larger devices. If the magnetic field direction is reversed, the electrons will pile up at the other drain side.

At 77 K the current density increases by a factor of 4 due to the increase of carrier mobility. This makes more difficult to visualize the carrier deflection (Figs. 39, 40, and 41). However, the simulated differential current at the contacts show an increase in the absolute value as seen from Figure 32. The carrier deflection ΔZ is directly dependent upon the carrier mobility. Therefore, the differential current increases at lower temperatures. The used Hall scattering factor was set to 2 [46].

5.4 Measurements

The detection of a magnetic field via a MAGFET is carried out, in the case of a two-drain structure, by means of measuring the differential current between both drains. Fig. 31 shows a comparison between the simulation results and the experimental data for room temperature. Fig. 32 shows the same differential current at 77 K.

At room temperature the simulation matchs perfectly the experimental data. At 77 K the simulation results are close to the measurements. This differential current is a function of the current magnitude, directly related to the carrier mobility, and the Hall scattering factor. Because the electrical characteristics of the MAGFET were matched before carrying out the simulation with magnetic field, it is clear that the Hall scattering factor has a great impact in the simulation.



Figure 33: Current Density (300 K, 0 mT) at x=30 μ m.



Figure 34: Current Density (300 K, 0 mT) at x=60 μ m.



Figure 35: Current Density (300 K, 0 mT) at x=90 μ m.



Figure 36: Current Density (300 K, 40 mT) at x=30 μ m.



Figure 37: Current Density (300 K, 40 mT) at x=60 μ m.



Figure 38: Current Density (300 K, 40 mT) at x=90 μ m.



Figure 39: Current Density (77 K, 40 mT) at x=30 μ m.



Figure 40: Current Density (77 K, 40 mT) at x=60 μ m.



Figure 41: Current Density (77 K, 40 mT) at x=90 μ m.

5.5 Conclusion

The analysis and simulation of a two-drain MAGFET have been successfully carried out with MINIMOS-NT in three dimensions. The involved vector product between the current density and the magnetic field has been computed by means of a linear combination of the different current projections along the meshing lines of the simulation grid. Using this discretization, a two-drain MAGFET structure has been simulated and the simulation results show a good agreement with the experimental data for two different temperatures.

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