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A. Gehring, C. Heitzinger, A. Hössinger, E. Ungersböck, W. Wessner, S. Selberherr



Institute for Microelectronics Technische Universität Wien Gusshausstrasse 27-29 A-1040 Wien, Austria

# Contents

1	Evaluation of ZrO <sub>2</sub> Gate Dielectrics for Advanced CMOS Devices		
	1.1	Introduction	1
	1.2	Device Preparation	1
	1.3	Modeling of Static Tunneling	2
	1.4	Modeling of Transient Tunneling	3
	1.5	Device Simulation	4
	1.6	Conclusion	4
2	Hig	h Quality Grids and its Application to a Trench Gate MOSFET	6
	2.1	Introduction	6
	2.2	The Grid Generation Method	6
	2.3	Grid Generation for Sample Structures	7
	2.4	Simulation of a TMOSFET	8
		2.4.1 Grid Generation	8
		2.4.2 Device Simulation	8
	2.5	Conclusion	8
3	A Si	moothing Algorithm for Cellular and Polygonal Datastructures	11
	3.1	Introduction	11
	3.2	Simulation Flow	11
	3.3	The Cellular Postprocessing Algorithm	12
		3.3.1 Triangular Surface Extraction	12
		3.3.2 Smoothing Stage	12
		3.3.3 Coarsening stage	14
		3.3.4 Simplification stage	14
	3.4	Conclusion	15

# CONTENTS

4	Simulation of Carrier Transport in Carbon Nanotube Field Effect		
	4.1	Introduction	16
	4.2	Device Modeling	16
	4.3	Transport Modeling	18
		4.3.1 Modeling of Tunneling Current	18
		4.3.2 Modeling of Thermionic Emission	19
	4.4	Results and Conclusion	19
5	Anis	sotropic Mesh Refinement for 3D Diffusion Simulation	21
5	Anis	Sotropic Mesh Refinement for 3D Diffusion Simulation	<b>21</b> 21
5	<b>Anis</b> 5.1 5.2	Sotropic Mesh Refinement for 3D Diffusion Simulation         Introduction         Anisotropic Refinement	<b>21</b> 21 21
5	<b>Anis</b> 5.1 5.2 5.3	Sotropic Mesh Refinement for 3D Diffusion Simulation         Introduction         Anisotropic Refinement         Diffusion	<ul> <li>21</li> <li>21</li> <li>21</li> <li>21</li> <li>23</li> </ul>
5	<b>Anis</b> 5.1 5.2 5.3 5.4	Sotropic Mesh Refinement for 3D Diffusion Simulation         Introduction         Anisotropic Refinement         Diffusion         Error Estimation	<ul> <li>21</li> <li>21</li> <li>21</li> <li>23</li> <li>23</li> </ul>
5	<b>Anis</b> 5.1 5.2 5.3 5.4 5.5	Sotropic Mesh Refinement for 3D Diffusion Simulation         Introduction         Anisotropic Refinement         Diffusion         Error Estimation         Example	<ul> <li>21</li> <li>21</li> <li>21</li> <li>23</li> <li>23</li> <li>24</li> </ul>

# **1** Evaluation of ZrO<sub>2</sub> Gate Dielectrics for Advanced CMOS Devices

We discuss modeling issues of ZrO<sub>2</sub> insulating layers fabricated by metal-organic chemical vapor deposition (MOCVD). Tunneling through such layers cannot be described within the established Tsu-Esaki model due to the presence of a strong trap-assisted tunneling component. Trap energy levels and concentrations can be extracted from the time constants of the measured trap charging and decharging processes. A trap concentration of  $4.5 \times 10^{18}$  cm<sup>-3</sup> with a trap energy level of  $1.3 \,\text{eV}$  below the  $\text{ZrO}_2$  conduction band edge was found for the considered layer. The parameters are used to simulate a 50 nm 'well-tempered' MOS-FET and the influence of the high- $\kappa$  dielectric on the threshold voltage was studied. Two counteracting effects are found: while the fringing fields from the drain contact reduce the threshold voltage, the presence of traps in the dielectric can lead to a strong increase of the threshold voltage.

### 1.1 Introduction

Gate dielectric stacks of high- $\kappa$  dielectrics have been proposed to enable the reduction of MOS-FET effective oxide thicknesses below 2 nm which is necessary to allow further device scaling. Several materials have been suggested to act as alternative dielectrics, such as  $Si_3N_4$ ,  $Al_2O_3$ ,  $Ta_2O_5$ ,  $HfO_2$ , or  $ZrO_2$ . Apart from thermodynamic stability, interface quality, and reliability, the dielectric permittivity and the barrier height are of utmost importance as they influence the gate current density through the layer [1]. Unfortunately, alternative dielectrics show a pronounced tradeoff between the permittivity and the barrier height. Simulations have shown that ZrO<sub>2</sub> promises good performance as compared to other materials [2]. In this paper the performance of ZrO<sub>2</sub> dielectric layers is studied by simulations based on static and transient measurements of ZrO<sub>2</sub> layers. Section 1.2 describes layer formation while Sections 1.3 and 1.4 are dedicated to the static and transient measurements. In Section 1.5 a 'welltempered' MOSFET is studied by means of device simulation using the parameters of the investigated layers, and Section 1.6 presents conclusions.

### **1.2 Device Preparation**

ZrO<sub>2</sub> pMOS capacitors have been fabricated by MOCVD on p-type (100) silicon wafers with an acceptor doping of  $1.5e18 \text{ cm}^{-3}$  and Al gate electrodes. A horizontal hot-wall reactor equipped with a bubbler system for metal-organic precursor delivery was employed, see Fig. 1. Zr(tfacac)4 was selected as precursor substance. It shows advanced stability towards hydrolysis compared to other possible precursor materials such as Zr(Ot-Bu)4 and has sufficient volatility for delivery at moderate bubbler temperatures. The already present Zr-O bonds in the precursor molecule also promote the formation of high quality thin films. The silicon substrates were subjected to a modified RCA-clean immediately prior to deposition including an HF dip to remove the native oxide and passivate the substrate surface. During the thin film deposition oxygen was supplied in addition to the argon carrier gas flow to support the decomposition of the precursor to zirconium oxide. All depositions were performed at a temperature of 450°C Gas flow rates were optimized in regard to the chemical composition of the product. Atmospheres of forming gas (10% hydrogen in nitrogen) and diluted oxygen (20% oxygen, 80% nitrogen) were employed as exemplary reducing (forming gas) and oxidizing (diluted oxygen) conditions in post-deposition annealing at 650°C [3].



Figure 1: MOCVD deposition scheme



Figure 2: Static gate current measurements of the  $ZrO_2$  layers compared with simulations.

The overall thicknesses of the dielectric layers has been evaluated by spectroscopic ellipsometry. Employing a relative permittivity of the high- $\kappa$  material itself of  $\kappa$ =18, which has been found for thicker films, the comparison of optical measurements and the results of C-V characterization implicates the presence of an interfacial layer with a permittivity in the range of 4 to 8. Table 1 summarizes the results of an evaluation of the thicknesses of the high- $\kappa$  films and interfacial layers. Also given is the effective oxide thickness  $t_{\rm eff} = t_{\rm int}\kappa_{\rm s}/\kappa_{\rm int} + t_{\rm hk}\kappa_{\rm s}/\kappa_{\rm hk}$ where  $t_{\rm int}$  and  $t_{\rm hk}$  are the thicknesses of the interface and the high- $\kappa$  layer, and  $\kappa_{int}$ ,  $\kappa_s$ , and  $\kappa_{\rm hk}$  the permittivities of the interface layer, silicon dioxide, and the high- $\kappa$  dielectric.

$t_{\rm phys}$	$t_{ m int}$	$t_{ m hk}$	$t_{\rm eff}$
6.9	0.75 - 2.0	6.15 – 4.9	2.0
12.7	0.3 – 1.0	12.4 – 11.7	3.0

 Table 1: Layer thicknesses of the deposited layers in nm.

### **1.3 Modeling of Static Tunneling**

The band diagram of  $ZrO_2$  dielectrics deposited on silicon shows a two-step energy barrier due to the presence of a thin layer of Zr-silicate at the interface between  $ZrO_2$  and silicon. We assume a band gap of the  $ZrO_2$ - and Zr-silicate layer of



Figure 3: Transient gate current of the dielectrics annealed under reducing and oxidizing conditions.

5.7 eV and 4.5 eV, respectively, with a conduction band offset of 1.5 eV for  $\text{ZrO}_2$  and 0.8 eV for the Zr-silicate [4]. For the calculation of tunneling current through the layer we used the the generalpurpose device simulator MINIMOS-NT and applied the Tsu-Esaki method, for which the tunnel current density is

$$J = \frac{4\pi m_{\rm ox} q \mathbf{k}_{\rm B} T}{h^3} \int_{\mathcal{E}_{\rm min}}^{\infty} TC(\mathcal{E}) N(\mathcal{E}) d\mathcal{E} \quad (1)$$

where  $m_{ox}$  is the effective electron mass in the oxide,  $\mathcal{E}_{min}$  the lower of the two conduction band edges next to the oxide,  $TC(\mathcal{E})$  the transmission coefficient, and  $N(\mathcal{E})$  the supply function which is calculated using Fermi-Dirac statistics. The transmission coefficient  $TC(\mathcal{E})$  can be calculated using several methods, such as the transfer-matrix or transmitting-boundary method. However, since the transfer-matrix method showed numerical instabilities we employed the transmitting-boundary method as described in [2].

Fig. 2 shows the measured gate current for the two dielectric layers, with the approximate shape of the energy barrier shown in the insets. As reference, the figure also shows the gate current for a 2 nm and a 3 nm SiO<sub>2</sub> layer (dotted lines). As expected, the measured current density is lower than for the SiO<sub>2</sub> counterparts. However, the tunnel current predicted by the Tsu-Esaki model for the ZrO<sub>2</sub> layer could not reproduce the measurements as it yielded tunneling currents orders of

magnitude lower than the measurements. We explain this failure of the Tsu-Esaki model by the presence of strong trap-assisted tunneling due to a high trap concentration in the dielectric layer. By assuming a simple Frenkel-Poole like conduction through the oxide layer

$$J = AF_{\rm ox} \exp\left(\frac{B\sqrt{F_{\rm ox}} - q\Phi_{\rm t}}{k_{\rm B}T}\right) \qquad (2)$$

where  $F_{\text{ox}}$  is the electric field in the oxide and Aand B were used as fitting parameters, the measurements could be reproduced (full lines). However, the values of A and B differ for positive and negative gate bias. That indicates that different conduction processes occur for accumulation and inversion. Note that in previous studies [5] tunneling through ZrO<sub>2</sub> layers fabricated by magnetron sputtering could be reproduced without considering trap-assisted tunneling.

### 1.4 Modeling of Transient Tunneling

To clarify the trap energy level and concentration, the step response of the MOS capacitors has been measured as shown in Fig. 3 for the 12.7 nm  $ZrO_2$  layer annealed in reducing conditions (forming gas) and the 6.9 nm layer annealed under oxidizing conditions. The gate voltage is turned off after being fixed at a value of 2.5 V and the resulting gate current is measured over time. The transient gate current exceeds the static gate current by orders of magnitude and decays very slowly. This behavior can be explained assuming slow states in the dielectric layer [6].

To account for this transient trap-assisted tunneling we use a model that has been presented in [7] and was implemented in MINIMOS-NT. Based on the rate equation for the concentration of occupied traps at position z and time t in the dielectric layer

$$\frac{df_{\rm T}(z,t)}{dt} =$$

$$= (1 - f_{\rm T}(z,t))\tau_{\rm c}^{-1}(z) - f_{\rm T}(z,t)\tau_{\rm e}^{-1}(z),$$
(3)

the trap occupancy follows an exponential decay

$$f_{\rm T}(z,t) = \frac{\tau_{\rm m}(z)}{\tau_{\rm c}(z)} + \left(f_{\rm T}(z,0) - \frac{\tau_{\rm m}(z)}{\tau_{\rm c}(z)}\right) \exp\left(-\frac{t}{\tau_{\rm m}(z)}\right).$$
(4)



Figure 4: Decay of the trap occupancy in the gate dielectric after removing a gate bias of 2.5 V

In these equations  $f_{\rm T}(z,t)$  is the trap occupancy function at position z and time t,  $\tau_{\rm m}^{-1} = \tau_{\rm c}^{-1} + \tau_{\rm e}^{-1}$ , and  $\tau_{\rm c}(z)$  and  $\tau_{\rm e}(z)$  are the time constants for capture and emission processes. They are calculated assuming inelastic phonon-assisted tunneling processes [8]. The free parameters of the model are the trap concentration, the trap energy level below the dielectric conduction band edge, the Huang-Rhys factor of the traps S, and the phonon energy  $\hbar\omega$ . Once the occupancy function is known, the transient tunnel current through one of the interfaces is

$$J(t) = q \int_0^{tox} \left( N_{\rm T}(z) \left( \tau_{\rm c}(z)^{-1} - f_{\rm T}(z,t) \tau_{\rm m}(z)^{-1} \right) \right) {\rm d}z.$$
(5)

The trap charge of occupied traps is calculated as the product of the local trap concentration  $N_{\rm T}(z)$ , the trap occupancy  $f_{\rm T}(z,t)$  and the trap charge state. The trap concentration was assumed to be constant in the dielectric layer. Only electron tunneling has been assumed, and the trap charge was self-consistently taken into account in the Poisson equation. Using this model, a trap energy level of 1.3 eV below the ZrO<sub>2</sub> conduction band edge, a trap concentration of  $4.5 \times 10^{18}$  cm<sup>-3</sup> and an energy loss of 1.5 eV have been found. For the dielectric layer annealed under oxidizing conditions



Figure 5: Transfer characteristics of the 'welltempered' MOSFET with SiO<sub>2</sub> and ZrO<sub>2</sub> dielectrics at  $V_{DS}$ =1.2V.

the trap concentration was reduced to  $4e17 \text{ cm}^{-3}$  to fit the measurements.

The model allows to study the location of occupied traps in the dielectric. Under inversion condition, traps near the substrate side of the dielectric layer are occupied while traps near the gate are empty. Fig. 4 shows that the trap occupancy has a Gaussian shape and shows a linear decay over time when the gate voltage is switched off.

### **1.5 Device Simulation**

To predict the performance of devices based on ZrO<sub>2</sub> dielectrics a well-tempered MOSFET as described in [9] with an effective channel length of 50 nm has been simulated. Effective gate oxide thicknesses of 2 nm and 3 nm SiO<sub>2</sub> and respective ZrO<sub>2</sub> layers have been considered. Fig. 5 show the transfer characteristics for a drain-source voltage of  $V_{\rm DS}$ =1.2 V on a linear and logarithmic scale for the different oxide thicknesses and dielectrics. It can be seen that the  $ZrO_2$  layer leads to considerably reduced threshold voltages. This reduction in the threshold voltage can be explained by the fringing fields from the drain contact which reduce the drain-source barrier, an effect which is especially pronounced for thicker layers. Fig. 6 depicts the conduction band edge in the channel for different gate-source voltages. It can be seen



Figure 6: Well-tempered MOSFET conduction band edge along the channel for  $SiO_2$ and  $ZrO_2$  dielectrics

that the barrier is slightly lower for the  $ZrO_2$  layer at  $V_{GS}$ =1.2 V, while there is a heavy barrier reduction for  $V_{GS}$ =0.1 V.

An additional topic of interest for high- $\kappa$  dielectrics is the influence of trapped charges in the high- $\kappa$  layer on the threshold voltage of the device. We used MINIMOS-NT to study this effect and defined the threshold voltage at a drain-source current of  $10 \,\mu$ A. The trap concentration in the ZrO<sub>2</sub> layer was increased from  $10^{15} \,\mathrm{cm}^{-3}$  to  $10^{19} \,\mathrm{cm}^{-3}$ , with full trap occupancy in the dielectric layer. It can be seen in Fig. 7 that the threshold voltage strongly increases with rising trap concentration. This effect is therefore contradictory to the increase of the threshold voltage due to fringing fields described above.

# 1.6 Conclusion

The tunneling current through  $ZrO_2$  layers deposited by MOCVD is mainly determined by trap-assisted tunneling which can be explained by a Frenkel-Poole tunneling model. The trap energy level and concentration can be estimated by measuring the step response of the MOS capacitors. The performance of a 'well-tempered' MOSFET using  $ZrO_2$  dielectrics was studied by means of device simulation. It was found that



**Figure 7:** Influence of the dielectric trap concentration on the MOSFET threshold voltage

there exist two controversial effects influencing the threshold voltage of the device. On the one hand, the high- $\kappa$  dielectric leads to a reduced threshold voltage especially for thicker layers. This effect is due to fringing fields from the drain contact. On the other hand, occupied traps in the dielectric layer increase the threshold voltage of the device. So, for low trap concentrations, the threshold voltage for the high- $\kappa$  device is lower than for the SiO<sub>2</sub> counterpart, while it is higher for high trap concentrations. This effect must be taken into account when modeling advanced MOS devices.

# **2** High Quality Grids and its Application to a Trench Gate MOSFET

The error of the numeric approximation of the semiconductor device equations particularly depends on the grid used for the discretization. Since the most interesting regions of the device are generally straightforward to identify, the method of choice is to use structurally aligned grids. Here we present an algorithm for generating structurally aligned grids including anisotropy and for producing grids whose resolution varies over several orders of magnitude. Furthermore the areas with increased resolution and the corresponding resolutions can be defined in a flexible manner and criteria on grid quality can be enforced.

The grid generation algorithm was applied to sample structures which highlight the features of this method. Furthermore we generated grids for the simulation of a high voltage trench gate MOS-FET. In order to resolve the junction regions accurately, four regions were defined where the grid was grown in several directions with varying resolutions. Finally device simulations performed by MINIMOS NT show current voltage characteristics and the threshold voltage.

### 2.1 Introduction

Generating structurally aligned grids is a crucial prerequisite for the accurate simulation of the electric behavior of semiconductor devices. The quality of the numeric approximation of the solution of the device equations by the finite element or the finite volume method particularly depends on the underlying mesh. In addition to aligning the meshes with the structures, it is desirable to be able to enforce quality criteria like the Delaunay criterion or the minimum angle criterion [10].

Here we present a new method to generate structurally aligned triangulations, including anisotropy if desired. The principal idea is to obtain a suitable, not connected set of edges by advancing a front through the simulation domain by a level set algorithm in the first step. In the second step these edges are used as the input for a specialized grid generator that enforces the quality criteria. Although a technique based on the level set method has been used for generating structurally aligned grids [11], that method cannot generate anisotropic grids and no condition concerning the quality of the grid, e.g., minimum angles or the Delaunay criterion, can be guaranteed. However, with our approach we can successfully carry out device simulations with the simulator MINIMOS NT [12] using the grids generated.

After the description of the grid generation algorithm, it is applied to two examples. The first example is a sample structure which highlights the critical parts near the corners. The second example stems from the simulation of a trench gate MOS-FET. Here several areas of refinement were chosen and the grid was generated to take the specific structure of the device and location of the junctions into account. This example emphasizes the applicability of the algorithm to real world examples.

Trench gate MOSFETS (TMOSFETS) are useful for power switching at high voltages [13–17]. They also provide advantages because of their geometric layout, i.e., because their inversion and accumulation channel regions are perpendicular to the wafer surface. Hence they enable to maximize the ratio of cell perimeter to area and thus to increase packing density. The TMOSFET considered is a 120V trench gate UMOS transistor (cf. Figure 10). After generating the structurally aligned grid, we present simulated characteristics of this TMOSFET in the final section.

### 2.2 The Grid Generation Method

In this section we discuss the algorithm devised for generating structurally aligned grids. The main idea is to advance one or more fronts through the simulation domain using a level set algorithm [18–20] and constant speed functions. For each moving front a certain number of boundaries are extracted. The number of these boundaries and the spacing between them can be arbitrarily defined and depends on the number of advancing level set steps and their time steps.



**Figure 8:** This figure shows a sample structure with angles of 270° and 90°. The set of edges was constructed from three moving boundaries: going downwards from the upper boundary and going upwards and downwards from a boundary in the lower part.

Clearly the spacing between the intermediate boundaries obtained by the level set algorithm will later determine the diameters of the triangles of the final grid.

Since the boundary segments of the intermediate boundaries obtained after surface extraction from the rectangular grid may be arbitrarily small, the boundary segments must be normalized. The segments are normalized by choosing points on the boundary that are equidistant when their distance is measured along the boundary. The normalized intermediate boundaries consist of straight lines which are the edges of the final grid to be respected in the second part of the algorithm.

This first part of the grid generation is highly customizable and anisotropy can be introduced here by choosing the spacing between the intermediate boundaries and the distance between points of the normalized boundary accordingly.

In the second part of the algorithm the set of edges constructed in the first part serve as input to the actual grid generator. The TRIANGLE program [21] was used in this work because of its robustness. After reworking the edges into the appropriate input format and running TRIANGLE, the output is translated into PIF files [12].

The benefits of this algorithm can be summarized as follows. The grid resolution is customizable and the areas of higher resolution can be chosen



**Figure 9:** A vertex with an outer angle of 90° of the grid in Figure 8 is magnified.

arbitrarily. The grid resolution may vary over several orders of magnitude. The algorithm can deal with arbitrary initial structures and an arbitrary number of starting fronts defining areas of high resolution. Anisotropy may be introduced by choosing appropriate parameters for the algorithm. At the same time quality criteria like the Delaunay criterion and requiring that all angles of the triangulation are larger than a certain minimum angle are enforced. It is important to note that the algorithm works reliably, since it is based on edges in contrast to just prescribing sets of points and hence directional information is preserved.

Compared to grid generation algorithms using iso-lines or iso-surfaces of solutions of the Poisson equation, the advantage of this algorithm is its flexibility. This is important, e.g., near the buried layers of SOI devices. The initial boundaries where the advancing fronts start, the prescribed number of intermediate boundaries and their spacing determine the properties of the final grid in a straightforward manner in contrast to the Poisson equation approach.

# 2.3 Grid Generation for Sample Structures

The grid in Figure 8 was generated by the above algorithm. The sample structure contains vertices with outer angles of  $90^{\circ}$  and  $270^{\circ}$  at the boundary where the grid is finest. Figure 9 shows a magnification of these interesting parts. In the examples we used a constant propagation speed for the first eight steps, starting at the upper boundary, and twice this value for the next seven steps.

Based on the edges constructed in the first step, the grid generator TRIANGLE [21] was used to obtain

a Delaunay triangulation. We demanded that the final triangulation contains no angle smaller than  $20^{\circ}$ . In these examples the grid resolution varies over several orders of magnitude and the critical areas near the corners are resolved without problems.

### 2.4 Simulation of a TMOSFET

The device structure of the trench gate UMOS transistor is shown in Figure 10 and its parameters in Table 2. Its trench depth is  $3\mu m$  and its gate oxide thickness is  $0.1\mu m$ . It is designed to achieve a forward blocking voltage of 120V.

### 2.4.1 Grid Generation

For the grid generation we used four boundaries following the three junctions (cf. Figure 10) and one in the *p*-region near the gate oxide. First, at the  $n^+-p$  junction we used three boundaries in each direction of the initial boundary following the junction with a distance of  $0.02\mu$ m between any two adjacent boundaries.

At the p-n junction we used one boundary above and below the initial boundary and a distance of  $0.02\mu$ m. At the n-n<sup>+</sup> junction in the lower part of the device we constructed two boundaries with a distance of  $0.5\mu$ m going downwards from the initial boundary following the junction. For the last prescribed edges we started at the right hand side of the p-region and moved to the left constructing three boundaries at a distance of  $0.005\mu$ m.

In the second step we used the TRIANGLE program requiring a minimum angle of  $25^{\circ}$  with these prescribed edges as input. The grid produced and two enlargements thereof are shown in Figure 11. The junction areas are resolved very finely as demanded.

### 2.4.2 Device Simulation

The device simulations were performed using MINIMOS NT [12]. Figure 13 shows typical on-state characteristics of the high voltage

Parameter	Value	
n drift doping	$1.5 \cdot 10^{15} \mathrm{cm}^{-3}$	
p well doping	$1\cdot10^{17}\mathrm{cm}^{-3}$	
p well	$\approx 1.4 \mu { m m}$	
$p^+$ buffer	$5 \cdot 10^{18} {\rm cm}^{-3}$	
$n^+$ source depth	$pprox 0.38 \mu { m m}$	
Gate oxide thickness	$0.1 \mu { m m}$	
Trench depth	$3 \mu { m m}$	
n drift length	$\approx 9.5 \mu \mathrm{m}$	

**Table 2:** The technological and geometrical parameters considered of the device.



Figure 10: Structure of the TMOSFET. The half cell pitch of the device is  $2.5\mu$ m and its *n* drift length is about  $9.5\mu$ m.

TMOSFET. The I-V curves of the figure show that good saturation currents behavior is obtained by increasing the drain voltage. Transfer characteristics are shown in Figure 14 for drain voltages of  $V_d = 0.1$ V and 0.5V. From this figure a threshold voltage  $V_T$  of 2.5V is obtained. It is important to note that the threshold voltage is independent of the drain voltage.

### 2.5 Conclusion

One of the main advantages of this method is the flexibility it provides. The resolution and



Figure 11: The grid generated for the device in Figure 10. Two enlargements are shown on the right hand side.



Figure 12: Enlargement of the upper grid shown in Figure 11.

anisotropy of the grid is customizable and the diameter of the triangles may vary over several orders of magnitude within one simulation domain. Compared to the approach of using iso-lines or iso-surfaces of solutions of the Poisson equation, our method allows to propagate



Figure 13: This plot shows the on-state characteristics of the vertical TMOSFET for gate voltages of 5V, 7V, and 10V.

several fronts through the device and thus to tailor the areas of high resolution precisely and in a straightforward manner. This is, e.g., especially important for the simulation of SOI devices, where high resolution is required in the vicinity of the buried layer.

Furthermore the algorithm is robust since the generation of the final triangulation is based on edges that have to be respected (and not on single points). Finally the grids generated satisfy the Delaunay criterion and the minimum angle criterion which ensures high grid quality with respect to numeric properties.

In a real world example the constructed mesh was used to obtain the on-state and transfer characteristics of a 120V trench gate MOSFET. The simulations of the TMOSFET show that the threshold voltage is independent of the drain voltage. The grid generated for the nontrivial geometry of this device increased the speed and accuracy of the simulations.



Figure 14: This figure shows the transfer characteristics of the high voltage TMOSFET for drain voltages of 0.1V and 0.5V.

# **3** A Smoothing Algorithm for Cellular and Polygonal Datastructures

When cellular based topography simulation is coupled with polygonal data structures it is necessary to extract a triangular representation of the surface of the simulated structure after a deposition or an etching process from the cellular discretization. In this work an advanced multistage cellular postprocessing algorithm is presented which is capable of generating a smooth triangulated surface with a relatively small number of triangles even for practical applications in semiconductor process simulation. All structural edges are maintained by the smoothing algorithm while almost all artificial edges are removed from the surface discretization.

### 3.1 Introduction

For the simulation of etching and deposition processes cellular algorithms [22] can be the method of choice due to their high robustness. However, they suffer from the fact that the cellular data structure is not directly compatible to polygonal based data structure used for the simulation of other semiconductor process steps like finite element simulators for annealing processes.

In [23] it has been demonstrated that this problem can be overcome by using a combination of polygonal and cellular data structures within the simulator. Roughly speaking the movement of the topography front is simulated using a cellular discretization, while the final simulation result is obtained by intersecting the generated process front with the input structure which is maintained in the polygonal data format.

Even if the method described in [23] seems to be straight forward on first glance, some critical problems have to be solved when using it within a simulation tool. The major problem is the generation of a smooth triangulated representation of the process front from the cellular discretization. According to our recent experience a multistage smoothing and simplification algorithm has turned out to be most successful to satisfy that purpose.

### **3.2** Simulation Flow



Figure 15: Simulation flow of TOPO3D

The algorithm proposed in this paper has been implemented into the three-dimensional etching and deposition simulator **TOPO3D** ([23], [24], [25]). Fig. 15 shows the simulation flow of the simulator. At the beginning the simulation structure is initialized. Than the actual simulation is performed. Therefore **TOPO3D** provides cellular algorithm based as well as polygonal algorithm based models. As a result both types of models generate a triangular discretization of the front of the topography process. The quality of this triangulation is improved by a postprocessing step before the front is intersected with the interfaces of the original structure. Afterwards a tetrahedrized representation of the merged structure is generated and separated into several single-connected regions. The regions are mapped to regions of the original structure and exposed regions are removed. With the mapping information a new consistent structure which maintains all information originally contained in the input file is generated.

In order to perform the cellular postprocessing a multistage smoothing and simplification algorithms has been integrated into **TOPO3D**, since it is very crucial to extract a smooth description of the process front to ensure the convergence of the succeeding volume meshing step. Furthermore the number of tetrahedral elements contained in the volume mesh is dramatically increased, if many artificial edges are contained in the triangular discretization of the process front.

# 3.3 The Cellular Postprocessing Algorithm

The postprocessing algorithm consists of four stages

- Surface extraction
- Smoothing
- Coarsening
- Simplification

### 3.3.1 Triangular Surface Extraction

The first stage of the algorithm is used to extract a triangulated representation of the process front. This is performed by applying a marching cube algorithm [26] to the cellular data. Thereby a set of triangles is extracted for each cell which is surrounded by at least one vacuum cell. The number of triangles and their shapes depend on the location of the neighboring vacuum cells. For a single test cube which is surrounded by eight cells 256 different cases of arrangement have to be distinguished by the marching cube algorithm. By extracting a set of triangles for each test cube which contains vacuum as well as material cells a contiguous surface is generated. Fig. 16 shows the triangulated topography front extracted by the marching cube algorithm. The edge length of the triangles in the marching cube discretization is of the order of the cell size. This means that the process front is made up of a huge number of triangles. Another problem is that even if the marching cube algorithm does minor smoothing by considering the surrounding of a test cube, the surface discretization still contains a lot of artificial edges. Therefore two additional postprocessing stages are required to get a smooth surface with as few as possible triangles.

Our investigations have raised that applying smoothing before coarsening is the best approach since it is only possible with a huge effort to avoid a degeneration of the surface triangulation if the coarsening stage is applied first.



Figure 16: Process front after marching cube discretization (332718 triangles)

### 3.3.2 Smoothing Stage

In order to get rid of most of the artificial edges all points connected to artificial edges are moved during the smoothing process. This is performed iteratively by applying small displacements to some point of the surface triangulation, as shown in Fig. 17. In order to decide whether a point should be moved mainly two criteria are checked (Fig. 18).



Figure 17: Illustration of the point offset mechanism in the smoothing stage

On the one hand side the curvature is analyzed. If the curvature is small the point is only surrounded by approximately iso-planar triangles and therefore needs not to be smoothed. Furthermore a typical property of a point on an artifical edge is that the curvature of at least one connected point has an opposite sign. This is why a point can be excluded from the smoothing process, if the curvature is smooth in the surrounding of the point. Worth mentioning is that due to performance reasons just an approximated curvature is used in the smoothing stage [27]. The approximate curvature  $C_{approx}$ is the average of the projection of all edges connected to a point onto the normal vector of the surface at that point.

$$C_{approx} = \frac{1}{N_{edges}} \cdot \sum_{edges} \vec{e} \cdot \vec{n_s} \tag{6}$$

 $\vec{e}$  is the vector of one edge and  $\vec{n_s}$  is the normal vector of the surface at the test point. It is approximately calculated as the sum of the normals of all triangles connected to the test point.

On the other hand side the distance of a point from its original position is analyzed. Since the maximal error of the cellular discretization is less than  $\frac{\sqrt{3}}{2}$  × the cellular resolution, the distance of the real surface from the discretized surface is smaller than the size of the discretization error. This defines a sphere of motion for each point around the original position of the point. If a point would leave its sphere of motion within one smoothing iteration, it is not moved.

Besides the selection of the points which have to moved during the smoothing process their direction of motion is a critical aspect. Within each iteration step the direction of motion of one point is calculated as the sum of the normals of all triangles connected to this point. The distance of motion is set to  $\frac{1}{10} \times$  the cellular resolution. If the distance of motion exceeds the length of one edge or the height of one triangle connected to the point, the motion is damped in order to inhibit a degeneration of the surface triangulation.



Figure 18: Illustration of the point selection method in the smoothing stage

The consistency of the surface triangulation is checked after all points have been moved, and point movements which have violated the consistency are reversed in a repairing step. Since the smoothing operation has to preserve the bounding box of the surface discretization, a special treatment is applied to the boundary points (point contained in the rectangular bounding box). Their freedom of motion is restricted to two dimensions or even one dimension, if the point is placed in the corner of the bounding box.

Fig. 19 shows the surface triangulation after applying smoothing steps while the number of points which can be moved decreases.



**Figure 19:** Process front after applying the smoothing stage (332718 triangles)

At the end of the smoothing stage the number of triangles is still very high. Therefore two stages are applied afterwards to significantly reduce the number of triangles.

### 3.3.3 Coarsening stage

During the coarsening stage triangles are removed by collapsing triangle edges to a single point. Due to performance reasons only two simple criteria are checked in the coarsening stage to determine whether an edge can be collapsed. On the one hand side there are edges which contain at least one iso-planar point and on the other hand side edges which are connected to two iso-linear edges. In the first case the edge is located within a larger plane, while in the second case the edge is part of a larger structural edge (Fig. 20).



Figure 20: Illustration of the edge removal algorithm in the coarsening stage

In general, when an edge is collapsed it is replaced by the point in the middle of the edge. But if one point of the collapsed edge is located at a structural edge, this point is chosen as the replacement point. Thereby a modification of the surface topology is avoided.

There are some cases where the collapsing of an edge results in a degeneration of the surface triangulation as shown in Fig. 21. Therefore the consistency of the surface triangulation is checked after each edge collapse operation and the edge collapse is reversed in case of a consistency violation.

Since the vast majority of triangles are located within iso-planar regions after the smoothing stage the coarsening stage is capable to significantly reduce the number of triangles, as shown in Fig. 22. Anyhow, there are still a lot of





unnecessary triangles especially within curved regions, which are eliminated by the following simplification stage.



Figure 22: Process front after applying the coarsening stage (24302 triangles)

### 3.3.4 Simplification stage

As well as the coarsening stage, the simplification stage uses the edge collapse algorithm to get rid of triangles. The same consistency checks and the same selection criteria for the replacement points are applied, but an alternative more sophisticated edge selection criterion as proposed in [28] is used.

The idea of the edge selection mechanism is to calculate the distance of any replacement point generated during the simplification process and to collapse an edge only if the distance does not exceed a certain limit. Within the simplification stage we again have chosen the cellular resolution as the limit for the selection algorithm since this is the minimal resolvable feature size of the cellular algorithm. Since the calculation of the distance of a replacement point from the original surface is extremely time consuming and requires to store two representations of the surface (the original surface and the simplified surface), an approximation for the distance is proposed in [28]. Using the  $4 \times 4$  distance matrix M derived for each point (Eq. 7), the distance d of the point from the surface can be calculated by (Eq. 8).

$$\mathbf{M} = \sum_{triangles} \left( \begin{pmatrix} \vec{n}_{tri} \\ \vec{n}_{tri} \cdot \vec{p} \end{pmatrix} \bigotimes \begin{pmatrix} \vec{n}_{tri} \\ \vec{n}_{tri} \cdot \vec{p} \end{pmatrix} \right)$$

$$d = \begin{pmatrix} \vec{p} \\ 1 \end{pmatrix} \cdot \mathbf{M} \cdot \begin{pmatrix} \vec{p} \\ 1 \end{pmatrix}$$
(8)

 $\vec{p}$  is the position vector of the point,  $\vec{n}_{tri}$  is the normal vector of a connected triangle. When a replacement point is added to the surface a distance matrix  $\mathbf{M_R}$  has to be calculated for the new point by summing up the distance matrices  $\mathbf{M_{E1}}$  and  $\mathbf{M_{E2}}$  of the corner points of the collapsed edge (Eq. 9).

$$\mathbf{M}_{\mathbf{R}} = \mathbf{M}_{\mathbf{E1}} + \mathbf{M}_{\mathbf{E2}} \tag{9}$$

While the distance is zero for points contained in the original surface the distance calculated by (Eq. 8) is greater than zero for a replacement point.

Although the selection mechanism used in the simplification stage would also select edges already eliminated by the coarsening stage, it is preferable to use both stages since the selection mechanism used in the simplification stage is more time and memory consuming. This is more critical as long as there is a large number of points in the surface triangulation. The surface discretization at the end of the simplification stage is shown in Fig. 23.

### 3.4 Conclusion

We present a multistage smoothing and coarsening algorithms for cellular based etching and deposition simulation, which has been implemented into the three-dimensional process simulator **TOPO3D**. It can significantly reduce the number of triangles in the surface triangulation and it removes almost all artificial



Figure 23: Process front after applying the simplification stage (710 triangles)

edges generated by the cellular discretization. Due to the small number of triangles in the surface also the number of the tetrahedral elements generated by the subsequent volume meshing step can be kept small.

16

# 4 Simulation of Carrier Transport in Carbon Nanotube Field Effect

We discuss models to describe carrier transport in axial and lateral type carbon nanotube field-effect transistors (CNT-FET). Operation is controlled by the electric field from the gate contact which can lead to strong band bending allowing carriers to tunnel through the interface barrier. We find that the difference between lateral and axial CNT-FETs is that in devices with axially aligned carbon nanotubes tunneling becomes negligible and transport can be modeled by means of thermionic emission. In lateral CNT-FETs tunneling dominates for which we present a model for the transmission coefficient using the WKB method and a non-parabolic dispersion relation. The simulated output and transfer characteristics show reasonable agreement with experimental data for both lateral and axial CNT-FET devices.

# 4.1 Introduction

Carbon nanotubes belong to the most promising candidates for future nanoelectronic applications. Experiments and theory have shown that the tubes can either be metals or semiconductors. Their electrical properties can rival, or even exceed, the best metals or semiconductors known. The electrical behavior is a consequence of the electronic band structure which depends on the exact position of the carbon atoms forming the tube. Semiconducting nanotubes can be used as active elements in field-effect transistor (FET) designs. While early devices showed poor device characteristics, improvements were achieved by using thinner dielectric films [29].

Recently models to describe the transport properties of carbon nanotubes have been developed [30, 31]. It was shown that carbon nanotubes act as unconventional Schottky barrier transistors. Transistor action is achieved by varying the contact resistance rather than the channel conductance. Transport through the nanotube is ballistic, so the current predominately depends on energy barriers between the source and drain contacts. Since the shape of this energy barrier and hence the operation of the transistor depends crucially on the device geometry, device simulation becomes necessary to predict device performance.

Simulation studies have shown that the shape of the contact electrodes has a high impact on the Schottky barriers and can be used for device optimization [32]. In this paper we compare two common CNT-FET geometries, namely transistors with laterally and axially aligned carbon nan-While lateral CNT-FETs have shown otubes. good performance with high  $I_{\rm on}/I_{\rm off}$  ratios [33], the manufacturability challenges are still signif-Transistors with axially aligned carbon icant. nanotubes [34] show worse device characteristics while being more suitable for large-scale integration. The considered device structures are presented in Section 4.2. In Section 4.3 models are discussed which allow the simulation of CNT-FETs in both the thermionic emission and the tunneling regime. Finally the simulations are compared to measurements of a lateral [31] and axial CNT-FET [34].

### 4.2 Device Modeling

The structure of axial and lateral CNT-FET devices is shown in Fig. 24. Lateral CNT-FETs resemble conventional MOSFET structures where the silicon channel is replaced by a single-wall or a highly defective multi-wall carbon nanotube connecting the source and drain contacts [32].

In axial CNT-FETs the gate contact lies above the drain contact from which it is separated by a thin gate oxide. While this structure has a much smaller footprint as compared to laterally aligned tubes, it has the shortcoming that the capacitive coupling between the gate and the tube is only weak. To get the potential distribution in such devices three-dimensional simulation is required.

However, since the principle of carrier transport in carbon nanotubes is still a subject of intense research and for the sake of simplicity we have used the two-dimensional general-purpose device simulator MINIMOS-NT to acquire the potential profile at the surface of the tube.



Figure 24: The lateral (a) and axial (b) carbon nanotube device structures

Since measured characteristics of most CNT-FETs resemble those of conventional p-type FETs the figures concentrate on hole transport and the valence band edge in the nanotube. Still the method is suited for electron transport as well. A band gap of  $0.6 \,\mathrm{eV}$  and undoped tubes have been assumed. The tube is covered in HfO<sub>2</sub> and connected to Al source and drain contacts. Fig. 25 shows the resulting valence band edge along the tube for the lateral and for the axial device at  $V_{\rm DS} = 0 \, {\rm V}$ . In case of lateral CNT-FETs the gate field heavily influences the valence band. Modulating the gate voltage from  $-0.25\,\mathrm{V}$  to  $-1.5\,\mathrm{V}$ , the valence band is shifted upwards towards the Fermi level of the



Figure 25: The valence band edge in a lateral CNT-FET at different gate voltages. The dashed line shows the band profile of an axial CNT-FET at  $V_{\rm G} = -10$  V



Figure 26: Valence band edge of a lateral CNT-FET for various drain voltages. One can observe suppression of the Schottky barrier at the drain contact

source and drain electrodes. This effectively reduces the energy barrier for holes. At modest gate voltages the carriers have to surmount a large energy barrier. Tunneling current is small and thermionic emission prevails. Increasing the gate voltage leads to a reduction of the energy barrier till tunneling dominates over thermionic emission. The threshold voltage  $VV_{th}$ of the device can be defined as the gate voltage necessary to shift the valence band up so that the tunneling current exceeds thermionic emission. The current saturates as soon as the second barrier is completely suppressed. Hence all electrons that can tunnel through the source barrier will contribute to the current.

The axial device, on the other hand, does not exhibit this behavior even for a gate voltage of  $-10 \,\mathrm{V}$ .

For a fixed gate voltage the band edge energies also depend on the drain voltage, as shown in Fig. 26 for a gate voltage of  $V_{\rm G} = -0.5$  V. At zero drain voltage the tunneling barrier is strong and thermionic emission dominates over tunneling. When  $V_{\rm DS}$  is decreased, the band edge at the drain side moves up and the effective barrier seen by holes coming from the source contact is reduced. This leads to an increase of tunneling current. At drain voltages below -0.375 V the drain tunneling barrier vanishes completely. The source energy barrier is fixed by the potential at the source contact and remains relatively insensitive to an increase of  $V_{\rm DS}$ . This gives rise to an output characteristics which is characterized by three distinguishable regions: an exponential region where thermionic emission dominates over tunneling, a linear region where tunneling prevails and the drain barrier decreases, and a saturation regime with a constant current.

For axial devices the gate field is blocked to a large amount by the underlying source contact (see Fig. 25). Even when applying relatively high gate voltages the effect on the barrier between source and drain is weak. The charge carriers have to surmount a potential barrier with two peaks at the contacts which is almost constant throughout the carbon nanotube. In this sense  $V_{\rm th}$  is never reached and thermionic emission will at all voltages dominate over tunneling. This results in output characteristics which resemble those of conventional Schottky barrier transistors.

### 4.3 Transport Modeling

Modeling of tunneling current is crucial for lateral CNT-FETs, while carrier transport in axial CNT-FETs can be described within the Schottky emission theory.

### 4.3.1 Modeling of Tunneling Current

To account for coherent transport in the nanotube the Landauer Büttiker formula has been implemented in MINIMOS-NT. The drain current through the nanotube is given by an integration in the energy domain [35]

$$I_{\rm d}(V_{\rm ds}) = \frac{4q}{h} \int dE (f_{\rm s}^0(E) - f_{\rm d}^0(E)) TC(E),$$
(10)

where TC is the transmission coefficient and  $f_{d,s}^0$  are the equilibrium Fermi functions at the source and drain contacts. The transport is ballistic, hence the current does neither depend on the length nor on the cross section of the carbon nanotube. The factor 4 in (10) stems from the twofold band and the twofold spin degeneracy.

In carbon nanotubes the dispersion relation cannot be described by a simple parabolic shape. Instead

$$E_{\pm n}(k) = \pm \frac{\sqrt{3}a\gamma_0}{2}\sqrt{\kappa(n)^2 + k^2}$$
(11)

has been used to approximate the band structure in the vicinity of the Fermi energy [36]. In this expression *a* denotes the lattice constant,  $\gamma_0$  is the transfer integral, and  $\kappa_n$  is related to the radius *R* of the nanotube via

$$\kappa_n = \frac{1}{R} \left( n - \frac{1}{3} \right). \tag{12}$$

Here, the value n denotes the band index. Accounting for this band structure, the transmission coefficient of carriers from band n can be estimated within the commonly used Wentzel Kramers Brillouin (WKB) approximation:

$$TC_n(E) = \exp\left(-2\int k(x)\,\mathrm{d}x\right)$$
 (13)

with the wave number

$$k = \frac{|\kappa_0|}{2} \sqrt{\left(\frac{\kappa_n}{\kappa_0}\right)^2 - \left(\frac{E - V(x)}{E_{\rm g}/2}\right)^2}.$$
 (14)

In this expression V(x) is the position dependent band edge along the tube. The band gap  $E_{\rm g}$  of single walled carbon nanotubes is related to the radius,  $E_{\rm g} = 0.9, {\rm eV}/2R$ , where R is given in nm.

Numerical integration is performed only within classical turning points. Note that the WKB method can only be used for slowly varying potentials and has the shortcoming that it fails at the classical turning points (E = V). Furthermore, the WKB method does not account for wavefunction interference effects which may occur due to the two separated barriers.

An alternative approach to calculate the transmission coefficient is to solve SCHRÖDINGER's equation with open boundary conditions in the whole nanotube. This has been done using the quantum transmitting boundary method (QTBM) [37]. This method has been preferred over transfer-matrix based schemes due to its better numerical stability. The resulting wavefunction at an energy of 0.1 eV is shown in



Figure 27: Potential along the nanotube at  $V_{ds}$ =-0.1 V (a) and the hole probability wavefunction (b)

Fig. 27. Exponential decay occurs in the barrier regions. Although no interference effects have been observed for long nanotubes, these affects can influence shorter devices.

### 4.3.2 Modeling of Thermionic Emission

The qualitative band diagram for axial CNT-FETs (see Fig. 25) motivates to describe the current density through the tube as emission over a Schottky barrier. Within the thermionic emission theory the current density can be written as [38]

$$J = C \exp\left(-\frac{q\Phi_{\rm B}}{k_{\rm B}T\gamma}\right) \cdot \left[\exp\left(\frac{qV_{\rm DS}}{k_{\rm B}T\gamma}\right) - 1\right],$$

where  $C = 4\pi m_{\rm eff} q k_{\rm B}^2 T^2 / h^3$  and the parameter  $\gamma$  has been introduced to describe the exponential slope of the IV-characteristics. To get a model which only depends on the gate-source and drainsource voltages, the values of  $\Phi_{\rm B}$  and  $\gamma$  have been fitted to measurement results with the gate-source voltage as parameter. This compact model has also been implemented in MINIMOS-NT, enabling the simulation of complete circuits.

### 4.4 Results and Conclusion

A lateral CNT-FET with a  $20 \text{ nm HfO}_2$  layer ( $\varepsilon_r = 11$ ) between the gate and the carbon

nanotube and a source drain separation of 300 nmhas been simulated. The single wall carbon nanotube has a radius of 0.7 nm and a bandgap of 0.6 eV. The subthreshold characteristics of this device for a drain voltage of  $V_{\text{DS}} = -1.2 \text{ V}$ is shown in Fig. 28. The experimental data [31] show reasonable agreement with the simulation results. The best fit is obtained if the radius of the tube is assumed to be 0.9 nm resulting in a band gap of 0.4 eV. However, we point out that the model has to be enhanced in order to take account for the linear increase of the drain current  $I_{\rm d}$  at high drain voltages of fully turned on devices.

Finally we used the thermionic emission model for the simulation of an axial CNT-FET. The conducting channel of this device is a highly defective multi-wall carbon tube with a diameter of approximately 20 nm, covered by SiO<sub>2</sub> and attached to source and drain contacts. The measured band gap of this device was 0.6 eV. Good agreement to experimental data [34] is found (see Fig. 29). Note that these measurements have been performed at liquid helium temperature. The low magnitude of the resulting drive current and the low  $I_{\rm on}/I_{\rm off}$  ratio makes the usage of axial devices as a replacement of MOSFET devices questionable.

We showed how transport through carbonnanotube devices can be understood as tunneling or thermionic emission depending on the device geometry. Lateral CNT-FETs allow good coupling between gate and tube, enabling output characteristics with good  $I_{\rm on}/I_{\rm off}$  ratios. Axial CNT-FETs can be described assuming thermionic emission. The presented models can be used to describe carrier transport in both types of carbon nanotubes.



**Figure 28:** Experimental data and simulation results for a lateral CNT-FET. Increasing the tube radius reduces the band gap and thus decreases the threshold voltage



Figure 29: Output characteristics of an axial multi-wall CNT-FET at 4.2 K compared to simulations assuming thermionic emission

# 5 Anisotropic Mesh Refinement for 3D Diffusion Simulation

We present a computational method for locally adapted conformal anisotropic tetrahedral mesh refinement. The element size is determined by an anisotropy function which is governed by an error estimation driven ruler according to an adjustable maximum error. Anisotropic structures are taken into account to reduce the amount of elements compared to strict isotropic refinement. The spatial resolution in three-dimensional unstructured tetrahedral meshes for diffusion simulation can be dynamically increased.

### 5.1 Introduction

In the numerical solution of practical problems of physics engineering such as semiconductor process and device simulation, one often encounters the difficulty that the overall accuracy of the numerical approximation is deteriorated by local exaltations. An obvious remedy is to refine the discretization in the critical regions [39].



The question then is how to identify these regions and how to obtain a good balance between the refined and unrefined regions such that the overall accuracy is optimal. These considerations clearly show the need for error estimators which can be extracted a posteriori from the computed numerical solution and the given data of the problem. The error should be local and should yield reliable upper and lower bounds. The global upper bounds are sufficient to obtain a numerical solution with an accuracy below a prescribed tolerance. Local lower bounds are necessary to ensure that the grid is correctly refined according to an adjustable error using a (nearly) minimal number of grid-points. As shown in Fig. 30, during the calculation of a time step a combination of error estimation and refinement mechanism is necessary to deliver higher accuracy, if needed, by increasing the spatial resolution.

### 5.2 Anisotropic Refinement

Using strict isotropic meshes for threedimensional process simulation is not practicable [40]. The need of calculation time and the limitation of memory tend to result in anisotropic adapted meshes which are more manageable. In [41], e.g., the element shapes are controlled by a tensor-based metric space for representing mesh anisotropy over the domain.

Anisotropy is defined by three orthogonal principal directions and an aspect ratio in each direction. The three principal directions are represented by three unit vectors  $\vec{\xi}, \vec{\eta}$ , and  $\vec{\zeta}$ , and in these directions the amounts of stretching of a mesh element are represented by three scalar values  $\lambda_{\xi}, \lambda_{\eta}, \lambda_{\zeta}$ , respectively. Using  $(\vec{\xi}, \vec{\eta}, \vec{\zeta})$  and  $(\lambda_{\xi}, \lambda_{\eta}, \lambda_{\zeta})$  we define two matrices **R** and **S** by

$$\mathbf{R} := \begin{pmatrix} \xi_x & \eta_x & \zeta_x \\ \xi_y & \eta_y & \zeta_y \\ \xi_z & \eta_z & \zeta_z \end{pmatrix} \text{ and } \mathbf{S} := \begin{pmatrix} \lambda_{\xi} & 0 & 0 \\ 0 & \lambda_{\eta} & 0 \\ 0 & 0 & \lambda_{\zeta} \end{pmatrix}.$$
(15)

By combining matrices  $\mathbf{R}$  and  $\mathbf{S}$ , we obtain a  $3 \times 3$  positive definite matrix  $\mathbf{M}$ 

Figure 30: Simulation procedure

$$\mathbf{M} := \mathbf{R}\mathbf{S}\mathbf{R}^T \tag{16}$$

that describes the three-dimensional anisotropy.

The basic refinement step in our algorithm is tetrahedral bisection which is well investigated by, e.g. Arnold [42]. When bisecting a tetrahedron, a particular edge – called the *refinement edge* – is selected and split into two edges by a new vertex. As new tetrahedra are constructed by refinement, their refinement edges must be selected carefully to take anisotropy into account without producing degenerately shaped elements. In order to identify which edge should be cut, the length of the edges is calculated in a metric space [43].

A set S with a global distance function (the metric g) which for every two points x, y in S gives the distance between them as a nonnegative real number g(x, y) is called the metric space [44]. The distance function must also satisfy

$$g(x, y) = 0 \Leftrightarrow x = y$$
  

$$g(x, y) = g(y, x)$$
  

$$g(x, y) + g(y, z) \ge g(x, z).$$
(17)

In our implementation this metric specially varies over the domain, and hence the length of an edge depends on its position. In case the *anisotropic length* is greater than an adjustable value, the edge is cut in the middle.

Calculating the length of an edge in a metric space can be seen as calculating a line integral. In general an arc length  $\ell_C$  is defined as the length along a curve  $C: \ell_C = \int_C ds$ . M as defined in (16) represents a metric when viewed as positive definite tensor  $\mathbf{M} = \mathbf{M}(x, y, z)$  over the entire domain. Roughly spoken, the metric tensor  $\mathbf{m}_{ij}$  shows how to compute the distance between any two points in a given space. Its components can be viewed as multiplication factors which must be placed in front of the differential displacements  $dx_i$  in a generalized Pythagorean theorem  $ds^2 = g_{11}dx_1^2 + g_{12}dx_1dx_2 + g_{22}dx_2^2 + \cdots$ .

The length of a line segment PQ in a metric space is calculated by [45]

$$\ell_{PQ} = \int_0^1 \sqrt{PQ^T \cdot \mathbf{M}(P + tPQ) \cdot PQ} \, dt \tag{18}$$

where  $\mathbf{M}(P + tPQ)$  is the metric at point  $P + tPQ, t \in [0, 1]$ .

The basic idea of our refinement algorithm is to use the gradient field of the solution and the given data of the scalar diffusion problem as *stretching direction* of the anisotropy metric. The gradient  $\nabla C = \operatorname{grad}(C)$  of a scalar field C = C(x, y, z) in Cartesian coordinates is given by

$$\nabla C = \frac{\partial C(x, y, z)}{\partial x}\vec{i} + \frac{\partial C(x, y, z)}{\partial y}\vec{j} + \frac{\partial C(x, y, z)}{\partial z}\vec{k}.$$
(19)

The gradient of a tetrahedral discretization can be calculated by using linear basis functions [46] applied to the three-dimensional unit simplex T. The coordinate transformation

$$x = x_1 + (x_2 - x_1)\xi + (x_3 - x_1)\eta + (x_4 - x_1)\zeta$$
  

$$y = y_1 + (y_2 - y_1)\xi + (y_3 - y_1)\eta + (y_4 - y_1)\zeta$$
  

$$z = z_1 + (z_2 - z_1)\xi + (z_3 - z_1)\eta + (z_4 - z_1)\zeta$$
  
(20)

allows to map an arbitrary tetrahedron at global coordinates (x, y, z) to the unit simplex T (cf. Fig. 31) with local element coordinates  $(\xi, \eta, \zeta)$ . In matrix notation this can be written as

$$\vec{r} - \vec{r_1} = \mathbf{J} \cdot \vec{\delta},\tag{21}$$

where  $\vec{r} = (x, y, z)^T$ ,  $\vec{r_1} = (x_1, y_1, z_1)$ ,  $\vec{\delta} = (\xi, \eta, \zeta)^T$ , and **J** denotes the Jacobian

$$\mathbf{J} = \begin{pmatrix} x_2 - x_1 & x_3 - x_1 & x_4 - x_1 \\ y_2 - y_1 & y_3 - y_1 & y_4 - y_1 \\ z_2 - z_1 & z_3 - z_1 & z_4 - z_1 \end{pmatrix}.$$
 (22)

Using linear basis functions on the threedimensional unit simplex, which are given by [47]

$$N_{1} = 1 - \xi - \eta - \zeta$$

$$N_{2} = \xi$$

$$N_{3} = \eta$$

$$N_{4} = \zeta,$$

$$(23)$$

allows a linear approximation over the element in the form

$$C(\xi, \eta, \zeta) = \sum_{k=1}^{4} N_k(\xi, \eta, \zeta) C_k,$$
 (24)

where  $C_k$  denotes the scalar value of the solution on vertex k of the three-dimensional unit simplex

### T.

Applying (19) to the linear approximation, given by (25), results in

$$\nabla C(\xi, \eta, \zeta) = \begin{pmatrix} -C_1 + C_2 \\ -C_1 + C_3 \\ -C_1 + C_4 \end{pmatrix}$$
(25)

for the gradient of the discretization. The gradient is constant over an element and represents the anisotropic stretching direction.



Figure 31: Coordinates transformation.

### 5.3 Diffusion

Diffusion is the transport of matter caused by a gradient of the chemical potential. This mechanism is responsible for the redistribution of dopant atoms within a semiconductor during a high-temperature processing step. The underlying ideas can be categorized into two major approaches, namely, the continuum theory of Fick's diffusion equation and the atomistic theory [48]. We are using the continuum theory approach which describes the diffusion phenomenon by the diffusion law:

$$\vec{J} = -D \cdot \operatorname{grad}(C) \tag{26}$$

 $\vec{J}$  denotes the diffusion flux, D is the *diffusion co-efficient* or *diffusivity*, and C is the concentration of the dopant atoms.

In general, the diffusion models used in semiconductor process simulation are strongly nonlinear, because the diffusion coefficients depend, e.g., on the impurity and point defects [49]. These dependences also couple the equations for multiple impurities and point defects. Additionally, more complex models include chemical reactions and contain convection terms. However, for better understanding of our refinement method we use the linear parabolic diffusion problem which is given by (27).

### 5.4 Error Estimation

Since the vector field  $\nabla C(\xi, \eta, \zeta)$  (26) is piecewise constant, it is obvious that strong variations of the gradient from one element to an adjacent one yield an approximation error when compared to the proper continuous gradient field. This gradient approximation error causes a diffusion flux error which gives rise to a violation of the law of mass conservation.

According to the discussion of a posteriori gradient recovery error estimation by Ainsworth [50], the basic idea is to estimate the error per cell by integrating the gradient jump of the solution along the faces of each cell.

For the elliptic problem  $-\nabla(a(x) \triangle u) = f$  with Dirichlet boundary conditions, an error estimator for two dimensional triangulations, proposed by Kelly et al. [51], is

$$\eta_K^2 = \frac{h}{24} \int_{\partial K} \left[ \frac{\partial u_h}{\partial n} \right]^2 d\sigma, \qquad (27)$$

where h denotes the longest edge of the triangle K and  $[\omega]_K(x) := \lim_{\epsilon \to 0+} \omega(x + \epsilon \nu_K) - \lim_{\epsilon \to 0+} \omega(x - \epsilon \nu_K), x \in K$ , is the jump of  $\omega$  over the triangle K.

Picking up this idea for elliptic problems we use a modification for the linear parabolic diffusion problem (27). In our implementation the error estimation is performed by calculating the gradient field of the solution in every element over the domain, where only a small variation in adjacent vectors is allowed. As shown in Fig. 32, to evaluate the variation, the maximum of the vector norm of the difference

$$\ell_d = \|\vec{E}\|_2 = \sqrt{(\vec{G}_1 - \vec{G}_2) \cdot (\vec{G}_1 - \vec{G}_2)} \quad (28)$$

of adjacent gradient vectors  $G_1$  and  $G_2$  is used. For this procedure only the face-to-face



Figure 32: Error of adjacent gradient vectors.

relationship of every tetrahedron is used. So in this sense every tetrahedron has as maximum only four neighbors. The length of the difference vector  $\ell_d$  can be seen as measure for the anisotropic *stretching values* (15). The refinement anisotropy is now fully described by the stretching direction (the gradient field) and the stretching values (length of the difference vectors).

According to Section 5.1 an adjustable lower bound for the whole discretized domain is necessary to identify which regions should be refined. As shown in Fig. 30 after error estimation critical elements are marked for the refinement procedure if  $\ell_d$  (29) is greater than the prescribed lower error bound. The refinement procedure utilizes the local element gradient as anisotropy direction in combination with (29) to identify which edge of the marked tetrahedron should be used for the new vertex.

### 5.5 Example

To see the essential impact of our refinement strategy we use a three-dimensional test structure. The underlying initial mesh (see Fig. 33) is a coarse fairly isotropic mesh which carries a dopant profile. The white area can be seen as mask, where at the upturn open part of the structure the diffusion dose  $N_d$  is kept constant. For an one-dimensional case this can be written as

$$N_d = \int_0^\infty C(x,t)dx = \text{const.}$$
(29)

This diffusion condition is referred to as *drive-in diffusion* [52]. Note that the gradient of the concentration C vanishes at the surface,

 $\nabla C = \text{grad}(C) = 0$ , and so does the diffusion flux  $\vec{J}$  (27). The dopant concentration has its maximum therfore at the step of the structure.

Fig. 34 shows the corresponding gradient field and iso-surfaces of the dopant concentration. The gradient vectors are calculated over every tetrahedron according to (26). The orientation of the gradient is turned towards higher concentration values and perpendicular to the iso-surfaces of the dopant concentration. The gradient field varies much stronger along the short edges of the structure.

To increase the accuracy, refinement is needed only in the relevant area around the step in the structure. The anisotropy should care of the variations of the vector field along the short edge of the structure and should keep the edge length along the long side.

As shown in Fig. 35, after refinement the edge length along the long side of the cuboid does not change much, but on the short side a much higher mesh density arises and the resolution can be increased. To find a good balance between refined and unrefined regions under consideration of element shapes its mandatory also to refine elements which belong to the white mask structure. Bisecting a tetrahedron by inserting a new vertex on an edge yields always the division of the whole patch. Well behaved element shapes demand a smooth transition between refined and unrefined regions. The algorithm produces a quite local refinement under consideration of a desired anisotropic behavior.

### 5.6 Conclusion

We present a computational method for anisotropic mesh refinement. The refinement method is based on bisecting tetrahedrons by inserting a new vertex on a particular edge. This particular edge is selected according to a specific metric which is governed by the gradient field of the numerical solution of the linear diffusion problem and the given initial data. The refinement



Figure 33: Dopant concentration (initial mesh).



Figure 34: Gradient field and iso-surfaces (initial mesh).

is driven by an a posteriori error estimator which identifies these regions where a higher spatial resolution is needed. The algorithm shows a local behavior and avoids ill shaped elements during refinement. The resulting mesh matches the dopant profile appropriately and a good resolution of the gradient field is expected. Therefore this refinement method is also a good choice for complex dynamic diffusion problems.



Figure 35: Refined anisotropic mesh.

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