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1 Evolution of Current Transport Models for Engineering Applications

An overview of models for the simulation of current transport in micro- and nanoelectronic devices within the framework of TCAD applications is presented. Starting from macroscopic transport models, currently discussed enhancements are specifically addressed. This comprises the inclusion of higher-order moments into the transport models, the incorporation of quantum correction and tunneling models up to dedicated quantum-mechanical simulators, and mixed approaches which are able to account for both, quantum interference and scattering. Specific TCAD requirements are discussed from an engineer's perspective and an outlook on future research directions is given.

1.1 Introduction

The continuous minimum feature size reduction of microelectronic devices, institutionalized by the ITRS roadmap [1], has been partly enabled by the support of sophisticated Technology CAD (TCAD) tools. These tools promise to assist process and device engineers during all stages of development, ranging from process simulation to device and circuit simulation. Today, device engineers face the challenge to move from the microelectronic feature scale in the mid-90's, with typical MOSFET gate lengths just entering the submicron region, to the realm of nanoelectronics with 90 nm gate length devices in production and 6 nm gate length transistors fabricated in research labs [2]. The continuum approximation, already questioned in the mid-1990's, has to be abandoned in this regime, and different approaches for the simulation of devices in the nanometer regime have been proposed.

In general, the inaccuracies of presently applied semiclassical macroscopic transport models are due to non-local effects [3], either caused by classical or quantum-mechanical non-localities. Classical non-localities arise because the distribution of electrons in very small devices does not depend on local quantities alone. Quantum-mechanical non-localities occur due to the wave nature of electrons and the occurrence of quantization, either due to high electric fields as in the inversion layer of a MOSFET, or due to the geometry as in ultrasmall double-gate or FinFET devices.

Figure 1 depicts the hierarchy of models which are currently used for the description of current transport. Semiclassical transport models rely on classical states characterized by a distribution function which is governed by the Boltzmann transport equation. In Section 1.2 we will give a review of the evolution of current semiclassical transport models, and describe recent results with regard to higher-order transport models. Quantum ballistic transport is based on pure states described by a wave function, the evolution of which follows SCHRÖDINGER's equation. These approaches are mainly used for the simulation of closed systems, such as quantum corrections in the inversion layer of MOSFETs. In Section 1.3, these quantum-ballistic transport approaches will be described. Finally, quantum transport theory deals with mixed states. There exist different formulations, which can be based on the Dyson equation, the Liouville/von Neumann equation, or the Wigner transport equation. Section 1.4 deals with quantum transport characterized by both scattering and quantization. A conclusion will summarize the main findings and give directions for future research.

1.2 Semiclassical Transport

In the early days of semiconductor technology, the electrical characteristics of semiconductor devices could be estimated based on simple analytic compact models, employing a variety of simplifying approximations but capturing the basic physical principles of carrier transport. These models were based on the drift-diffusion (DD) formalism, where the current in the device is governed by the electric field and the concentration gradients alone. Based on the ground-breaking work of Scharfetter and Gummel [4], who first proposed a robust discretization scheme for the drift-diffusion equations, the numerical simulation of semiconductor devices was enabled.



Figure 1: Hierarchy of transport equations in semiconductor current transport modeling.

Computer programs such as Minimos [5] and Pisces [6] have been developed and played a pioneering role in the deeper understanding of current transport for engineering purposes and in the development of miniaturized devices. For the first time, it was possible to provide insight into the functioning of semiconductor devices by means of the distribution of internal device quantities, instead of global quantities such as current-voltage characteristics. Since then, numerous transport models of increasing complexity have been proposed. All models are coupled to the POISSON equation

$$\nabla \cdot (\kappa \nabla \phi) = \rho(\phi) , \qquad \rho(\phi) = q(n - p - C)$$
 (1)

where ϕ denotes the electrostatic potential and κ the dielectric permittivity. The question of current transport basically reduces to the self-consistent modeling of the non-linear charge density $\rho(\phi)$ in (18), which includes the electron and hole concentration, the net concentration of impurities, and other charges such as ionized traps.

Neglecting the quantum-mechanical nature of electrons, carrier transport in a device is described by BOLTZMANN's transport equation, a seven-dimensional integro-differential equation in phase space [7]

$$\frac{\partial f}{\partial t} + \mathbf{v} \cdot \nabla_r f - \frac{q\mathbf{E}}{\hbar} \cdot \nabla_{\mathbf{k}} f = \left(\frac{\partial f}{\partial t}\right)_{\text{coll}} .$$
 (2)

Here, $f(\mathbf{r}, \mathbf{k}, t)$ is the distribution of carriers in space (**r**), momentum ($\hbar \mathbf{k}$), and time. On the right-hand side stands the collision operator which describes scattering of particles due to phonons, impurities, interfaces, or other scattering sources.

However, for realistic structures, the direct solution of this equation is computationally prohibitive. It is rather solved by approximate means applying the method of moments or using Monte Carlo methods. In the method of moments each term of (2) is multiplied with a weight function and integrated over **k**-space. This yields a set of differential equations in the (\mathbf{r} ,t)-space. The moments of the distribution function are defined as

$$\langle \Phi \rangle = \frac{1}{4\pi^3} \int \Phi f(\mathbf{r}, \mathbf{k}, t) d^3 k$$
 (3)

This generates an infinite set of equations which must be closed by a suitably chosen ansatz. Closure after the second moment and assuming a cold Maxwellian distribution leads to the drift-diffusion equations, which for electrons read

$$\nabla \cdot \mathbf{J}_n = \mathbf{q}R + \mathbf{q}\frac{\partial n}{\partial t} , \qquad (4)$$

$$\mathbf{J}_n = \mathbf{q} n \boldsymbol{\mu}_n \mathbf{E} + \mathbf{q} D_n \nabla n \;. \tag{5}$$

In these equations J_n denotes the current density, R the net recombination rate, μ_n the mobility, E the electric field, and D_n the diffusion coefficient. Together with (1), a coupled equation system is formed which is solved numerically by means of the box integration method. From an engineering point of view, this model has proven amazingly successful due to its efficiency, numerical robustness, and the feasibility to perform two-and three-dimensional studies on fairly large unstructured grids. However, several shortcomings of this model are critical for miniaturized devices. Especially hot-carrier effects such as impact ionization or velocity overshoot motivated the development of higher-order transport models



Figure 2: Comparison of macroscopic transport models with full-band Monte Carlo [10]. While all models yield similar results at large gate lengths, only the six-moments model reproduces the short-channel Monte Carlo results.

such as the hydrodynamic, energy-transport, and six-moments model [8]. These models allow the electron energy distribution function to be described beyond the Maxwellian approximation, and they are used routinely in commercial and academic device simulators. As a calibration tool, the full-band Monte Carlo method has become accepted, since it can precisely account for the various scattering processes in the scattering operator [9]. Figure 2 shows a comparison of different macroscopic simulation approaches with full-band Monte Carlo results for a 250 nm and a 50 nm double-gate MOSFET [10]. It can be seen that transport models based on two, four, and six moments deliver similar results for the long-channel device, while only the six moments model is able to reproduce the full-band Monte Carlo results for the short-channel device.

1.3 Quantum-Ballistic Transport

Within the macroscopic transport models presented above, quantum-mechanical effects are usually accounted for by means of quantum corrections in the continuity equations. However, the fabrication of structures in the nanometer regime triggered the development



Figure 3: Comparison of CV characteristics of a 1.5 nm dielectric layer with different polysilicon doping applying onedimensional classical and quantummechanical simulations.

of quantum-mechanical modeling tools. This became especially important for the evaluation of gate dielectrics, which represent the smallest feature scale in microelectronics. Neglecting quantum confinement in this regime leads to results which are not just slightly inaccurate, but systematically wrong. As an example, the CV-characteristics of an 1.5 nm dielectric layer is shown in Figure 3 for different poly doping concentrations calculated classically and quantum-mechanically and showing a large discrepancy under inversion conditions. This apparent inaccuracy of conventional models justified the development of one-dimensional quantum device simulators which are today established tools for the characterization of gate dielectric layers [11, 12, 13]. Such one-dimensional solutions of the SCHRÖDINGER equation are also frequently used to derive correction factors for the carrier concentration calculated by macroscopic transport models [14, 15, 16]. They can be used to yield a quick estimate of quantum-confinement related effects without degrading the efficiency of the device simulator used. However, based on the closed-boundary SCHRÖDINGER equation charge transport is neglected.

Regarding quantum-mechanical current transport, quantum-ballistic models are predominantly

applied for the simulation of gate leakage caused by tunneling. Here, the central quantity is the transmission coefficient $TC(\mathcal{E})$ which is used in the so-called Tsu-Esaki equation

$$J = \frac{4\pi m_{\rm eff} q}{h^3} \int_{\mathcal{E}_{\rm min}}^{\mathcal{E}_{\rm max}} TC(\mathcal{E}_x) N(\mathcal{E}_x) \, \mathrm{d}\mathcal{E}_x \quad (6)$$

to calculate the tunneling current density. Methods such as the Wentzel-Kramers-Brillouin (WKB), the transfer-matrix, or quantum transmitting boundary method have been proposed to calculate the transmission coefficient [17]. The resulting tunneling currents can be easily incorporated into macroscopic transport models by means of additional generation/recombination processes in (4).

However, the further reduction of channel lengths raises the question for a fully quantum-mechanical treatment of carrier transport. This makes the solution of SCHRÖDINGER's equation with open boundary conditions necessary, which can be done by means of the quantum transmitting boundary method as shown in [18, 19]. An established and sophisticated framework for these calculations is the non-equilibrium Green's Function method, which is predominantly used for one-dimensional studies of resonant tunneling diodes [20]. Two- and three-dimensional quantum ballistic simulations can be performed by means of an adiabatic decomposition of wave functions into one or two confinement directions [21, 22]. Recently, simulators accounting for a full two-dimensional solution of the open-boundary SCHRÖDINGER equation have been reported and applied to the simulation of 10 nm double-gate MOSFETs [23, 24]. Besides the requirement for a fine and sometimes even equidistant mesh, a main obstacle in these approaches is that the treatment of scattering is not straightforwardly possible. Furthermore, these simulators are usually limited to specific geometries, restrictive grids, or small length scales, which makes their usability applications for engineering questionable. Nevertheless, these simulation approaches are necessary for the estimation of upper bounds of current transport at the quantum limit.

1.4 Quantum Transport

The methods described so far are either based on the assumption of pure classical or pure quantum transport. Modern microelectronic devices, however, are characterized by the transition between large reservoirs with strong carrier scattering, and small regions where quantum effects are important or even dominate. To first order, quantum correction models can account for these effects. A more rigorous approach is to consider models derived from the Wigner equation. The Wigner function is given by a transformation of the density matrix [25, 26]

$$f_{\rm w}(\mathbf{r}, \mathbf{k}, t) = \int \rho\left(\mathbf{r} + \frac{\mathbf{s}}{2}, \mathbf{r} - \frac{\mathbf{s}}{2}, t\right) \exp(-\iota \mathbf{k} \cdot \mathbf{s}) \,\mathrm{d}\mathbf{s} \,.$$
(7)

The kinetic equation for the Wigner function is the Wigner transport equation which is similar to the Boltzmann equation except the Wigner potential at the right-hand side

$$\left(\frac{\partial}{\partial t} + \mathbf{v} \cdot \nabla_r + \frac{\mathbf{q}\mathbf{E}}{\hbar} \cdot \nabla_k\right) f_{w} = \int V_{w}(\mathbf{r}, \mathbf{k} - \mathbf{k}') f_{w}(\mathbf{k}', \mathbf{r}, t) \mathrm{d}\mathbf{k}' + \left(\frac{\partial f_{w}}{\partial t}\right)_{\mathrm{coll}}.$$
(8)

The Wigner potential is defined by

$$V_{\rm w}(\mathbf{r}, \mathbf{k}) = \frac{1}{i\hbar (2\pi)^3} \int \left(V\left(\mathbf{r} + \frac{\mathbf{s}}{2}\right) - V\left(\mathbf{r} - \frac{\mathbf{s}}{2}\right) \right) \exp\left(-i\mathbf{k} \cdot \mathbf{s}\right) \,\mathrm{d}\mathbf{s} \,.$$
(9)

From this equation the quantum drift-diffusion or quantum hydrodynamic models can be derived applying the method of moments [27]. It is therefore more suitable for the implementation in device simulators than a SCHRÖDINGER-POISSON solver which strongly depends on non-local quantities. However, it was reported that, while the carrier concentration in the inversion layer of a MOS-FET can be modeled correctly, the method fails to reproduce tunneling currents [28].

Therefore, strong efforts have been undertaken to couple the most accurate classical device simulation approach, the Monte Carlo technique, with quantum-mechanical formulations [29, 30, 31]. One possibility is to use an effective potential instead of the solution of POISSON's equation in





10¹

10¹⁴

resonant tunneling diode [31].

the Monte Carlo simulation [32, 33]. That can be achieved by a convolution of the electrostatic potential with a GAUSSian function which leads to a smoothing of the original potential.

A less heuristic approach is to solve the WIGNER transport equation (8) by means of Monte Carlo techniques. Unlike classical distribution functions, however, the WIGNER function permits positive and negative values. Therefore, it cannot be interpreted as a probability distribution function, a peculiarity known as the negative sign problem. Instead, the WIGNER function can be modeled as the difference of two positive functions which describe in-scattering and out-scattering of particles. This approach has the advantage that it allows for a seamless transition between classical and quantum-mechanical regions in a device [31]. This method has been applied to the simulation of resonant tunneling diodes as shown in Figure 4 and it was recently used for the simulation of 10 nm double-gate MOSFETs [34].

A typical application of quantum transport interesting for device engineers is shown in Figure 5, depicting a cross-section through the channel of different multi-gate silicon-oninsulator devices, namely a FinFET (top) and a П-gate FET (bottom) [35]. Three-dimensional device simulations have been performed for turned-off devices ($V_{\text{DS}}=1.0 \text{ V}$, $V_{\text{GS}}=0.0 \text{ V}$) by



Figure 5: Carrier concentration in the middle of the channel of a turned-off triple-gate FinFET (top) and a II-FET [35] (bottom). The Π -gate efficiently suppresses the spurious drain field.

means of coupling a two-dimensional SCHRÖ-DINGER-Poisson solver to the device simulator MINIMOS-NT [36], and the figures show the resulting carrier concentrations. While only the gate-all-around structure can fully deplete the channel, the Π -gate FET efficiently shields the channel from the drain bias, while posing only moderate additional process complexity.

1.5 Conclusion

Semiconductor physics is a vast field and simulation approaches abound. Physicists are often tempted to use overly complicated

mean energy

Energy [eV] 0.1

approaches, in an understandable effort not to lose the important physics. However, some constraints for engineering application should be kept in mind. Models must be efficient: Timely results are more valuable than accurate analyses [37]. There is a need for three-dimensional simulations, even if they are only rarely applied to check for spurious effects. Device simulators must allow a coupling with process simulators, since a detailed, physics-based transport model is of no use if geometry and doping are not described correctly. Therefore, support of unstructured grids is necessary. Furthermore, the simulators should be general-purpose and not limited to specific geometries or simulation modes. It is still not clear which of the outlined quantum transport approaches will find its way into integrated TCAD environments, but its further success depends on efficient and accurate modeling of these new effects.

2 Improving the Ambipolar Behavior of Schottky Barrier Carbon Nanotube Field Effect Transistors

Due to the capability of ballistic transport, carbon nanotube field-effect transistors (CNTFETs) have been studied in recent years as a potential alternative to CMOS devices. CNTFETs can be fabricated with Ohmic or Schottky type contacts. We focus here on Schottky barrier CNTFETs which operate by modulating the transmission coefficient of Schottky barriers at the contact between the metal and the carbon nanotube (CNT). The ambipolar behavior of Schottky barrier CNTFETs limits the performance of these devices. We show that a double gate design can suppress the ambipolar behavior of Schottky barrier CNTFETs considerably. In this structure for an n-type device the first gate which is near the source controls electron injection and the second gate which is near the drain suppresses hole injection. The voltage of the second gate can be set to a constant voltage or to the drain voltage. We investigated the effect of the second gate voltage on the performance of the device and finally discuss the advantages and disadvantages of these designs.

2.1 Introduction

Carbon nanotubes (CNTs) have emerged as promising candidates for nanoscale field effect transistors. While early devices have shown poor device characteristics, improvements were achieved by using doped CNTs [38] or high- κ materials [39]. The contact between metal and CNT can be of Ohmic [40] or Schottky type [41, 42]. Schottky contact CNTFETs operate by modulating the transmission coefficient of the Schottky barriers at the contact between the metal and the CNT [38, 42], but the ambipolar behavior of Schottky barrier CNTFETs limits the performance of these devices [43, 44].

Two important figures of merit of transistors are the $I_{\rm on}/I_{\rm off}$ ratio and the subthreshold slope. By using thin high- κ materials as gate dielectric the subthreshold slope of CNTFETs can be improved [45], but due to their ambipolar behavior the $I_{\rm on}/I_{\rm off}$ ratio is limited. In this work we propose a double gate structure for CNTFETs. Using this structure the carrier injection at the source and drain contacts can be separately controlled. We show that for an n-type device electron injection at the source contact can be controlled via the first gate while the detrimental hole injection at the drain contact can be reduced by the second gate. Thus, the ambipolar behavior of CNTFETs can be completely avoided.

2.2 Approach

Assuming ballistic transport, we calculate the drain current using the Landauer-Büttiker formula [46]

$$I_{\rm d} = \frac{4q}{h} \int [f_{\rm s}(\mathcal{E}) - f_{\rm d}(\mathcal{E})] TC(\mathcal{E}) \mathrm{d}\mathcal{E}, \qquad (10)$$

where $f_{s,d}$ are equilibrium Fermi functions at the source and drain contacts and $TC(\mathcal{E})$ is the transmission coefficient through the device. The factor 4 in (13) stems from the twofold band and twofold spin degeneracy [38]. In this work we focus on ambipolar devices, where the metal Fermi level is located in the middle of the CNT band gap at each contact.

We evaluate $TC(\mathcal{E})$ using the WKB approximation [45, 47, 48]

$$\ln TC(\mathcal{E}) = -2\int k(x)\mathrm{d}x,\qquad(11)$$

and an idealized band structure [47, 48, 45, 49]

$$k = \frac{\mathcal{E}_{g}}{\sqrt{3}a\gamma_{0}}\sqrt{1 - \left(\frac{\mathcal{E} + qV(x)}{\mathcal{E}_{g}/2}\right)^{2}}dx, \qquad (12)$$

The symbol a = 0.246 nm denotes the lattice constant, \mathcal{E}_g is the band gap energy set here to 0.6 eV corresponding to a CNT of a diameter of 1.4 nm, $\gamma_0 = 2.5$ eV is the transfer integral, and V(x) is the electrostatic potential along the CNT. The integration in (15) is performed only within the classical turning points.



Figure 6: Comparison between the simulation and experimental results for an axial CNT.

For electrostatic analysis the Smart-Analysis-Package (SAP) [50] was used. Since we focus on the subthreshold behavior of CNTFETs, we neglect charge on the CNT, which is considered to be a good approximation for the off-state regime [38, 45, 44, 43].

As seen in Figure 6 our approach is in good agreement with experimental results for an axial CNT [51], more details can be found in [52]. Note that these calculations were performed for axial CNTs, which explains the low $I_{\rm on}/I_{\rm off}$ ratio and also the ambipolar behavior. In the following we will focus on lateral CNTs.

2.3 Results and Discussion

We investigated a double gate structure as sketched in Figure 7 and a single gate structure. In the latter case the gate is extended from source to drain, like in conventional FETs. We used the same geometric dimensions for simulations as indicated in Figure 7, except the CNT diameter was set to 1.4 nm.

As seen in Figure 7 high- κ and low- κ materials were used above and below the CNT. Like light refraction at the boundary of two media having different relative dielectric constants, the direction of the electric field will change. If the relative dielectric constant of the top material is higher than the bottom one, the direction of the electric field near



Figure 7: Sketch of the the double gate structure.

the CNT is directed along the CNT axis, suppressing the Schottky contact. As a result the control of the gate over the Schottky barrier is increased, leading to a higher subthreshold slope [45]. In this work we use the relative dielectric constants of the high- κ and low- κ materials of 11 and 3.9 respectively.

Figure 8 shows the current-voltage characteristics of the single gate structure. For this structure the current is symmetric with respect to the gate voltage, in agreement with experimental results [43, 45]. To understand this behavior the band edge profile for this single gate structure is shown in Figure 9. Positive gate voltages near the source increase the tunneling current of electrons, which is desirable for n-type devices. By decreasing the gate voltage the tunneling current of electrons decreases, but the thermionic emission current of electrons does not vary. If the gate voltage decreases further to negative values the thermionic emission current of electrons also decreases. On the other hand by applying positive voltages higher than the gate voltage to the drain, the Schottky barrier near the drain is suppressed and consequently hole injection at the drain increases, an undesirable phenomenon for an n-type device. Especially in the off regime this would result in an intolerably high off-current.

From the above discussion it seems reasonable to control the band edge profile near the source and the drain contacts separately, leading to a double gate structure as shown in Figure 7. The first gate near the source controls electron injection and the second gate near the drain suppresses hole injection at the drain contact.

We considered two possibilities for the second gate voltage:

- a) Applying the same voltage as the drain voltage.
- b) Applying a constant voltage equal or higher than the maximum drain voltage.

If the same voltage as at the drain is applied to the second gate, at any drain voltage the band edge profile near the drain would be flat, see Figure 11. In consequence the tunneling current of holes is suppressed and there is just some thermionic emission current of holes, resulting in an off-current which is nearly independent of the drain voltage and equals to the thermionic emission current over the Schottky barrier, see Figure 10.

If an even lower off-current is required, then the second gate can be biased at a fixed voltage which is higher than the maximum drain voltage. This results in suppressing the hole thermionic emission current, see Figure 11. As seen in Figure 10 by using this design a very low off-current can be obtained, but due to the exponential relationship between thermionic emission current and the barrier height the off-current increases exponentially as the drain voltage increases. When the drain voltage reaches the second gate voltage the drain current reaches the limit of the thermionic emission current of holes over the Schottky barrier. If the drain voltage is more increased, the tunneling current of holes also appears. This means that for having an off-current below the thermionic emission limit it is necessary to apply a voltage higher than the maximum drain voltage to the second gate.

In Figure 10 for the case of $V_{G2} = 0.8$ V a change in the subthreshold slope near zero gate voltage is seen. This phenomenon results from suppressing the thermionic emission current of electrons at the source contact. Since the relationship between the thermionic emission current and the barrier height is exponential, the subthreshold slope in this regime is near its ideal value 70 mV/dec. This behavior is not seen in other current voltage



Figure 8: Current-voltage characteristics of the single gate structure.



Figure 9: Band edge profile of the single gate structure.

characteristics since in other cases the hole current dominates over the electron current in the off regime. Here, however, the hole current is suppressed and the electron current is the dominant part of the total current.

For a better comparison between these designs current-voltage characteristics of the single gate and the double gate structures are shown in Figure 12. For the single gate structure the off-current is very high, but for the both double gate structures an $I_{\rm on}/I_{\rm off}$ ratio higher than five orders of magnitude can be obtained.



Figure 10: Current-voltage characteristics of the double gate structure.



Figure 11: Band edge profile of the double gate structure.

2.4 Conclusion

Our simulation results show that by using a double gate structure the $I_{\rm on}/I_{\rm off}$ ratio of CNTFETs can be increased considerably. The second gate voltage can be either set to the drain voltage or to a constant voltage higher than the maximum value of the drain voltage. The advantages of connecting the drain voltage to the second gate are avoiding parasitic capacitances between the second gate and the drain, avoiding a separate voltage source for the second gate, and also ease of fabrication.



Figure 12: Comparison between current-voltage characteristics of different structures at $V_d = 0.3$ V.

The disadvantage of this method is that the minimum off-current is limited to the thermionic emission current over the Schottky barrier. By applying a constant voltage higher than the maximum value of the drain voltage to the second gate, a very high $I_{\rm on}/I_{\rm off}$ ratio can be obtained. However, for both of these methods the $I_{\rm on}/I_{\rm off}$ ratio is higher than five orders of magnitude which is completely satisfactory for conventional logic applications.

3 Optimization of Single Gate Carbon Nanotube Field Effect Transistors

The performance of Schottky barrier carbon nanotube field effect transistors (CNTFETs) depends critically on the device geometry. Asymmetric gate contacts, the drain and source contact thickness, and inhomogenous dielectrics above and below the nanotube influence the device operation. An optimizer has been used to extract geometries with steep subthreshold slope and high $I_{\rm on}/I_{\rm off}$ ratio. It is found that the best performance improvements can be achieved using asymmetric gates centered above the source contact, where the optimum position and length of the gate contact varies with the oxide thickness. The main advantages of geometries with asymmetric gate contacts are the increased $I_{\rm on}/I_{\rm off}$ ratio and the fact that the gate voltage required to attain minimum drain current is shifted towards zero, whereas symmetric geometries require $V_{\rm G} = V_{\rm D}/2$. Our results suggest that the subthreshold slope of single gate CNT-FETs scales linearly with the gate oxide thickness and can be reduced by a factor of two reaching a value below 100 mV/dec for devices with oxide thicknesses smaller than 5 nm by geometry optimization.

3.1 Introduction

Semiconductor device technology using nanocarbon materials in semiconductor chip wiring is receiving accelerated development. This trend is mainly caused by their overall properties and not only by their small size. The electrical properties of carbon nanotubes can rival, or even exceed, the best metals or semiconductors known. The electrical behavior is a consequence of the electronic band structure which depends on the chiralty and the radius of the nanotube. Metallic nanotubes are promising for interconnects and vias [53] in integrated circuits because of their high electrical and thermal conductivity, whereas semiconducting tubes have emerged as possible candidates for nanoscale field effect transistors (CNTFETs) with the potential for ULSI integration [54, 55, 56, 57].

A critical issue for conventional CNTFET geometries is the required scaling of the drain voltage

 $V_{\rm D}$ as the gate oxide thickness ($T_{\rm ox}$) is decreased. The off-current (I_{off}) rises significantly when the absolute value of the drain current is increased leading to a decrease of $I_{\rm on}/I_{\rm off}$. This effect can be understood within the Schottky band model, where the subthreshold characteristics of CNT-FETs with symmetric geometries, i.e. symmetric gate, source, and drain contacts, is symmetric around the gate voltage $V_{G,off} = V_D/2$ [43]. At this point the barrier for electrons is the same as for holes and the minimum current will flow through the nanotube. The electron current rises with $V_{\rm G}$, whereas the hole current rises with $V_D - V_G$. For a large $V_{\rm D}$ the resulting gate voltage $V_{\rm G,off}$ is large enough to suppress the Schottky barriers at the nanotube contacts and thus large Ioff currents can flow. This effect will occur whenever the devices are scaled to smaller size, or high- κ gate oxides increase the electric field at the metal nanotube contacts.

Surprising effects regarding to the scaling of the performance of CNTFETs have been observed recently [58, 44, 59, 60]. It was shown that dielectrics with different permittivity above and below the nanotube influence the device operation. Furthermore it was demonstrated that asymmetric geometries with gate contacts located only in the vicinity of the source contact can enhance device performance. These unexpected scaling trends can be well understood, assuming that the transistor action is caused by the modulation of Schottky barriers at the metal-nanotube contact. The barriers can be thinned by applying gate voltages sufficiently large to allow tunneling of electrons or holes.

In this work an optimization setup (see Figure 13) is used to study the scaling behavior of CNTFETs. The device geometry and the permittivity of the dielectric material surrounding the nanotube is optimized to extract structures with a steep subthreshold slope $S = (d \log_{10} I/dV_G)^{-1}$ and a high I_{on}/I_{off} ratio. The one-dimensional transport model based on the Landauer Büttiker formula and the simulation setup are discussed in Section 3.2.



Figure 13: Diagram of the optimization tool flow.

The influence of the contact geometry and the effect of dielectrics on device performance are adressed and the results from geometry optimization are presented in Section 3.3.

3.2 Device Optimization

This paper focuses on single-gated device geometries, comparable to conventional MOSFETs with a single-walled nanotube replacing the silicon channel. We optimized this geometry (see Figure 14) with respect to the following six parameters: the position and length of the gate contact (by varying L_{dg} , L_{sg}), the thickness of source and drain contact (T_s , T_d), and the permittivity of the top and bottom dielectric (ε_{top} , ε_{bot}).

The simulation framework SIESTA [61] was used for the optimization. It provides various optimizers that can be chosen to fit best for the problems at hand. The optimizer used for this work is a genetic optimizer that relies on the theory of evolutionary computation and genetic algorithms. The population of the n-tuples of free parameters is chosen randomly with respect to a Gaussian normal distribution where a large set of distribution and generation parameters can be configured and tuned for various kinds of problems. Furthermore, the simulation of the population was distributed on a computer cluster to significantly decrease the optimization time. At start time SIESTA provides the initial values of the free geometry parameters (T_s , T_d , T_{ox} , L_{sg} , L_{dg} , ε_{top} , and ε_{bot}) as shown in Figure 13. These values are passed to the electrostatic solver, which calculates the potential profile for a device in the on-state and in the off-state. For the optimization of the $I_{\rm on}/I_{\rm off}$ ratio $I_{\rm on}/I_{\rm off}$ is defined as the ratio between the current at $V_{\rm G} = 1.5 \, {\rm V}$ and $V_{\rm G} = 0 \,\rm V$. Afterwards the potential along the nanotube for the two states is extracted and $I_{\rm on}$ and $I_{\rm off}$ are calculated. The $I_{\rm on}/I_{\rm off}$ ratio is submitted to the optimizer which generates the next n-tuple of free parameters to improve this The subthreshold slope was optimized value. analogously, submitting the ratio of the current at $V_{\rm G} = 0.3 \,\rm V$ and $V_{\rm G} = 0.2 \,\rm V$ to the optimizer. Since the regime where the subthreshold slope can be extracted when plotting $\log_{10} I$ over $V_{\rm G}$ depends on the geometry of the structure, the slope was afterwards reextracted from the optimized structures in a region where the slope was linear.

Electrostatic simulations were performed using the Smart-Analysis-Package [62]. This software contains a finite element solver to obtain the distributions of the potential and the electric field in the simulation domain. Electrical contacts with given voltages are represented by Dirichlet boundary conditions. For the rest of the border of the simulation domain a homogeneous Neumann boundary condition is assumed. The nonuniform triangular grid is refined at the metal-nanotube interface, where the Schottky barriers control the current through the tube. The resulting potential profile along the tube is used for the calculation of the transmission coefficient in a postprocessing step.

3.2.1 Transport Modeling

Coherent transport in the nanotube is described by the Landauer-Büttiker formula. The drain current through the nanotube is given by an integration in the energy domain [63]

$$I_{\rm d} = \frac{4q}{h} \int [f_{\rm s}(E) - f_{\rm d}(E)] TC(E) \mathrm{d}E \,, \qquad (13)$$

where $f_{s,d}$ are equilibrium Fermi functions at the source and drain contacts, and TC(E) is



Figure 14: Device geometry with simulation parameters.

the transmission coefficient. Note that, even if TC(E) = 1, the resistance of the tube is given by $h/(4q^2) \approx 6.5 \text{k}\Omega$, assuming two conduction channels in the tube. This quantum mechanical resistance stems from the difference of possible conduction channels in the tube and the macroscopic metal contact.

Accounting for an idealized CNT band structure [64], which is symmetric around the Fermi level, the first conduction (valence) band is given by:

$$E(k) = \pm \frac{\sqrt{3}a\gamma_0}{2} \sqrt{\left(\frac{1}{-3\rho_{\text{cnt}}}\right)^2 + k^2}, \quad (14)$$

where *a* denotes the lattice constant, $\gamma_0 = 2.5$ eV is the transfer integral, ρ_{cnt} is the nanotube radius, and *k* denotes the wavevector along the CNT radius. The transmission coefficient to states of the first conduction (valence) band is estimated using the Wentzel-Kramers-Brillouin (WKB) approximation [65]

$$\ln TC(E) = -2\int \frac{\mathcal{E}_{g}}{\sqrt{3}a\gamma_{0}}\sqrt{1 - \left(\frac{E + q\phi(x)}{\mathcal{E}_{g}/2}\right)^{2}}dx.$$
 (15)

Here \mathcal{E}_g is the CNT band gap energy and $\phi(x)$ is the electrostatic potential along the CNT. The integration is performed within the classical turning points.

For self-consistent simulations of CNTFETs we followed the approach of John [66, 67] solving

a one-dimensional open-boundary Schrödinger equation

$$-\frac{\hbar^2}{2m^*}\frac{\partial^2\Psi_s}{\partial x^2} + (\mathbf{U} - \mathcal{E})\Psi_s = 0, \qquad (16)$$

where Ψ_s is the wavefunction of a carrier with energy \mathcal{E} and effective mass m^{*}. The local potential energy *U* is given by $U_e = -q\phi(x) - \chi_{cnt}$, and $U_h = -U_e + \mathcal{E}_g$ for holes, with χ_{cnt} denoting the electron affinity. The charge induced on the carbon nanotube can be calculated from:

$$n_{\rm s,d} = \frac{4}{2\pi} \int f_{\rm s,d} |\Psi_{\rm s,d}|^2 dk_{\rm s,d} =$$
$$\int \frac{\sqrt{2m^*}}{\pi \hbar \sqrt{\mathcal{E}_{\rm s,d}}} f_{\rm s,d} |\Psi_{\rm s,d}|^2 d\mathcal{E}_{\rm s,d}. \tag{17}$$

Here, $n_{s,d}$ denote the concentrations induced from the source and drain side, respectively. The factor 4 in (13) and (17) stems from the twofold band and twofold spin degeneracy [68]. The total carrier concentrations $n = n_s + n_d$ and $p = p_s + p_d$ enter the Poisson equation

$$\nabla \varepsilon \nabla \phi = -\frac{q(p-n)\delta(\rho - \rho_{\text{cnt}})}{2\pi\rho}, \qquad (18)$$

where δ denotes the Dirac delta function describing the CNT charge density. Carriers were considered as charged sheets with the charges being distributed uniformly around the surface of the nanotube. The Poisson equation is solved self-consistently with the Schrödinger equation (16) using the general purpose device simulator MINIMOS-NT [36]. Band structure modifications due to the potential drop across the nanotube diameter occuring in planar geometries have been neglected since the potential variation across the nanotube diameter is below 0.8 V [69, 70].

3.2.2 Simulation Setup

For device optimization a (16,0) nanotube with a length of 120 nm was assumed to connect the source and drain contact of the CNTFET. The nanotube's band gap \mathcal{E}_g and radius ρ_{cnt} were set to 0.6 eV and 0.63 nm, respectively. For the effective mass m^{*} a value of 0.06 m₀ was chosen, both for electrons and holes[71].



Figure 15: Conduction band edge for three gate voltages from self-consistent (solid lines) and non-self-consistent calculations at $V_{\rm D} = 0.2$ V.

The length of the source and drain contact and the overall thickness of the simulation domain were the only geometry parameters fixed during the optimization process $(L_s = L_d = 10 \text{ nm},$ T = 100 nm). We focus on mid-gap Schottky barriers where the Fermi level of the metal contacts is located in the middle of the CNT bandgap. Charge on the CNT was neglected during the optimization. Setting n and p to zero in (18), only (13) and (18) have to be solved in a single optimization step. For positive-barrier devices of the type considered here, this leads to only a very slight overestimation of the current $(\approx 10\%)$ with respect to that predicted by a fully self-consistent solution [66], even when the device is in the on-regime [72, 58]. In Figure 15 the band bending along the CNT is plotted for a self-consistent simulation and a simulation where the charge on the CNT has been neglected. It can be seen that the Schottky barriers at the source and drain side are not significantly changed in the energy range of significant tunneling current.

3.3 Simulation Results

In order to get a better understanding of the optimization results, the influence of size and location of the gate contact, size of drain and source contact, and the permittivity of the top and bottom dielectric on the device performance are adressed independently in this section. Our



Figure 16: Subthreshold characteristics for different gate contact geometries. The solid line shows the drain current I_d for a symmetric geometry with $L_{dg} = L_{sg} = 5 \text{ nm}$, whereas the other lines correspond to geometries with an increased distance between the gate and the drain contact.

results for symmetric geometries show good agreement with recent simulations [43, 58, 44], where these parameters have been investigated separately. Then the results of the CNTFET geometry optimization for several fixed gate oxide thicknesses are presented. Finally, we compare important figures of merit like the subthreshold slope *S* and the $I_{\rm on}/I_{\rm off}$ ratio of optimized geometries with values from conventional geometries from both simulation and experiments.

3.3.1 Effect of the Gate Geometry

CNTFETs with symmetric gate contacts show ambipolar behavior leading to a symmetric subthreshold characteristics, drawn as solid line in Figure 16. When $V_G = V_D/2$ the current through the nanotube reaches its minimum [43]. The amount of electron tunneling from the source side is equal to the hole tunneling from the drain side for this gate bias. Larger gate voltages allow more electron tunneling from the source side whereas the hole current from the drain is essentially supressed. When $V_G < V_D/2$ hole tunneling is favored and the electron current is supressed, whereas for $V_G > V_D/2$ electron current dominates over hole current. When using asymmetric structures the subthreshold characteristics becomes asymmetric. In Figure 16 the subthreshold characteristics of geometries with $L_{dg} > 5 \text{ nm}$ are plotted. While $L_{\rm sg} = 5\,\rm nm$ is kept constant, the length of the gate contact is decreased by increasing L_{dg} and thus the control of the gate over the CNT at the drain side is partially lost. This geometry modification directly affects the subthreshold characteristics where a lower hole current can be observed at small or negative gate voltages. At the same time the electron current which dominates for $V_{\rm G} > V_{\rm D}/2$ is insensitive to the different gate placement. Only if the overall gate length is below a critical value, a decrease of electron current takes place. This is illustrated in Figure 16, where the subthreshold characteristics for a geometry with $L_{dg} = 130$ nm, thus having a gate length of only 5nm, is plotted. The decrease of the subthreshold slope is noticable, but due to fringing fields from the gate contact the device can still be turned on. From Figure 16 it can also be seen, that the gate voltage leading to a minimum drain current moves towards zero as the gate length decreases. Thus asymmetric structures have the advantage that the $I_{\rm off}$ current is located around 0 V, which is more practical for real life applications. Generally it can be observed that Ion and the subthreshold slope are only weakly influenced by the location of the gate as long as $L_{\rm dg}$ stays beyond a critical value, whereas $I_{\rm off}$ can be reduced which results in a higher $I_{\rm on}/I_{\rm off}$ ratio.

3.3.2 Effect of Drain and Source Contact Geometries

To achieve low I_{off} it is necessary to have large tunneling barriers for both electrons and holes at the source and drain contact in the off-state. CNTFETs with thin needle-like contacts have thinner tunneling barriers than devices with large contacts for source and drain which can be understood from simple electrostatic arguments. Hence large contacts have broader barriers and are able to reduce I_{off} . From Figure 17 it can be seen how the hole current is reduced for a device with $T_d = 20$ nm as compared to a device with a needle like drain contact with $T_d = 2.5$ nm. For both geometries $T_s = 2.5$ nm, and it can be seen



Figure 17: Drain current as a function of $V_{\rm G}$ for a drain thickness $T_{\rm d}$ of 20nm (squares) and 2.5 nm (circles). Solid lines are used for the total current and dashed lines for the hole current which is reduced in the case of large $T_{\rm d}$ (squares). The electron current (dash-dotted line) is the same for both cases.

that the electron current is not influenced by the increase of $T_{\rm d}$. In the same manner as $I_{\rm off}$ can be reduced by increasing the drain contact thickness, the tunneling barrier for electrons at the source side can be reduced using thin source contacts resulting in an increase of $I_{\rm on}$.

3.3.3 Effect of Inhomogenous Dielectrics

been reported that using different It has materials above and below the carbon κ nanotube increases the subthreshold slope of CNT-FETs [58], where this effect was explained from the refraction law for electric field lines at interfaces of materials with different permittivities:

$$\frac{\tan \alpha_{\rm top}}{\varepsilon_{\rm top}} = \frac{\tan \alpha_{\rm bot}}{\varepsilon_{\rm bot}} \tag{19}$$

Here α_{top} and α_{bot} are the incident field line angles between normal to the interface between a top and bottom dielectric. (19) is valid when the charge on the tube is neglected and results in a lowering of the barrier when using materials with different permittivity above and below the tube. The effect is more pronounced for thick gate oxides and



Figure 18: Conduction band edge near the source contact for a device with $T_{ox} = 10$ nm, plotted for three different ratios $\delta = \epsilon_{top}/\epsilon_{bot}$. For higher δ the energy barrier is thinned. The inset shows the impact of inhomogenous dielectrics on the subthreshold characteristics at $V_D=0.3$ V.

becomes stronger as the ratio $\delta = \varepsilon_{top}/\varepsilon_{bot}$ is increased (see Figure 18). The inset of Figure 18 shows that the reduction of the barrier caused by $\delta > 1$ results in higher drive currents. Furthermore it can be observed that the overall subthreshold characteristics is shifted upwards and the subthreshold slope increases when increasing δ . On the other hand side I_{on}/I_{off} is not influenced by this effect.

For CNTFETs with symmetric gate geometries by increasing δ the potential barrier for holes tunneling from the drain side is reduced in the same manner as the tunneling barrier for electrons is reduced. This leads to high off-currents at large V_d and requires a proper scaling of V_D. To the contrary, the hole tunneling of CNTFETs can be suppressed with an asymmetric contact geometry and inhomogenous dielectrics can improve device characteristics for a large range of drain voltages.

3.3.4 Optimized Geometries

Finally we present results of the device optimization of CNTFETs with different gate oxide thicknesses. In the optimization setup we fixed T_{ox} and



Figure 19: Comparison of subthreshold slope and $I_{\rm on}/I_{\rm off}$ ratio for conventional (dashed lines) and optimized (solid lines) geometries. Experimental data for the subthreshold slope from [58] shows a similar scaling behavior.



Figure 20: Optiomization results for a homogenous (dashed line with open circles) and a inhomogenous CNTFET (solid line with open squares). The gate length, the $I_{\rm on}/I_{\rm off}$ ratio, and the subthreshold slope *S* are plotted.

varied the other geometry parameters in order to find optimized structures for a given T_{ox} .

We find that devices with inhomogenous dielectrics, thin source contacts, thick drain contacts yield the best subthreshold slope for the whole range of gate oxide thicknesses (2-30 nm). However, the length of the gate contact which results in the optimum subthreshold slope depends on T_{ox} . It was found that the current through the CNT does not depend on L_{sg} as long as $L_{sg} < 10$ nm, which results in a small overlap of gate and source contact. The gate length L_{g} for structures optimized with respect to a steep subthreshold slope continuously decreases when decreasing T_{ox} . This stems from the fact that for geometries with small T_{ox} the gate contact is more efficient in suppressing the potential barriers at the source (drain) contact. While geometries with a large T_{ox} need a larger gate contact in order to control the current over the potential barrier at the source contact, $L_{\rm g}$ can be reduced for geometries with small T_{ox} .

From Figure 19 it can be seen that for geometries optimized with respect to the subthreshold slope, the subthreshold slope scales approximately as T_{ox} . For comparison in Figure 19 also the subthreshold slope of a symmetric CNTFET ($L_{\text{dg}} = L_{\text{sg}} = 5 \text{ nm}$, $T_{\text{s}} = T_{\text{d}} = 10 \text{ nm}$, $\varepsilon_{\text{top}} = \varepsilon_{\text{bot}} = 3.9$) is given. In addition to the improved subthreshold slope for these geometries, the $I_{\text{on}}/I_{\text{off}}$ ratio is increased when decreasing the gate oxide thickness. This behavior is different from that of symmetric CNTFETs. For symmetric geometries the $I_{\text{on}}/I_{\text{off}}$ ratio of $I_{\text{on}}/I_{\text{off}}$ takes place. The $I_{\text{on}}/I_{\text{off}}$ ratio of symmetric and optimized CNTFETs are plotted in the lower graph of Figure 19.

When optimizing geometries with respect to the $I_{\rm on}/I_{\rm off}$ ratio, a different behavior occurs. At $T_{\rm ox} > 10$ nm structures with inhomogenous dielectrics show a steeper subthreshold slope as well as a higher $I_{\rm on}/I_{\rm off}$ ratio, while at $T_{\rm ox} < 10$ nm geometries with homogenous dielectrics have a larger $I_{\rm on}/I_{\rm off}$ ratio than geometries with inhomogenous dielectrics. This can be seen from Figure 20, where the gate length, $I_{\rm on}/I_{\rm off}$, and the subthreshold slope of optimized geometries with $\delta = 1$ ($\epsilon_{top} = \epsilon_{bot} = 3.9$) and $\delta = 20$ $(\varepsilon_{top} = 20, \varepsilon_{bot} = 1.0)$ are plotted. Furthermore it can be observed that the length of the gate contact, leading to the maximum $I_{\rm on}/I_{\rm off}$ ratio, is larger when using homogenous dielectrics. This can be explained by the more efficient reduction of the

potential barriers taking place in inhomogenous structures.

3.4 Conclusion

The $I_{\rm on}/I_{\rm off}$ ratio of single gate CNTFET structures can be significantly improved by using an asymmetric gate contact located near the source contact and thin source and wide drain contacts. Additionally the subthreshold slope of such geometries can be improved by inhomogenous dielectrics above and below the tube, whereas the use of inhomogenous dielectrics in symmetric structures merely leads to high $I_{\rm off}$ currents. A subthreshold slope below 100 mV/dec was found for optimized geometries with $T_{\rm ox} < 5$ nm, which is significantly closer to the thermal limit of about $k_{\rm B}T \ln 10 \sim 60 \,\mathrm{mV/dec}$ at room temperature than previously reported values for conventional geometries [43]. Simulation results suggest that the subthreshold slope of single gate CNTFETs scales linearly with the gate oxide thickness.

In contrast to symmetric devices, structures with asymmetric gate contacts show an increase of $I_{\rm on}/I_{\rm off}$ when scaling down the gate oxide thickness, whereas $I_{\rm on}/I_{\rm off}$ decreases with increasing $T_{\rm ox}$ for symmetric devices when $T_{\rm ox} < 10$ nm.

4 Mixed-Mode Device and Circuit Simulation

We present the motivation for mixed-mode device and circuit simulation. The possible approaches are discussed and the particular methods of the multi-dimensional device/circuit simulator MINIMOS-NT are presented. The available capabilities are demonstrated on a Colpitts oscillator and two intermediate circuits, which are matter of transient and small-signal ac simulations.

4.1 Motivation

Advances in the development of semiconductor devices have lead to more and more sophisticated device structures. This concerns device geometry as well as doping profiles and the combination of different materials. Due to shrinking device geometries, the models describing the device physics increase in complexity. Traditional device simulation has considered the behavior of isolated devices under artificial boundary conditions (singlemode). To gain additional insight into the performance of devices under realistic dynamic boundary conditions imposed by a circuit, mixed-mode simulations have proven to be invaluable. However, this problem is very complex and only limited solutions have been available so far. The main advantages of mixed-mode simulations are:

- A calibrated device simulator can be directly employed for circuit simulations: No subsequent and often expensive parameter/model extraction is necessary. Thus, in time-to-market considerations results of many different devices are available at significantly earlier times.
- It is common practice to create optimization loops consisting of process and device simulators. Controlled by various kinds of optimizers, device figures of merit (e.g., cutoff frequency f_i) trigger process variations in order to be improved. By switching the device simulator in the mixed-mode, also circuit figures of merit can be optimization targets.

The major drawback in comparison to compact model approaches is the significant performance difference, since much larger equation systems have to be assembled and solved.

4.2 Introduction

Over the last decades, numerous powerful circuit simulation programs have been developed. Amongst those are general purpose programs (e.g., ASTAP [73] or SPICE [74]) and special purpose programs providing highly optimized algorithms, e.g. for filter design. They have in common that the electrical behavior of the devices is modeled by means of a compact model, that is, analytical expressions describing the device behavior. Once a suitable compact model is found, it can be evaluated in a very efficient way. However, this task is far from being trivial and many complicated models have been developed. Even if the behavior of the device under consideration can be mapped onto one of the existing compact models, the parameters of this compact model have to be extracted, which is obviously a cumbersome task.

The BSIM4.4.0 model [75] for short-channel MOS transistors provides over 300 parameters for calibration purposes, the VBIC95 model [76] for bipolar junction transistors offers about 30. If the device design is known and not modified, these parameters need to be extracted only once and can be used for circuit design as long as they deliver sufficiently accurate results. For example, the approximations that underlie the Spice Gummel-Poon [74] model ignore effects that are important for accurate modeling of today's bipolar technologies.

When there is need to optimize a device using modified geometries and doping profiles, the compact model parameters have to be extracted for each different layout, since many of these parameters are mere fit parameters without any physical meaning.

4.2.1 Device Simulation

To cope with exploding development costs and strong competition in the semiconductor industry today, Technology Computer-Aided Design (TCAD) methodologies are extensively used in development and production. Several questions during device fabrication, such as performance optimization and process control, can be addressed by simulation.

The electrical behavior of devices can be obtained by numerical simulators, such as DESSIS [77], These MEDICI [78], or MINIMOS-NT [36]. device simulators solve the semiconductor equations for a device with given doping profiles and a given geometry. The transport equations form a highly nonlinear partial differential equation system which cannot be solved analytically. Numerical methods must be applied to calculate a solution by discretizing the equations on a simulation grid [79]. The data obtained from these simulations can be used to extract the parameters of the compact model.

4.2.2 Circuit and Device Simulation

Altogether, this subsequent use of different simulators and extraction tools is cumbersome and error-prone. To overcome these problems several solutions have been published where a device simulator was coupled to the circuit simulator SPICE [80]. This is again problematic, when considering the communication between two completely different simulators. On the other hand some solutions were presented, where circuit simulation capabilities were added to a However, application device simulator [81]. was severely restricted, in particular due to limitations regarding the distributed devices. Commercially available simulators like DESSIS provide mixed-mode circuit simulations with SPICE and physical models.

Our device simulator MINIMOS-NT has been equipped with full circuit simulation capabilities [82] with the only major limitation being the available amount of computational resources. MINIMOS-NT is a general purpose device simulator developed as the successor of MINIMOS [83]. Whereas the latter is restricted to rectangular MOS structures, MINIMOS-NT can be employed for arbitrary device structures with unstructured grids.

4.3 Circuit Equations

A physical circuit consists of an interconnection of circuit elements. Two, actually, well-known different aspects have to be considered when developing a mathematical model for a circuit.

First, the circuit equations must satisfy Kirchhoff's topological laws:

- Kirchhoff's current law: the algebraic sum of currents leaving a circuit node must be zero at every instant of time.
- Kirchhoff's voltage law: the algebraic sum of voltages around a circuit loop must be zero at every instant of time.

Second, each circuit element has to satisfy its branch relation which will be called a constitutive relation in the following. There are current-defined branches where the branch current is given in terms of circuit and device parameters, and voltage-defined branches where the branch voltage is given in terms of circuit and device parameters. Devices with N terminals can be described using $N \cdot (N-1)/2$ branch relations. It is not necessary to include all branch currents and voltages into the vector of unknowns x, it is possible to also include charges and fluxes into x. The wide choice of possible unknown quantities leads to a huge variety of equation formulations that are available.

Furthermore, depending on the choice of x, different phenomena may be described and the complexity of the problem varies drastically. From the vast number of published methods, the nodal approach and the tableau approach [84] are the most important. Whereas the latter is the most general approach allowing also simulation of many idealized theoretical circuit elements, it has several inherent disadvantages (e.g., ill-conditioned system matrices). Since the main objective is to solve realistic devices, the nodal approach perfectly suits the needs.

4.3.1 The Nodal Approach

The independent variables of the nodal approach are the node voltages of each circuit node to a reference node which can be chosen arbitrarily. This choice guarantees that Kirchhoff's voltage law is fulfilled. Kirchhoff's current law is applied to each node other except the reference node in the circuit such that the summation of the currents leaving the node is zero. Thus, in matrix representation, the admittance matrix of the circuit is assembled, which consists of N-1 independent equations for a circuit of N nodes. The admittance matrix can be assembled by inspection on a per-element basis. The various admittance matrices of the circuit elements can simply be superpositioned to yield the complete circuit admittance matrix. Current sources contribute to the current source vector on the right-hand-side of the equation system. All contributions are commonly referred to as stamps as they can be directly stamped into the equation system without considering the rest of the circuit.

For circuits containing conductances and current sources only, the condition of the resulting system matrix is very good. In this case the nodal approach produces diagonal-dominant matrices which are well suited for iterative solution procedures. Two additional devices can be modeled, namely a voltage controlled current source and the gyrator. However, these devices destroy the diagonal dominance of the circuit admittance matrix.

4.3.2 The Modified Nodal Approach

One disadvantage of the nodal approach is the inadequate treatment of voltage sources. Ideal voltage sources and current controlled elements cannot be modeled with this approach. However, a very large class of integrated circuits can be accommodated by adding a provision for grounded sources. The modified nodal approach [85] overcomes these shortcomings by introducing branch currents as independent variables, which are available to formulate the device constitutive relations.

The modified nodal approach enjoyed large popularity due to its simplicity and ease of implementation and is employed in SPICE. But the numerically well-behaved system matrix obtained by the nodal approach is distorted by those additional equations, and some additional measures (see section Numerics) have to be taken. Furthermore, the additional equations can even produce zero diagonal entries which are avoided by exchanging the rows of the admittance matrix [86].

4.3.3 Simulator Coupling

Several efforts dealing with circuit simulation using distributed devices have been published so far [80, 81]. Most publications deal with the coupling of device simulators to SPICE. This results in a two-level Newton algorithm since the device and circuit equations are handled subsequently. Each solution of the circuit equations gives new operating conditions for the distributed devices. The device simulator is then invoked to calculate the resulting currents and the derivatives of these currents with respect to the contact voltages.

The alternative approach is called full-Newton algorithm as it combines the device and circuit equations in one single equation system. This equation system is then solved applying Newton's algorithm. In contrast to the two-level Newton algorithm where the device and circuit unknowns are solved in a decoupled manner, here the complete set of unknowns is solved simultaneously. In MINIMOS-NT the capability to solve circuit equations was added to the simulator kernel. This allowed for assembling the circuit and the device equations into one system matrix which results in a real full-Newton method.

4.3.4 Thermal Simulation

As thermal circuit simulation is an equivalent problem to electrical simulation, one can make use of similar formulations. The thermal interaction between the distributed devices is modeled by solving the lattice heat flow equation in conjunction with a thermal network. The thermal heat flow over the contact replaces the electrical current and the contact temperature the contact voltage.

4.4 The Device Simulator

In order to analyze the electronic properties of an arbitrary semiconductor structure under all kinds of operating conditions, the effects related to the transport of charge carriers under the influence of external fields must be modeled. In MINIMOS-NT carrier transport can be treated by drift-diffusion and hydrodynamic models.

The transport models are based on the semiclassical Boltzmann transport equation which is a timedependent partial integro-differential equation in the six-dimensional phase space. By the so-called method of moments this equation can be transformed in an infinite series of equations. Keeping only the zero and first order moment equations (with proper closure assumptions) yields the basic semiconductor equations (drift-diffusion model). These equations as given first by VanRoosbroeck [87] are the Poisson equation, the continuity equations for electrons and holes. The unknown quantities of this equation system are the electrostatic potential ψ , and the electron and hole concentrations *n* and *p*, respectively. The heat flow equation is added to account for thermal effects in the device, which requires proper modeling of the thermal conductivity, the mass density, and the heat capacity.

Considering two additional moments gives the hydrodynamic model [88], where the carrier temperatures are allowed to be different from the lattice temperature. Since the current densities depend then on the respective carrier temperature, two more unknowns, the electron temperature T_n and the hole temperature T_p , are added.

The physical models implemented in MINIMOS-NT allow the simulation of today's advanced devices, since all important physical effects such as bandgap narrowing, surface recombination, transient trap recombination, impact ionization, selfheating, and hot electron effects can be taken into account. The simulator deals with different complex structures and materials, such as Si, Ge, SiGe, GaAs, AlAs, InAs, GaP, InP, their alloys and nonideal dielectrics.

4.4.1 The Input-Deck

MINIMOS-NT employs a powerful input-deck [89], enabling the user to customize the simulation in many details. The basic idea is that the input-deck is not evaluated once at the beginning of the simulation, but is stored as a database which can be accessed at runtime. Since each keyword in this input-deck can be an arbitrary complex and time dependent expression, fine-tuning can be done without the need of any predefined heuristic algorithms.

4.4.2 Iteration Schemes

The need for iteration schemes arises from the fact that, when solving very complex coupled equation systems, the solution can very often not be obtained from the available initial-guess as the region of attraction for the Newton scheme would be to small. Hence, the problem can be split into different levels of complexity with each of them using the previous level as an initial-guess to further refine the solution by applying more complicated models. This procedure is called iteration scheme. MINIMOS-NT provides an interface so that iteration schemes can be arbitrarily programmed with several additional options making use of the features provided by the input-deck [82]. An iteration scheme consists of arbitrarily nested iteration blocks. Each block can have subblocks which will be evaluated recursively.

For mixed-mode an iteration scheme consisting of two blocks has been created. In the first block, specified node voltages are kept constant in order to obtain a converged solution for the distributed devices. This block is similar to single-mode device simulation. In the second block, the fixed voltages are set free in order to start the full circuit simulation.

4 Mixed-Mode Device and Circuit Simulation



Figure 21: Circuits with the three subcircuits as shown in Figure 22.

4.4.3 Numerics

The full-Newton method is characterized by integrating one or more distributed devices in one equation system. Whereas the compact models require relatively few equations per device, the complete discretized structure of each device has to be taken into account. For example, if one MOS structure requires 10.000 equations, about 100.000 equations for a ring-oscillator consisting of ten transistors must be assembled. As stated above, the modified nodal approach yields system matrices with numerically problematic equations which can distort the convergence of these solver systems. Therefore, specific preconditioning measures such as pre-elimination of numerically or structurally problematic equations have to be taken, which are provided by the linear assembly module [90]. Basically, iterative methods such as BI-CGSTAB are preferred for solving large linear However, for mixed-mode equation systems. simulations with more than one distributed device state-of-the-art implementations of direct solvers show a significant performance advantage.

4.5 Example Circuits

In the following the implemented features are demonstrated on the simulation of a Colpitts oscillator. We start building an amplifier which is the first example circuit. In the second step a resonant circuit is coupled to the output of the amplifier. The oscillator is eventually constructed by feeding back the output.



Figure 22: The three subcircuits which are embedded in the example circuits.

Since all three circuits (see Figure 21) consist of equal subcircuits (see Figure 22), the input-deck inheritance feature can be perfectly The section SubCircuits contains used. the definition of all three subcircuits. The settings for the distributed devices are specified like in the single-mode [36]. In addition, MINIMOS-NT directly provides compact models of the commonly used circuit elements like capacitors and inductors. Therefore, the respective Devices sections have to be simply inherited and their public members accordingly In the definition of the resonant overwritten. circuit both terminals are connected to the input, output, and ground nodes of the subcircuit: SubCircuits

```
{
LC
 {
      = ""; // is assigned in circuit
  in
  out = "";
     : ~Devices.L { N1 = ^in;
  T.1
                      N2 =  out;
                      L = 1 nH; }
  Cla : ~Devices.C { N1 = ^in;
                      N2 = "qnd";
                      C = 0.279 \text{ pF}; }
  C1b : "Devices.C { N1 = "gnd";
                      N2 = out;
                      C = 2.790 \text{ pF}; }
 // [...]
```

4.5.1 Amplifier

The amplifier circuit is a combination of the core, the ac source subcircuits and load elements. The transistor used in the core subcircuit is a $0.4 \times 12 \mu m^2$ SiGe-HBT device structure obtained by process simulation [91]. The structure was thoroughly investigated by steady-state and small-signal ac simulations as presented in [92].

All simulations use the mixed-mode iteration scheme. In the first block the fixed node voltages apply static boundary conditions at the transistor terminals in order to improve convergence to an initial solution useful for the subsequent circuit simulations. In this case, the three fixed node voltages ($V_{pin2} = 2.0$ V, $V_{pinB} = 1.2$ V, and $V_{pinE} = 0.4$ V) represent the dimensioning of the circuit in respect to the chosen operating point. Transient simulation results are shown in Figure 23. Due to the large equation system with a dimension of 11.601, the simulator requires between 1.0 and 2.9s per time step (2.4 GHz single Intel Pentium IV with 1 GB memory).

4.5.2 Amplifier with resonant circuit

The second example circuit consists of all three subcircuits, since the resonant circuit is now coupled to the output of the amplifier. The resonant circuit is configured for an oscillation frequency of 10GHz. This can be confirmed by results of a small-signal ac simulation as shown in Figure 24 ($V_{ac} = 1 \text{ mV}$). In average, MINIMOS-NT requires 8.5 s per frequency step. With a VBIC95 compact model of a similar transistor, the circuit simulator ADS [93] was used to obtain data from the same circuit.

4.5.3 Colpitts oscillator circuit

Finally, a Colpitts oscillator circuit is built by feeding back the output of the resonant circuits to the input of the core circuit (amplifier).

```
CircuitOscillator {

Core: SubCircuits.Core { in = "pin1";

out = "pin2"; }

LC : SubCircuits.LC { in = "pin2";

out = "pin1"; }

}
```

At turn on, random noise is generated within the active device, which is here the SiGe bipolar junction transistor, and then amplified. This noise is



Figure 23: Result of transient simulation of the amplifier circuit with $V_{ac} = 10 \text{ mV}, f = 2.4 \text{ GHz}.$



Figure 24: Result of small-signal ac simulation of the resonant circuit. The results are compared with ADS simulations using a VBIC95 model of a similar transistor.

fed back positively through the frequency selective circuit (resonant circuit consisting of an inductor and two capacitors) to the input, where it is amplified again. After the initial phase, a state of equilibrium is reached. Then, the losses of the circuit are compensated by the power supply. The amount of feedback to sustain oscillation is basically determined by the C_{1a}/C_{1b} ratio.

Transient simulation results are shown in Figure 25. In the simulator, the random noise of the active device is replaced by a numerical noise caused by the restricted representation of floating point numbers. The simulator requires 0.4s in the initial phase and between 1.9s and 2.9s in the state of equilibrium per time step.



Figure 25: Result of the transient simulation of the oscillator. The upper figure shows the output V_{pin2} in the initial phase, the lower figure both possible outputs in the state of equilibrium.

4.6 Conclusion

The highly sophisticated models required for today's advanced device structures can be directly employed for circuit simulations. MINIMOS-NT has been equipped with many powerful capabilities for these mixed-mode simulations. One or more distributed devices can be embedded in arbitrary circuits applying realistic dynamic boundary conditions. In turn, the setup of MINIMOS-NT can be based on compact models using the circuit simulator only.

5 Anisotropic Laplace Refinement for 3D Oxidation Simulation

We present a computational method for threedimensional tetrahedral mesh refinement according to the demands of oxidation simulation. The main focus lies on two major problems. First, the start-up condition of oxidation claims an initial mesh preparation which is done by the so called Laplace refinement, second the transient conversion of silicon (Si) to silicon dioxide (SiO₂) forces a high spatial resolution in a small area around the material interface which shows the need of adaptive refinement on demand. More over our approach takes anisotropy into account to keep the amount of elements small compared to strict isotropic refinement.

5.1 Introduction

Oxidation, by the means of a process step involved in the fabrication of integrated circuits (IC), is an directional and surface near process step. This means that the interesting simulation region is near the surface and therefore it is important to guarantee a good spatial resolution at the *skin* of the simulation domain.

This can only be achieved efficiently by anisotropic meshes. Strict isotropic threedimensional regular meshes are not practicable for realistic structures due to required high resolution compared to the size of the simulation domain. The demand on calculation time and the limitation of memory requires anisotropic meshes.

The generation of small, strongly anisotropic, and unstructured mesh layers by three-dimensional mesh generators is, unfortunately from a technology point of view, still something of an art, as well as a science [94]. A more robust way is to generate mostly isotropic coarse initial meshes for instance with a Delaunay mesh generator, followed by a mesh adaption post processing step on demand. A means to an end for this task is a robust grid refinement step which is based on tetrahedral bisection. One way to increase spatial resolution and to take anisotropic mesh refinement at the same time into account was shown in [95]. The basic idea in this work is to introduce a metric tensor function. The initial mesh refinement is based on the solution of the Laplace equation, while the dynamic adaptation observes the diffuse interface function which describes the moving boarder between silicon and silicon dioxide.

5.2 Anisotropic Metric

The idea used in our approach is to apply a combination of rotation and dilation to define an anisotropic metric. The dilation is represented by three scalar values $\lambda_{\xi}, \lambda_{\eta}$ and, λ_{ζ} , respectively. Using $(\vec{\xi}, \vec{\eta}, \vec{\zeta})$ and $(\lambda_{\xi}, \lambda_{\eta}, \lambda_{\zeta})$ we define two matrices

$$\mathbf{R} := \begin{pmatrix} \xi_x & \eta_x & \zeta_x \\ \xi_y & \eta_y & \zeta_y \\ \xi_z & \eta_z & \zeta_z \end{pmatrix} \text{ and}$$
$$\mathbf{S} := \begin{pmatrix} \lambda_{\xi} & 0 & 0 \\ 0 & \lambda_{\eta} & 0 \\ 0 & 0 & \lambda_{\zeta} \end{pmatrix} \text{ which leads to}$$
$$\mathbf{M} := \mathbf{R}\mathbf{S}\mathbf{R}^T.$$

The anisotropic metric **M** is a tensor function which varies over the domain $\mathbf{M} = \mathbf{M}(x, y, z)$. The tensor function is symmetric and positive definite which allows to use this tensor as a metric tensor.

5.3 Laplace Refinement

Our idea is to use the solution of Laplace's equation as approximation for a surface distance function. The imagination is based on electrostatic field calculations of the plate-capacitor. A typical plate-capacitor structure is formed by two coplanar metal planes which are connected to a voltage supply. We neglect the surrounding area by applying zero Neumann boundary conditions at open borders of the capacitor and Dirichlet boundary conditions at the electrodes (assumes an infinitely expanded capacitor). Iso-surfaces of the electrostatic potential inside the plate-capacitor form also coplanar planes which can be used as a measure for the perpendicular distance to the surface (electrodes).

For the description of the metric tensor function, we first calculate the solution of Laplace's equation considering the given Dirichlet boundary conditions on the initial coarse mesh. This approach allows to define in a very flexible way where the refinement should take place. To take anisotropy into account we use the derivative of the electrostatic potential ψ as primary stretching direction for the anisotropic metric description (20). To accomplish this task we first rotate the three axes of the Cartesian coordinate system (*x*-, *y*-, and *z*-axes) so that the *new y*-axis is parallel to the gradient vector $\nabla \psi$.

At the second step we apply a dilation-factorfunction $\lambda_{\eta} = \lambda_{\eta}(\psi)$. So the dilation along the gradient direction depends on the potential ψ . All other stretching weights are set to unity, which guarantees a dilation only along the gradient field. According to (20) the anisotropic metric function is now completely specified over the element. For the three-dimensional simplex partitioning the *anisotropic length* of all tetrahedron edges are calculated under consideration of

$$\ell_{PQ} = \int_0^1 \sqrt{\overline{PQ}^T} \cdot \mathbf{M}(P + t \cdot \overline{PQ}) \cdot \overline{PQ} \, dt. \quad (21)$$

The longest anisotropic edge which transcends the maximum edge length value is chosen as the refinement edge.

5.4 Oxidation

For the oxidation model we use analogously to [96, 97] a normalized silicon concentration $\eta(\vec{x},t) = \frac{C_{Si}(\vec{x},t)}{C_{OSi}}$ where $C_{Si}(\vec{x},t)$ is the silicon concentration at time *t* and point $\vec{x}(x,y,z)$ and C_{OSi} is the concentration in pure silicon. So η is 1 in pure silicon and 0 in pure silicon-dioxide. The oxidant diffusion is described by $D\Delta C(\vec{x},t) = k(\eta)C(\vec{x},t)$. Here *D* is the diffusion coefficient and $k(\eta)$ is the strength of a spatial sink and not just a reaction coefficient at a sharp interface like in the standard model for oxidation [98]. However, $\eta(\vec{x},t)$ varies during oxidation simulation with ascending time, so therefor it is important for the convergence of the model and the quality of the computed solution to increase the spatial resolution near the interface on demand.

The idea is to solve the Laplace equation on the initial coarse mesh with special Dirichlet boundary conditions. Boundary conditions on the upper silicon surface which is exposed to an oxidizing atmosphere are set to unity and the opposite part of the silicon body is set to zero. The solution of the Laplace equation and the corresponding iso-surfaces can be seen in the right part of Figure 26, the initial coarse mesh is shown in the left part. For the refinement post processing step we detect those elements which hold a solution value close to unity, all others are untouched. The orientation of the anisotropy should reflect boundary aligned elements by the mean of short point distances perpendicular to, and long point distances along the oxidizing surface. Observing the gradient field of the solution, c.f. Figure 26(b), reflects the anisotropic compression direction and is therefore a good choice for the anisotropic tensor function.

While performing the simulation we use $\eta(\vec{x},t)$ to identify the interface region and the first derivative of η for our anisotropic refinement. Figure 27(b) shows the resulting mesh at the end of the oxidation simulation caused by applying our strategy. The interface between silicon and silicon dioxide migrates from the upper surface of the initial silicon body downwards. The refinement procedure follows this behavior and thereby a good spatial resolution near the interface is reached. Other regions at the simulation domain are left untouched which guarantees the usage of an almost minimal number of grid points.



(a) Cubic silicon (Si) body with L-shaped silicon nitride (Si_3Ni_4) mask on top. Initial mostly coarse regular mesh.

(b) Iso-surfaces of Laplace's equation solution and according gradient field vectors on initial coarse mesh.

Figure 26: Calculations for anisotropic refinement on the initial coarse mesh.



(a) Highly anisotropic thin mesh layer after Laplace-Refinement in the upper region of the silicon body (input for oxidation).

(b) Anisotropic mesh after oxidation simulation. The refinement procedure followed the moving interface of Si and SiO_2 .

Figure 27: Mesh adaption during oxidation simulation.

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