

EXACT FIRST PRINCIPLES MODELLING OF SHORT-CHANNEL VMOS TRANSISTORS

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1. INTRODUCTION

The application of exact two-dimensional numerical computer models has found wider use during the past few years. As far as we know these models have been totally limited to simple planar structures. Recently VMOS technology has turned out a real challenge to simple planar MOS in the field of large scale static and dynamic memory devices. The use of the third dimension makes it possible to increase circuit complexity up to 64k RAM memory chips.

In this contribution we present a method and some important results of a two-dimensional exact model for VMOS devices. To gain maximum insight into the influence of the technological and the geometrical variations the modelling of both the technology and the electrical behaviour of the devices have been coupled. This has been performed using a one-dimensional process model and a two-dimensional device model.

2. METHOD AND RESULTS

The structures investigated are transistors which are used for one-transistor dynamic memory cells (e.g. (1)). The doping profile of a typical VMOS device before the selective etching process is shown in fig.1. The transistor is made on a p⁺ substrate. The n⁺ buried source is an antimony diffused layer. The channel region is made by p epitaxy. The drain regions are highly phosphorus doped. The doping profile has been calculated with SUPREM I (2) using an improved phosphorus model (3). The computed profiles have been verified by extensive experiments. Anodic oxidation in connection with 4-point sheet resistance and computer-aided 2-point measurements has been used.

To facilitate the electrical characterization of the VMOS device the three-dimensional structure is reduced to two dimensions by rotating the V-groove around the half angle. A simple two-dimensional planar geometry can be constructed as shown by the dashed line in fig. 2. Essential MOS quantities such as channel length L, oxide thickness T_{ox}, and pn-junction depth R_j are also defined. Table 1 lists the complete set of the non-stationary basic semiconductor equations. Heat transfer is included to give complete device simulation at higher current levels. Nearly all of the quantities have their usual meaning. K and ρ are the heat constant and the density of silicon, respectively, c_p denotes the specific heat constant. Table 2 shows the data of the MOS transistors investigated. The drain voltage dependence of the threshold voltage is shown in fig. 3. The substrate to source voltage is taken as a parameter. The squares denote the measured points and the full drawn lines give the computer results. Experimentally the threshold voltage has been determined by the extrapolation method. In the saturation region

we use the square-root technique and in the ohmic range the curves can be simply extrapolated. Numerically the threshold voltage has been found by use of the inversion criterion at the semiconductor surface. Due to the relatively high substrate doping short channel effects become only visible at the most negative substrate voltage of -8V and higher drain bias. At low drain voltages (between 0.1 and 1V) the threshold voltage shows the same dependence on the substrate voltage as simple planar MOS structures. A more accurate study of VMOS devices can be carried out if one looks at the substrate current behaviour. Fig. 4 shows the substrate current of the short channel device depending on the gate voltage. Circles denote computer results. The substrate current has been measured in the bulk lead of the device. Numerically it is calculated by an integration over the hole distribution. In the saturation region the substrate current shows an exponential dependence on the drain voltage according to an avalanche process which has been exactly modelled with the inclusion of the avalanche generation. The curves reach a maximum value and fall down if the device comes back into the ohmic range.

The validity and predictability of our two-dimensional model have been tested with a down scaled VMOS device. An appropriate reduction of junction depths and voltage levels lead to a 4μx4μ VMOS pyramid element. A design based on this device could realize a 256k RAM. Due to the lack of space only two results can be given here.

Fig. 5 shows the behaviour of the carrier densities when the device is switched from deep inversion to accumulation. Fig. 6 depicts the isothermal lines in the device for a high current situation. The maximum internal temperature is calculated to be about 415K at the boundary between channel region and pinch-off area.

3. CONCLUSIONS

The static and dynamic behaviour of short channel VMOS devices of a 64k RAM is simulated estimating the influence of technological and geometrical variations. Theory and experiment agree well for all operating conditions down to 0.7μm channel length. Short channel devices in the limit of punch-through and avalanche conditions are characterized with an error smaller than 30 percent.

In the same way a down scaled VMOS transistor is simulated. Appropriate reduction of geometrical dimensions and voltage levels leads to a 4μx4μ VMOS element. A design based on this device could realize a 256k RAM.

4. REFERENCES

1. Hoffmann, K., et al., 1978, ISSCC San Francisco, paper THPM 12.6.
2. Antoniadis, D.A., et al., 1977, SEL-Report 77-006, Stanford University.
3. Fair, R.E., 1978, J.Electrochem.Soc.125, 323.

TABLE 1 - Basic Equations

Poisson Equation: $\nabla^2 \psi = -\frac{q}{\epsilon}(p-n+C)$

Continuity Equations: $\nabla \cdot J_p = -q(R-G + \frac{\partial p}{\partial t})$
 $\nabla \cdot J_n = q(R-G + \frac{\partial n}{\partial t})$

Heat Transfer: $\nabla \cdot (KV.T) = -Q + \rho c_p \frac{\partial T}{\partial t}$

TABLE 2 - VMOS transistor data

p ⁺ substrate doping	10 ¹⁸ cm ⁻³
n ⁺ buried source	70 ohm/square
p epitaxy	1.5x10 ¹⁶ cm ⁻³
n ⁺ drain	15 ohm/square
oxide thickness	550 Å
epilayer thickness	4µm
source thickness	2.5µm
drain junction depth	1.3µm
channel length	1.6µm
channel width	10µm (5µm pyramid)
mobility	120cm ² /Vsec

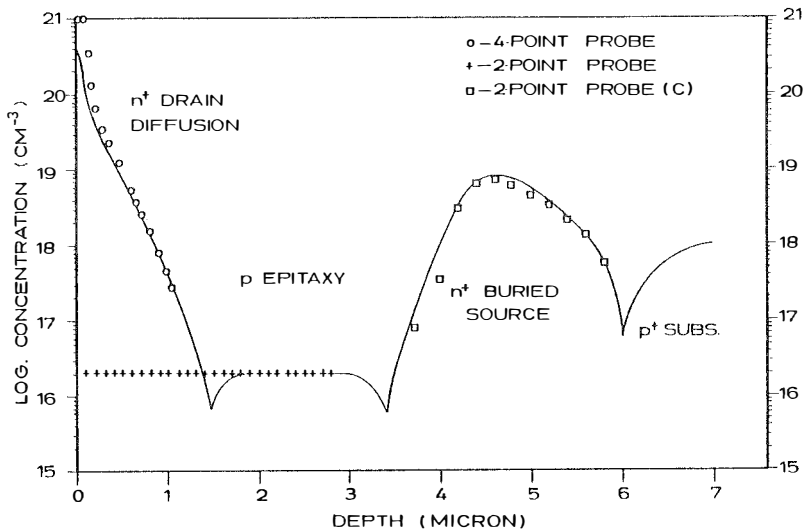


Fig. 1: Doping profile of a VMOS transistor before etching. (o) 4-point probe, (+) 2-point probe, (□) computer corrected 2-point probe, (-) SUPREM I.

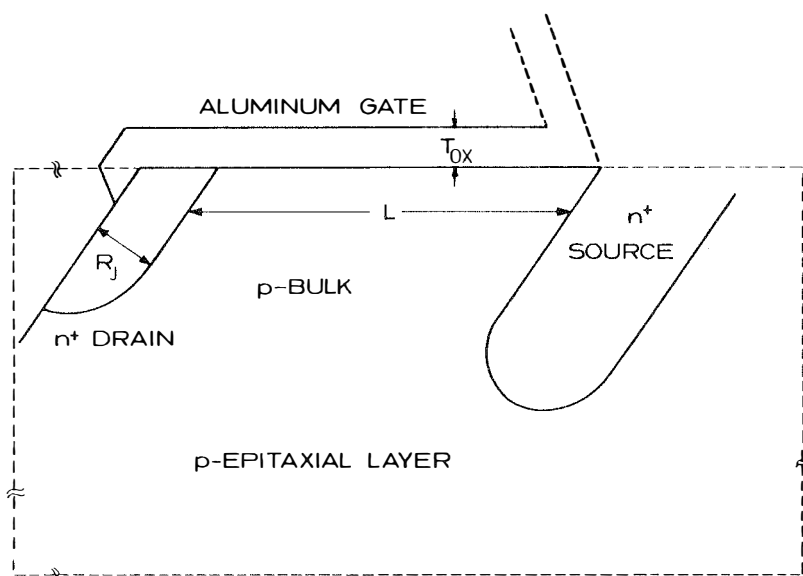


Fig. 2: Two-dimensional cross section of a typical VMOS device with a floating source. The dashed lines show the planar generalization used in the numerical computations.

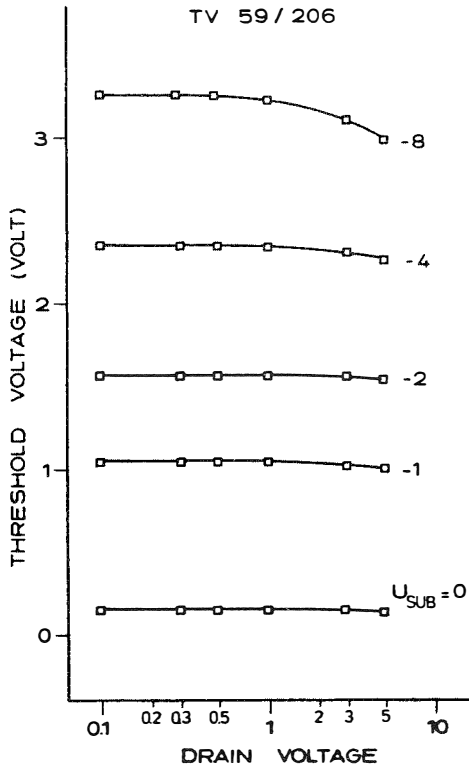


Fig. 3: Threshold voltage behaviour in dependence of drain voltage and substrate voltage. (\square) theory, (\circ) experiment.

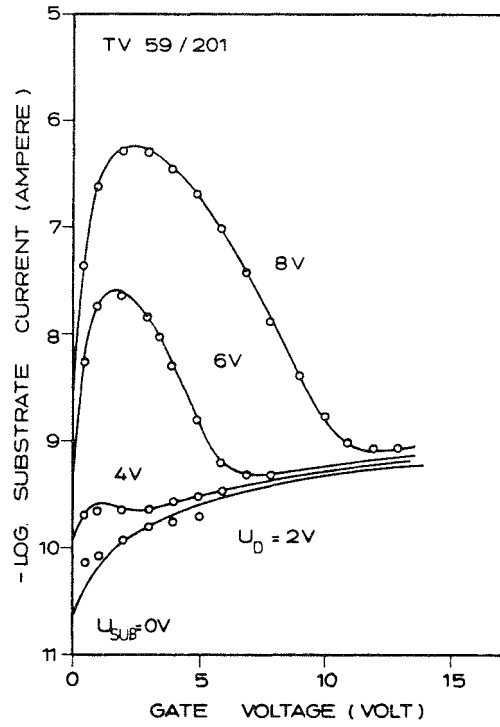


Fig. 4: Substrate current in dependence on gate voltage with drain bias as a parameter. (\circ) theory, (\square) experiment

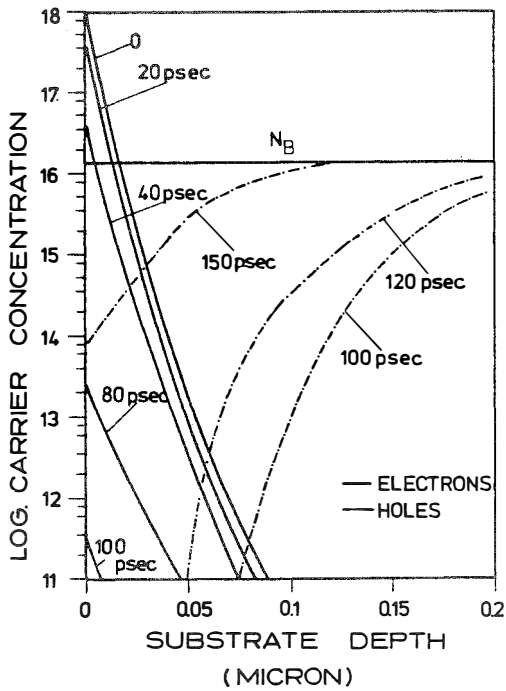


Fig. 5: Behaviour of carrier densities during switch-off conditions. (—) electrons, (---) holes, $U_G(t=0) = 2V$, pulse height $-2V$, rise time 100 psec.

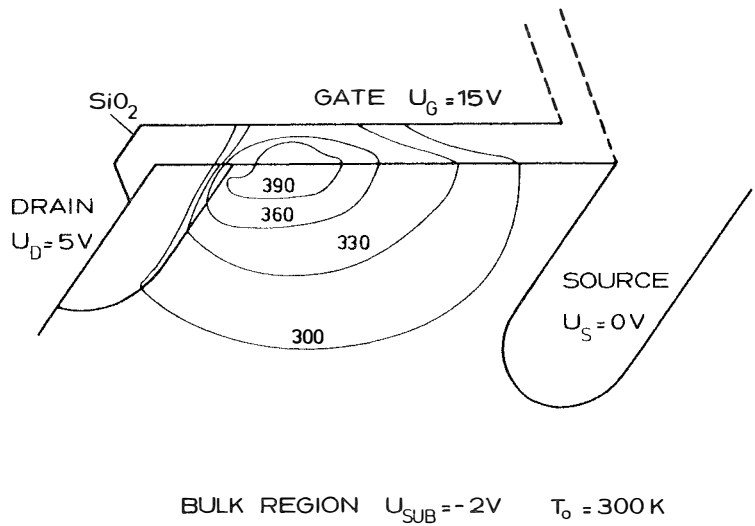


Fig. 6: Isothermal lines at $U_G = 15V$, $U_D = 5V$, $U_{SUB} = -2V$.