Numerical 2-D Simulation of Vertical Power MOSFET's

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The area of applications for power MOSFETs has steadily increased in spite of the fact that these devices appeared on the market only a few years ago. Their greatest advantages over bipolar power devices involve their fast switching capability and the presence of a well defined safe operating area, which stems from the lack of second breakdown. This broadening of application requires not only to measure the devices but also to simulate their performance with numerical tools. To help tackling this problem, the program-system BAMBI (=Basic Analyzer of MOS and BIpolar devices) has been developed to analyze arbitrarily shaped devices using new simulation techniques which are published in /1/.

BAMBI has been succesfully applied for the simulation of DMOS power transistors. The device, which has been analyzed for this contribution, has a channel length of 2 um, an epilayer of 12 um, an oxide thickness of 800A and a total simulated device thickness of 20 um. The epilayer doping is 1.5E15/cm^3, the channel surface p-doping is approximately 5E16/cm^3. The doping profile has been simulated numerically by SUPREM /2/ in one dimension and extended analytically to two dimensions.

The results which will be presented encompass three different ranges of the IV-characteristic : the subthreshold region, the resistance region and the saturation region. The main differences between those regions can be explained with regard to electron distributions. The subthreshold region is characterized by the space charge area throughout the whole epilayer. In the resistance region, the accumulation-layer at the Si/SiO2 interface allows for a homogenous current flux towards the substrate. By increasing the drain voltage and therefore approaching the saturation region, the space charge region underneath the middle of the gate-contact is enlarged. The electrons from the channel towards the drain contact are squeezed into a very narrow band with high current densities. In comparing the measured current values to the calculated ones, satisfactory agreement can be remarked.

/1/ A.F.Franz et.al, IEEE Trans.Electron Devices, Vol.ED-30, pp.1070-1082, (1983).

/2/ D.A.Antoniadis et.al, Report 5019-2, Stanford University (1978).