wide array of advanced development and production techniques using photooptics, electrons, and X-rays as energy sources for pattern generation and relication. Over the past 3-4 yr a new technique, focused ion beam lithography, has emerged as a challenger to these lithography tools for very large-scale integration (VLSI) research and production applications. A number of significant advantages exist when using focused beams in mincroelectronic fabrication that are not available in the technologies mentioned above. For example, the focused ion beam (FIB) may allow manufacturers to eliminate many of the process steps associated with conventional implantation since FIB implants can be performed without lithography and chemical processes. Special implant steps can also be done that are neither practical nor even possible with conventional photomasking techniques.

Ion Beam resists.
JOHN E. JENSEN
Solid St. Technol. 145 (June 1984)
Conventional organic polymenr resist exhibit sensitivity enhancements of from one to more than two orders of magnitude when exposed to ions compared to electrons. This is due to the difference in energy deposition in the resist material with ions. Additionally, higher resolution can be expected for ion exposed images due to the shorter range of secondary electrons generated in the energy deposition process. Current ion-beam technologies utilize finely focused ion-beams, large area ion-beams with masks, and ion-beam images that are demagnified and focused on the wafer surface. Because of the variety of ions and accelerating energies available there is a greater selection of materials that can be used with ion exposure systems. The interaction of ions with organic polymers and several resist applications is discussed.

Reactive ion etching: its basis and future. Part II.
D. BOLLINGER, D. LIDA and O. MATSUMOTO
Solid St. Technol. 167 (June 1984)
The characteristic ability of Reactive Ion Etching (RIE) is its use of controlled, energetic ion bombardment to assist in chemically reactive etch processes. Etch mechanisms in RIE are to some degree common to all present production dry etch processes. The role of ion bombardment is a key factor in determining which etch mechanism will dominate. Process parameters, along with the gas chemistry used are directly and predicatbly related to the etch characteristics attainable. Automated RIE systems are now proving their capabilities in high throughput production. The most demanding of the production etch applications, such as that of the Al/Si/Cu alloys, are being solved and process capabilities are being continually developed to meet new etch requirements.

Evaporated As_2S_3 - reproduction fidelity for microlectronics.
B. MEDNIKAROV
Solid St. Technol. 177 (May 1984)
The possibilities for reproducing details in the one micron and submicron regions and the processing latitude of a new evaporated As^2S_3 photoresist are discussed. The stability of the evaporated photoresist in oxidizing solutions used for etching the chromium layer is demonstrated. Other advantages of the new photosensitive system and its applications are also discussed.

Corrosion protection for semiconductor packaging
KARL W. ROSENGARTH, Jr.
Solid St. Technol. 191 (June 1984)
Corrosion of ASTM F-15 alloy (29 Ni, 17 Co, 54 Fe) and 42 alloy (Fe, 42 Ni) semiconductor packaging alloy was studied in both aqueous chloride and liquid metal environments. Stress corrosion cracking (SCC) of F-15 alloy and 42 alloy occurred in the aqueous chloride environment. Temperature and chloride concentration each had a significant influence on the SCC behaviour. Additionally, intergranular liquid metal corrosion was discovered during silver-copper eutectic (Ag, 28 Cu) brazing experiments. The performance and reliability of semiconductor devices packages under actual service conditions are discussed with respect to protective coatings of electroplated nickel and hot dipped solder (Sn, 40 Pb) coatings.

Process and device modelling for VLSI.
S. SELBERHERR
Microelectron. Reliab. **24**, 225 (1984)
The appearance of very large scale integration caused a pronounced interest in concentrating on process and device modeling. The fundamental properties which represent the basis for all device modeling activities are summarized. The sensible use of physical and technological parameters is discussed and the most important physical phenomena which are required to be taken into account are scrutinized. The assumptions necessary for finding a reasonable trade-off between efficiency and effort for a model synthesis are recollected. Methods to bypass limitations induced by these assumptions are pin-pointed. Formulae that are applicable in a simple and easy way for the physical parameters of major importance are presented. The necessity of a careful parameter-selection, based on physical information, is shown. Some glimpses on the numerical solution of the semiconductor equations are given. The discretisation of the partial differential equations with finite differences is outlined. Linearisation methods and alogrithms for the solution of large sparse linear systems are sketched. Results of our two dimensional MOSFET model reached a complexity level of more than one hundred thousand devices per chip will require more interconnects per unit silicon area and higher current density capabilities. Examples include high performance macrocell arrays which are already industry standard with three-level metallization. Requirements to improve autorouter performance, as well as to increase the efficiency of silicon area usage, will soon increase the number of levels to four. Factors in this increasing density and number of levels of interconnects include the choice of contact and conductor metals, deposition conditions, patterning techniques, and insulator technology. The latter's constituents include material selection, via definition and planarizing proper-

ties. Inherent in all technology segments is the reliability aspect. Some device structures, process options, and some equipment implications will be discussed.

XPS analysis of (100) GaAs surfaces after applying a variety of technology-etchants.
E. HUBER and H.L. HARTNAGEL
Solid St. Electron. **27,** 589 (1984)
XPS measurements were undertaken on differently treated (100) GaAs surfaces using $2p_{3\,2}$ and 3d core level peaks of As and Ga and the 1s level peak of 0. The $2p_{3\,2}$ level peaks are more sensitive to the direct surface composition while the 3d peaks reflect the more bulk-like composition. It was found that 0 is bonded to surface As atoms in NaOH + H_2O_2 etched samples, while in HCl etched samples 0 is probably bonded to defects produced by the formation of Ga-O bonds. Depth profiles obtained by sputtering show a deplation of both Ga and As in the surface region. The depletion of Ga, however, is much more obvious in the HCl treated samples compared to NaOH + H_2O_2 treated samples. In interpretation of depth profiles obtained by sputtering one has to be aware of sputtering artifacts demonstrated also in this paper.

Profile control in plasma etching of SiO_2.
R.N. CASTELLANO
Solid St. Technol. 203 (May 1984)
Sloped profiles of SiO_2 contact windows are necessary in order to achieve good step coverage and minimize microcracks in vacuum deposited metal films. One method for achieving sloped profiles utilizes controlled photoresist erosion by the incorporation of oxygen into the process mixture. As the ratio of etch rates of oxide to resist approaches one, the profile of the resist (sloped by high temperature baking) is reproduced in the oxide. At high oxide etch rates, vertical etching of the oxide proceeds at a faster rate than that of the lateral erosion of the resist so that vertical profiles result. Experiments directed at achieving sloped profiles and high SiO_2 (Si selectivities with C_2F_6, CHF_3, He and O_2 are described.

Diffusion, ion implantation and annealing
PIETER S. BURGGRAAF
Semiconductor Int. 100 (November 1983)
Equipment for semiconductor doping processes and associated annealing operations were enhanced this year to enable the fabrication of higher density VLSI ICs.

Sources of failures and yield improvement for VLSI and reconstructable interconnects for RVLSI and WSI: Part I - sources of failures and yield improvements for VLSI.
TULIN ERDIM MANGIR
Proc. IEEE **72,** 690 (June 1984)
Redundancy of both logic circuits and interconnections is the core principle of both RVLS (Reconstructable or Fault-Tolerant VLSI) and WSI (Wafer Scale Integration). For varying complexity and size of circuits different factors of redundancy are required. Effective use of redundancy requires understanding of the failures and failure modes at different stages of the processing and lifetime of VLSI and WSI circuits.

This paper consists of two parts. In Part I, sources of failures for MOS devices are discussed. Manifestations of physical failures are described. Use of redundancy for the yield improvement of VLSI circuits is explored through the use of a mathematical model. It is shown that interconnection density and pattern complexities around each section determines the effectiveness of yield improvement. In Part II (to be published in a forthcoming issue), programmable interconnect technologies are described to facilitate restructuring of VLSI and WSI circuits, in this case as they apply to yield improvement through the use of redundancy.

10. Testing

Measurement technique of electromigration.
Y.Z. LU and Y.C. CHENG
Microelectron. Reliab. **23,** 1103 (1983)
In view of a series of advantages of the resistometric technique there have been more and more reports applying this technique to conduct research in electromigration in different material thin films. However, to our knowledge, few papers have been published so far in which the resistometric technique itself has been discussed in detail so as to facilitate an application in the study of reliability in integrated circuits. This paper summed up our experience in using this technique to carry our research in the electromigration phenomena in thin aluminium films and reported our measured results of electromigration parameters of this film. Comparing with other investigators', we found that our results were in agreement with the literature.

Properties of nickel oxide films grown by sputter oxidation.
NARUMI INOUE and YOSHIZUMI YASUOKA
Vacuum **34,** 687 (1984)
Thin nickel oxide layers grown on nickel films by sputter-oxidation in an oxygen plasma were studied by ellipsometry and ionmicro analysis. It was found that the steady-state oxide thickness depends on the oxygen pressure. For oxygen pressure of (4.5-5.3) x 10^{-4} Pa, the steady-state oxide thickness was found to be 70-90 A by ellipsometry. This result was supported by the IMA measurement.

Replica electron microscopy of the nickel oxide layer indicated that the oxide, grown in the oxygen pressure of (4.5-5.3) x 10^{-4} Pa, had uniform distribution. However the oxide films grown in 7.5 x 10^{-4} Pa had many cracks.

Investigation of fretting corrosion at dissimilar metal interfaces in socketed IC device applications.
JOHN J. MOTTINE and BARBARA T. REAGOR
IEEE Trans Components Hybrids Mfg Technol. **CHMT-7,** 61 (March 1984)
Gold has traditionally been the material of choice for separable connector contact surfaces in high reliability applications. With the rising cost of gold, major efforts