

Two-Dimensional Transient Simulation of the Turn-On Behavior of a planar MOS Transistor

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Abstract – The paper presents results of a fully two-dimensional transient analysis of the behavior of a MOS Transistor with 5V applied to the Drain, if the gate is pulsed from -0.3V to 7V within 50ps. With four selected snapshots the development of all interesting quantities (i.e.: electrons, holes, electrostatic potential, electric field, electron current density, and hole current density) is shown. Finally the calculated contact currents are plotted as a function of time describing the development of the negative channel-charge and the charge pumping effect, caused by the rapid gate-voltage ramp.

1. Introduction

The switching behavior of MOS transistors is of considerable interest because of a wealth of work aimed at the increase of integrated circuit switching speeds.

In addition there have been successful attempts to use MOS transistors as special emitter shorts in thyristors, the so called MCT (MOS Controlled Thyristor)[1,2]. This technology makes it possible to drive the gate of that power device with a voltage pulse, which is more easy to handle than the long current pulse necessary for switching traditional thyristors and GTO thyristors. As the properties of all these applications are mainly defined by the switching MOS transistor, the switching behavior of that device is of great interest for designers of above mentioned structures.

Therefore many transient analyses and analytical models have been published, that describe and explain what happens during the switching process of MOS transistors.[3,4,5] These publications deal with transistors with long channel lengths or work out one dimensional models which loose validity for channel length shorter than $3\mu\text{m}$.

The aim of this paper is to illustrate the switching process of a realistic short channel device. The simulated structure is a NMOS transistor with oxide thickness of $d_{ox} = 250\text{\AA}$, a channel length of $L_{eff} = 0.8\mu\text{m}$, a channel doping under the oxide of $N_a = 1.10^{17}\text{cm}^{-3}$ and substrate doping $N_a = 6.10^{15}\text{cm}^{-3}$. The doping profile of the channel region is given by Fig. 1. This doping profile is modeled by means of analytic functions as described by Selberherr[6]. A deep channel implantation was not necessary because no punch-through effect occurs at the voltage levels we have used.

DOPING PROFILE (CM**3)

$V_g = 0\text{ V}$ $V_d = 0\text{ VOLT}$

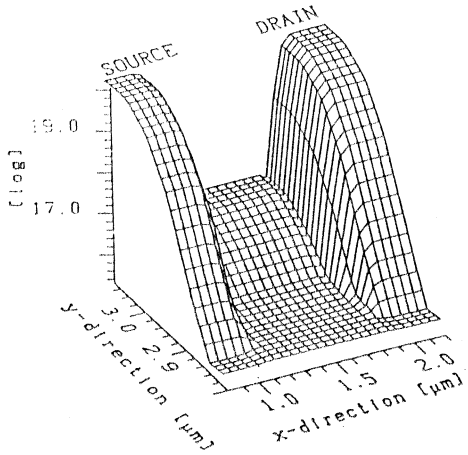


Fig. 1

Our simulations have been performed by the two-dimensional transient device simulator BAMBI[7], which solves the three basic semiconductor equations utilizing a 'Finite Boxes' discretization[8]. The results are based on a totally selfconsistent solution.

2. Channel Charge

In Fig.2-9 the history of the electrons and the holes in the channel region is shown. The four selected snapshots are 0ps (steady-state), 30ps, 50ps and 70ps at which it should be mentioned that the gate-voltage ramp starts to rise after 20ps. At the steady-state bias-point with -0.3V both electrons (Fig. 2) and holes (Fig. 3) have nearly their equilibrium distribution. By the rise of the electron- and the decrease of the hole concentration in x-direction, the space-charge region on the drain side, caused by the high drainvoltage, can nicely be seen. As the concentration of the acceptors decreases deeper in the bulk, the space-charge region becomes wider. Directly under the gate a small accumulation of holes can be recognized near drain in the space-charge region.

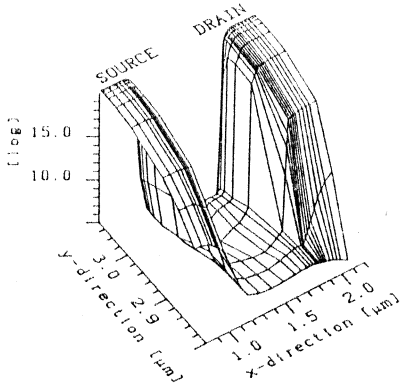
ELECTRON CONCENTRATION (CM^{**3}) $T = 0$ NS $UG = -0.3$ VOLT

Fig. 2

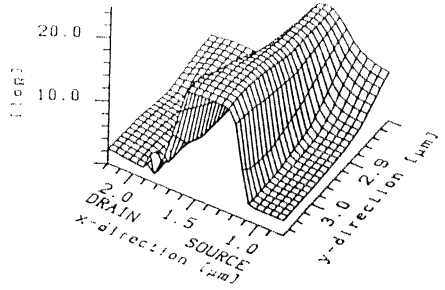
HOLE CONCENTRATION (CM^{**3}) $T = 0$ pS $UG = -0.3$ VOLT

Fig. 3

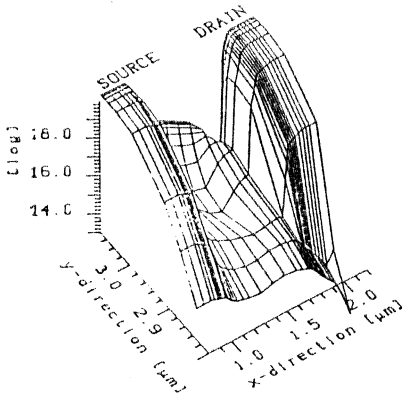
ELECTRON CONCENTRATION (CM^{**3}) $T = 30$ pS $UG = 1.16$ VOLT

Fig. 4

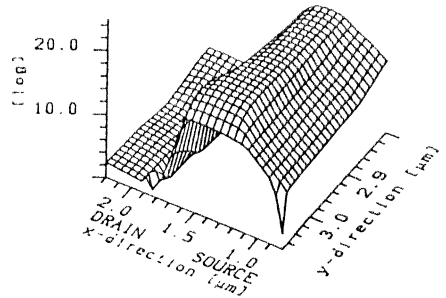
HOLE CONCENTRATION (CM^{**3}) $T = 30$ pS $UG = 1.16$ VOLT

Fig. 5

Not more than 10ps later (at 30ps simulation time) the electron concentration has risen significantly, the inversion layer has already started building up from source(Fig. 4) and the holes slowly flow back into the bulk(Fig. 5). On the drain side the pn junction is still reverse biased so that neither electrons nor holes can pass. On the source side the junction barrier has been significantly reduced and the enhancement in hole concentration indicates weak injection.

ELECTRON CONCENTRATION (CM^{*x-3}) HOLE CONCENTRATION (CM^{*x-3})
 $T = 50 \text{ pS}$ $UG = 4.08 \text{ VOLT}$ $T = 50 \text{ pS}$ $UG = 4.08 \text{ VOLT}$

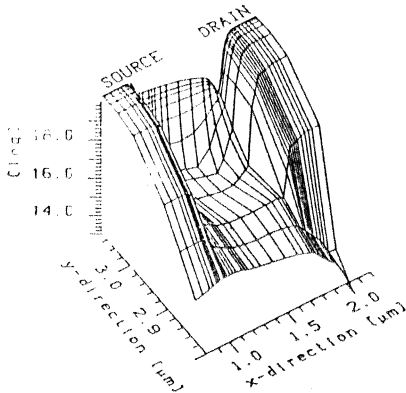


Fig. 6

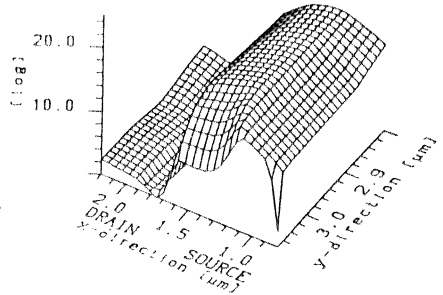


Fig. 7

This process continues and another 20ps later (at 50ps simulation time) the channel is nearly completely built up, besides a small pinch-off region, under which the field, still showing in negative x-direction, causes a slight increase of electrons near drain (Fig. 6). The hole depletion under the surface advances slowly (Fig. 7).

ELECTRON DENSITIES (CM^{*x-3}) HOLE DENSITIES (CM^{*x-3})
 $T = 70 \text{ pS}$ $UG = 7. \text{ VOLT}$ $T = 70 \text{ pS}$ $UG = 7. \text{ VOLT}$

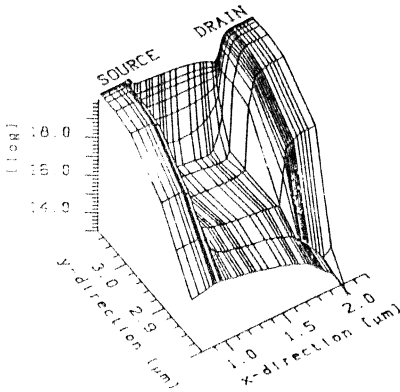


Fig. 8

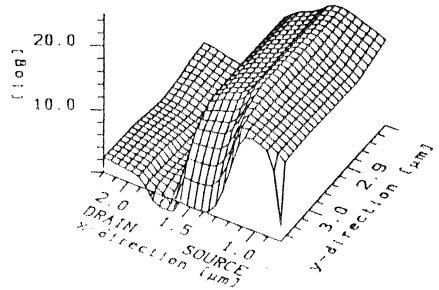


Fig. 9

The gate voltage has reached its final value of 7V after 50ps (at 70ps simulation time) and Fig. 8 shows that the electrons have already reached their final distribution. As the gate voltage is high enough for the device operating in the ohmic region of the current-voltage characteristic, the pinch off has completely vanished, although the level of the inversion layer is lower near drain what can be explained by the lower inversion field on this side (Fig. 15,16). The area under the surface is completely depleted from holes(Fig. 9) but the holes have not yet reached their steady state distribution. Deeper in the bulk the depletion procedure carries on after the switching of the gate voltage. This is verified by the behavior of the current out of the bulk contact.

3. Potential

The potential distribution of the steady-state bias point is determined by the two space-charge regions (Fig. 10),because a curvature of potential distribution can only occur in regions with existing charge. Again it can be recognized that on drain side the space-charge region expands deeper into the bulk. As the electrons accumulate the potential continuously rises with time, especially at the oxide interface, until its final value is reached(Fig. 11). Due to the high negative charge (electrons and acceptors) the potential now is positively bent in x- and y-direction in the whole channel region.

POTENTIAL (V)

$T = 0 \text{ pS} \quad U_G = -0.3 \text{ VOLT}$

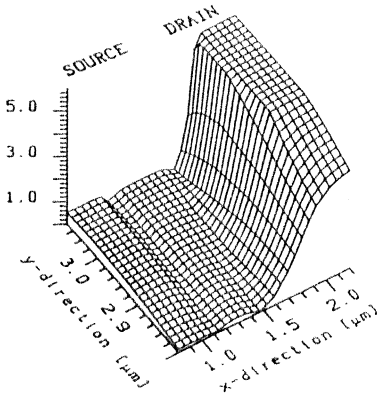


Fig. 10

POTENTIAL (V)

$T = 70. \text{pS} \quad U_G = 7. \text{VOLT}$

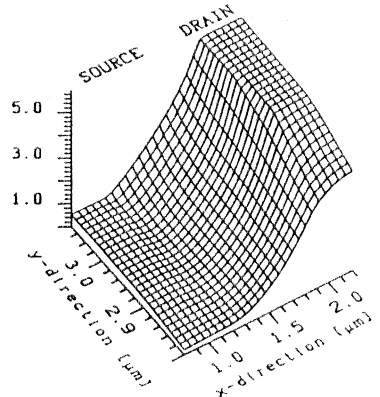


Fig. 11

ELECTRIC FIELD MODULUS (V/CM)

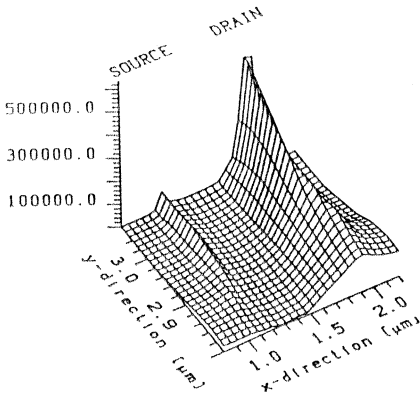
 $T = 0 \text{ pS}$ $U_G = -0.3 \text{ VOLT}$ 

Fig. 12

ELECTRIC FIELD MODULUS (V/CM)

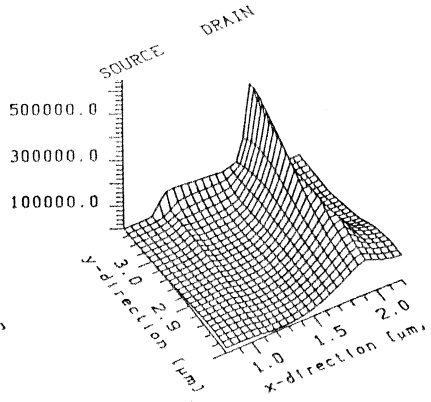
 $T = 30 \text{ pS}$ $U_G = 1.16 \text{ VOLT}$ 

Fig. 13

4. Electric Field

There is a high peak of the electric field near drain caused by the high drain voltage and the short extension of the space-charge region (Fig. 12). After the first time step (10ps) the peak is reduced and, on the other hand, an inversion field starts to build up under the gate (Fig. 13). As the space-charge region on source side has nearly vanished the field is very low and the potential barrier for the carrier densities has been reduced.

ELECTRIC FIELD (V/CM)

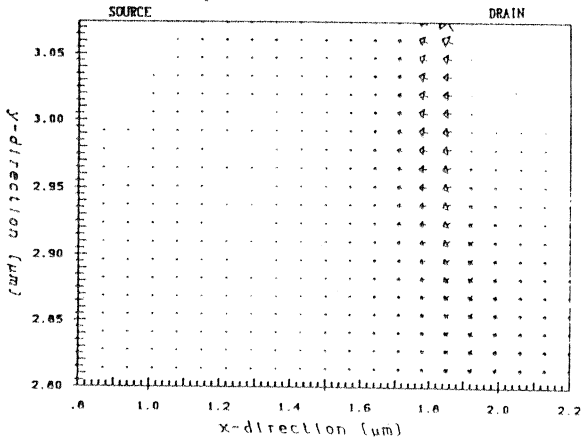
 $T = 30 \text{ pS}$ $U_G = 1.16 \text{ VOLT}$ 

Fig. 14

ELECTRIC FIELD MODULUS (V/CM)

$$T = 70 \text{ pS} \quad U_G = 7. \text{ VOLT}$$

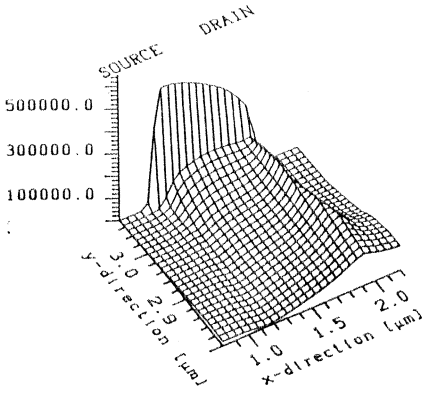


Fig. 15

Since the device is still in pinch-off condition the field has a strong component in the positive y -direction near the drain (Fig. 14). Fig. 15 shows the high inversion field directly at the silicon surface after 50ps (at 70ps simulation time) with its maximum near source due to the high potential difference between gate- and source contact. In Fig. 16 we see that the field shows into negative y -direction over the whole length of the oxide interface and the x -component on the drain side is significantly reduced compared to earlier instants of time (Fig. 16).

ELECTRIC FIELD (V/CM)

$$T = 70. \text{ pS} \quad U_G = 7. \text{ VOLT}$$

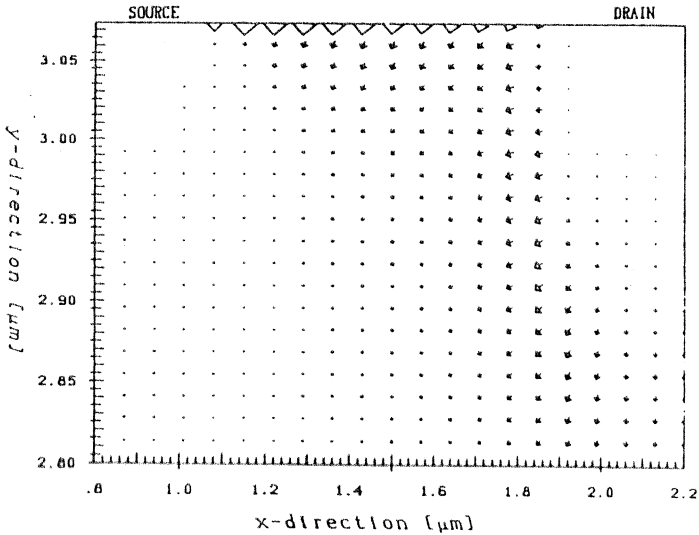


Fig. 16

5. Current Density of Electrons

*CURRENT DENS. ELECTRONS (MOD.) (A/CM**2)*

The figures of the electron $T = 30. \text{pS}$ $UG = 1.16 \text{VOLT}$ current density prove that the development of the channel starts from source only, because of the blocking pn-junction to drain. The current density has a sign reversal exactly at the junction (Fig. 17) i.e. it changes its direction there (Fig. 18). As the inversion layer keeps growing the electrons start to pass the junction and to flow into the drain area.

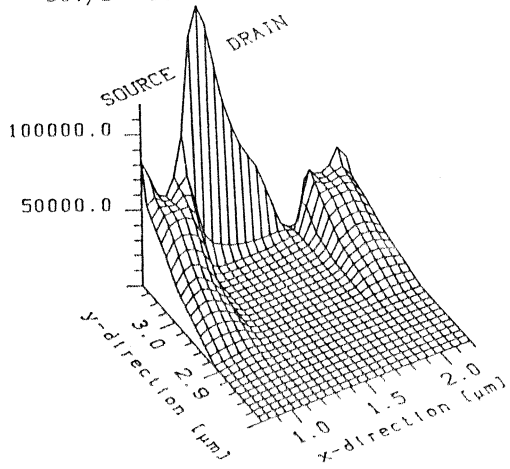


Fig. 17

*CURRENT DENS. ELECTRONS (A/CM**2)*

$T = 30. \text{pS}$ $UG = 1.16 \text{VOLT}$

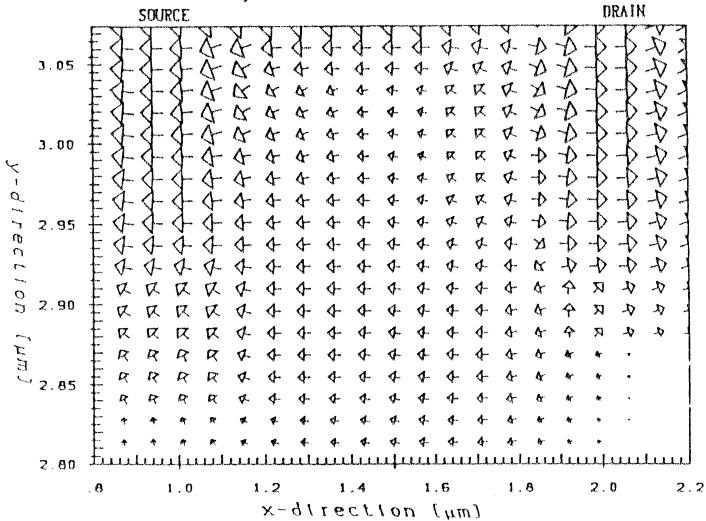


Fig. 18

CURRENT DENS. ELECTRONS (MOD.) (A/CM**2)

$T = 70. \text{pS}$ $UG = 7. \text{ VOLT}$

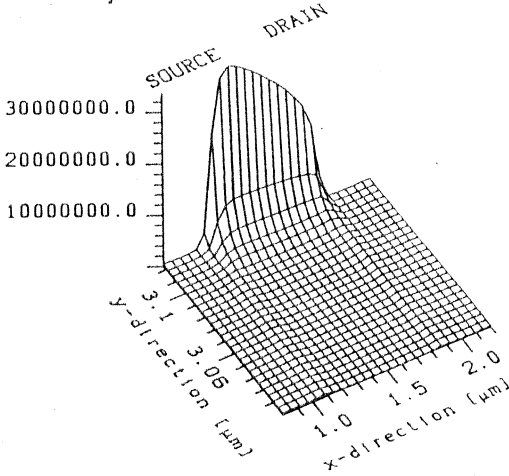


Fig. 19

The current density rises dramatically (Fig. 19) and shows a maximum near source. The direction of the field (Fig. 16) forces the electrons to flow towards the surface causing an accumulation of the current density (Fig. 20).

CURRENT DENS. ELECTRONS (A/CM**2)

$T = 70. \text{pS}$ $UG = 7. \text{ VOLT}$

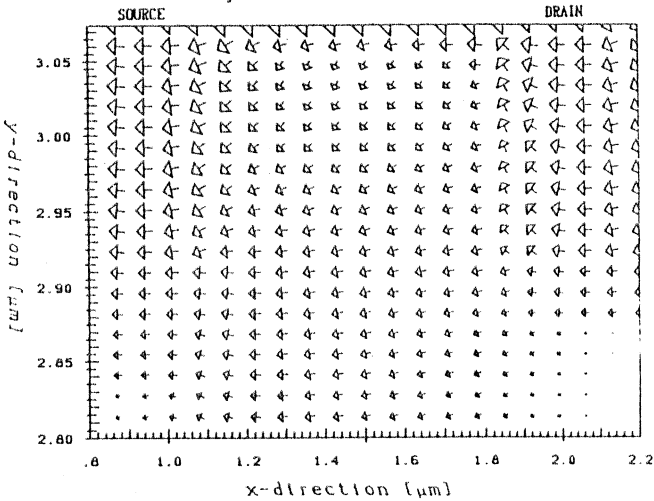


Fig. 20

6. Current Density of Holes

The hole current density flows from the silicon surface back into the bulk to the bulk contact due to the growth of the depletion region under the oxide (Fig. 21). The direction of the current density is similar to that of the electric field in the region between source and drain (Fig. 16). Evidently the current density shifts back deeper into the bulk since the extension of the depletion region increases (Fig. 22), until a small current path results, that slowly depletes the hole region between source and drain (Fig. 23). As the space-charge region on the drain side is already depleted from holes, all figures show that the current only flows in that part of the region being closer to source.

*CURRENT DENS. HOLES (A/CM**2)*

T = 30. pS UG = 1.16VOLT

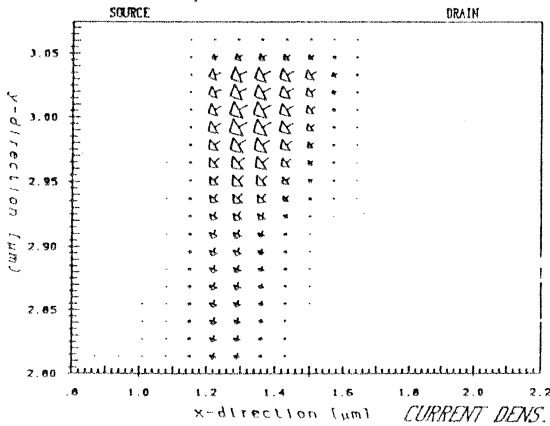


Fig. 21

*CURRENT DENS. HOLES (A/CM**2)*

T = 50. pS UG = 4.08VOLT

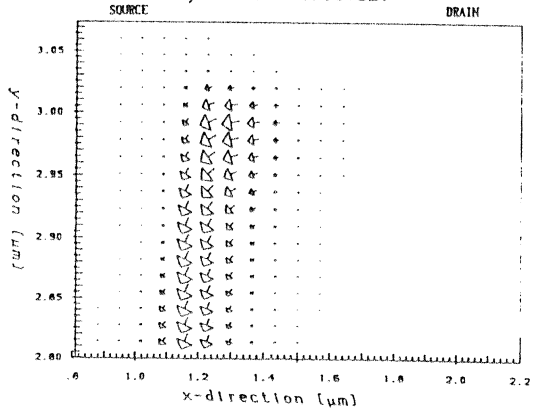
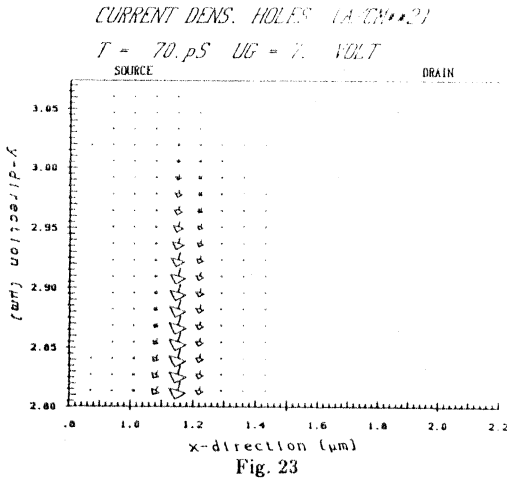


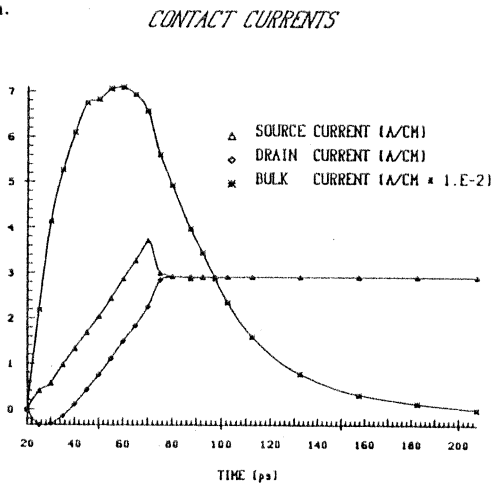
Fig. 22



7. Contact Currents

The curves of the contact currents (Fig. 24) show the predicted transient behavior [3,5]. Source and bulk current flow out of the device, whereas drain current starts flowing out of the device too but changes sign after a delay of $\tau_d=18\text{ps}$ due to the transit time of the channel charge. The transient difference between source- and drain current is caused by the erection of the storage charge in the channel region.

channel region.



The bulk current strongly rises due to its capacitive behavior, reaches its maximum shortly before the gate voltage reaches its final value and decreases then slowly until the holes reach their steady-state distribution.

8. Conclusions

Our simulation showed that the channel charge easily can follow the steep gate-voltage ramp whereas the reaction of the holes and the response of the bulk current has a significantly higher time constant. Furthermore it should be pointed out that the amount of negative charge stored in the region under the inversion layer between source and gate is not negligible and the prediction is justified that the turn off behavior will be dominated by its destruction by recombination. This fact has already been proved by our two-dimensional transient simulation of the turn-off behavior the results of which will be published soon. The switching behavior of short channel devices is a two dimensional phenomenon which cannot be sufficiently described by one-dimensional models.

9. Acknowledgements

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References:

- [1] M.STOISIEK, H.STRACK, MOS GTO- A Turn Off Thyristor with MOS-Controlled Emitter Shorts, in IEDM Tech.Dig., p.185, 1985
- [2] V.A.K.TEMPLE, MOS-Contolled Thyristors-A New Class of Power Devices in IEDM Tech.Dig., p.282, 1984
- [3] SOO-YOUNG OH, D.E.WARD, R.W.DUTTON
Transient Analyses of MOS Transistors
in IEEE Trans. on Electr.Dev., Vol. ED-27, No.8, Aug.80
- [4] M.E.ZAHN, Calculation of the Turn On Behavior of MOST
in Solid-State Electr.,1974,Vol.17,pp.843-854
- [5] K.GOSER Einschaltzeiten und Umladungsvorgänge bei MOS-Transistoren
in AEÜ, Band 24, 1970, Heft 1
- [6] S.SELBERHERR, Analysis and Simulation of Semiconductor Devices,
Springer-Verlag 1984
- [7] A.F.FRANZ, G.A.FRANZ, BAMBI-A Design Model for Power MOSFET's
in IEEE Trans. on CAD, Vol.Cad-4, No.3, July 85, p.177
- [8] A.F.FRANZ, G.A.FRANZ, S.SELBERHERR, CH.RINGHOFER, P.MARKOWICH
Finite Boxes-A Generalization of the Finite-Differences Method Suitable for
Semiconductor Device Simulation
in IEEE Trans.on Electr.Dev., Vol. ED-30, No.9, Sept 83