Punch-Through in Resurf Devices

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Abstract — A two-dimensional analysis of punch-through effects in high voltage lateral DMOS transistors is presented. The behaviour of these devices has been investigated for various doping concentrations. For one doping profile punch-through occurs between 6V and 60V drain voltage depending on the gate voltage, for the other doping profile no parasitic channel is built up even at 100V drain voltage. Furthermore, it is shown that the parasitic channel does not influence the switching behaviour in a critical way. These two-dimensional effects cannot be explained by approximations from one-dimensional models.

1. Introduction

In recent years various CMOS structures have been developed using lateral DMOS transistors as output driver devices ([1]). Especially for high voltage applications the proper design of these so called resurf devices is of particular importance.
There is a considerable number of publications about threshold voltage (e.g. [2]) and breakdown behaviour (e.g. [3], [4]) of DMOS transistors comparing experimental data with results from simulations and introducing refined formulae for the numerical approximation of various properties of these devices. Only few articles ([2], [5]) deal with punch-through effects at the npn-junction under the gate contact. Furthermore, in [5] very little numerical data are provided and in [6] the effect is presented as a result of impact ionization exactly in the channel.
The aim of this paper is to show, that punch-through at the npn-junction may also occur for doping concentrations as they are reported ([1]), even if the influence of impact ionization is neglected. It should be pointed out, that the presented results cannot be confirmed by approximations from one-dimensional theories. This punch-through is a two-dimensional effect and therefore requires fully two-dimensional simulations.

Our simulations have been performed by the two-dimensional transient device simulator BAMBI, which solves the three basic semiconductor equations utilizing a 'Finite Boxes' [6] discretization. The results are based on a totally selfconsistent solution.

The geometry of the lateral DMOS transistor presented in this paper is taken from [3]. It is shown in Fig.(1): an n-channel device with about 2μm channel length, oxide thickness 0.2μm and a large drift region in order to increase the breakdown voltage.

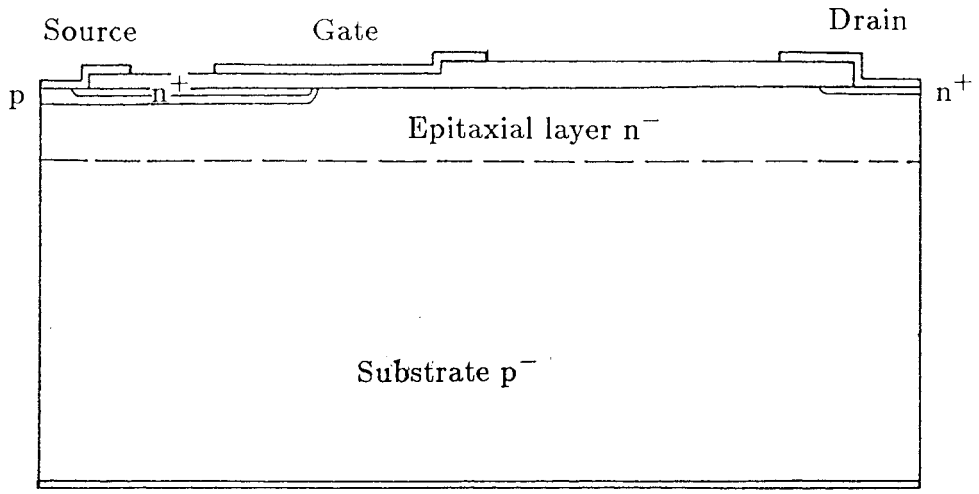

Fig.(1) Geometry

2. Punch-through in OFF-condition

For our investigations of punch-through at the npn-junction under the gate contact we assumed a substrate doping concentration of $1.2 \cdot 10^{15}$ cm^{-3} and an epitaxial doping concentration of $3.0 \cdot 10^{15}$ cm^{-3}. In Fig.(2) this doping profile is drawn, in Fig.(3) a section of the npn-junction can be seen. The profiles are approximated by Gaussian distribution functions.

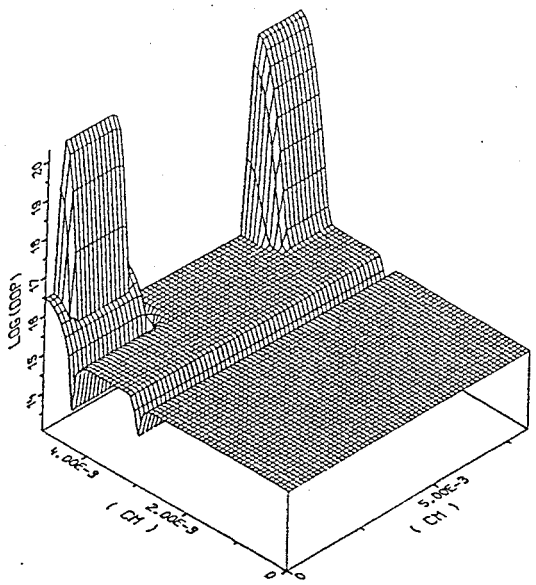

Fig.(2) Doping concentration

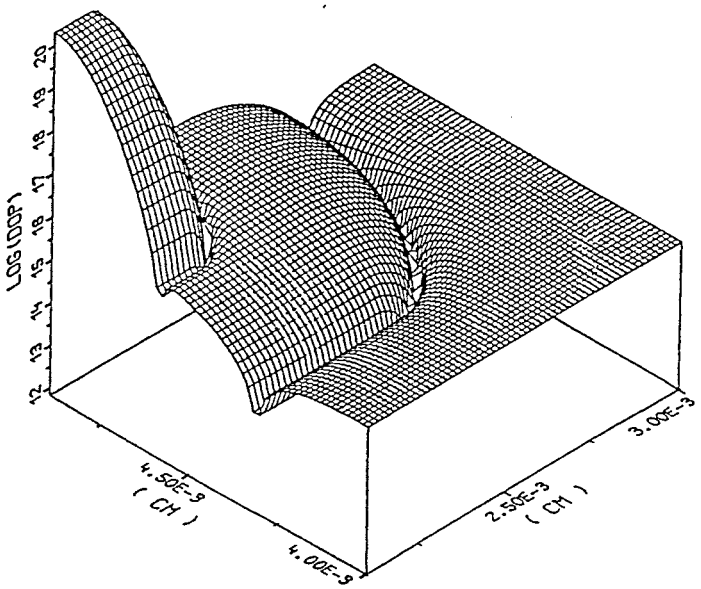

Fig.(3) Section of doping concentration

We started the simulation at −1V gate voltage (for numerical reasons) successively increasing the drain voltage from 0V. Usually a negative bias at the gate contact speeds up convergence. In this case it does not influence the behaviour of the transistor since the threshold voltage of the transistor is larger than 6V.

At a drain voltage of 52V the values for the current flow at the drain contact and the source contact raised significantly from 10^{-8} A/cm to 10^{-2} A/cm in spite of an expected breakdown voltage of more than 400V ([3]). In Fig.(4), (5), (6) the onset of the parasitic channel is shown at 53V 54V and 55V drain voltage. One can clearly see how the total current density raises exactly at the curvature of the npn-junction. The total current density is qualitatively and quantitatively the same as the electron current density. This means that the hole current flow is negligible all over the device.

From one-dimensional approaches for MOSFET's [7] the punch-through could not be explained. In these calculations the space charge regions were clearly separated from each other.

In order to demonstrate the influence of the gate voltage on punch-through the same procedure was repeated for a gate voltage of 0V. In this case punch-through occurred at 6V drain voltage. In Fig.(7) the total current density is drawn from another angle of view at $U_{Drain} = 6.5V$ ($U_{Gate} = 0V$).

There is a moderate current flow from the drain contact (right peak) through the epitaxial layer towards the parasitic channel where it raises up to the n^+-doped source region (left peak). It should be noticed that there is no current flow (exept very small leakage currents) through the substrate towards the contact at the opposite side of the device which may be expected at high voltage breakdown by avalanche.

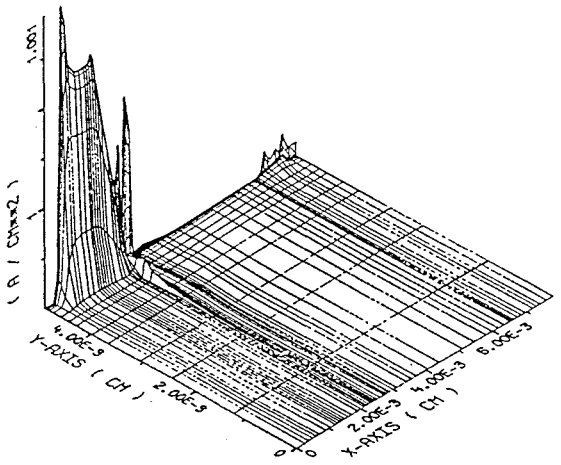

Fig.(4) Total current density at 53V drain voltage

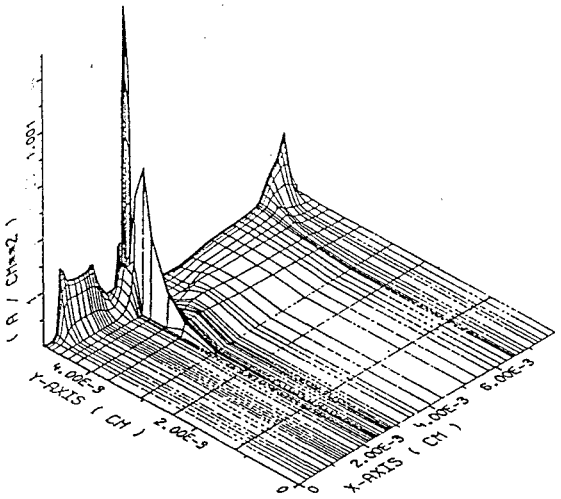

Fig.(5) Total current density at 54V drain voltage

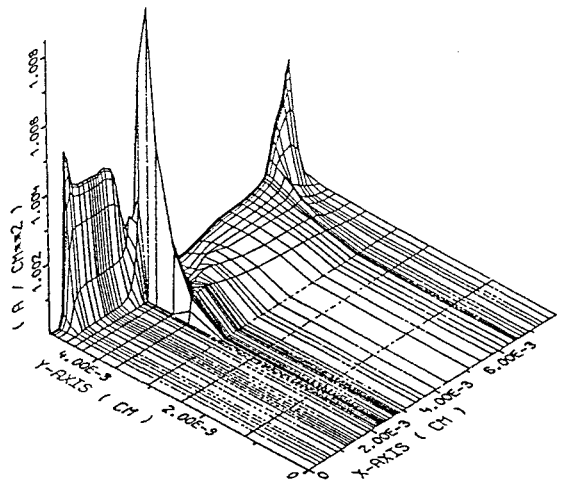

Fig.(6) Total current density at 55V drain voltage

In Fig.(8) the electron concentration is shown ($U_{Gate} = -1V$, $U_{Drain} = 60V$). It can be seen that there is a high electron concentration in the region of the parasitic channel (arrow). This effect is only of local importance. Regarding the whole semiconductor area there is qualitatively no difference to the electron concentration at a doping profile avoiding punch-through except in this small area. It should be pointed out that the MOS transistor is still in OFF-condition as we could easily recognize from the values for the electron concentration in the n-channel.

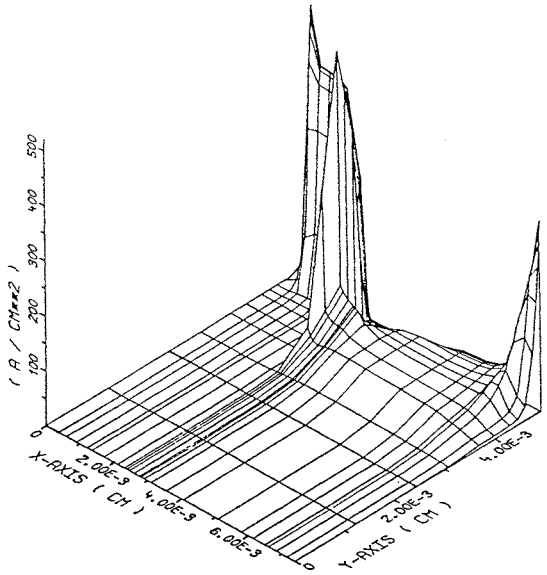

Fig.(7) Total current density at 6.5V ($U_{Gate} = 0V$)

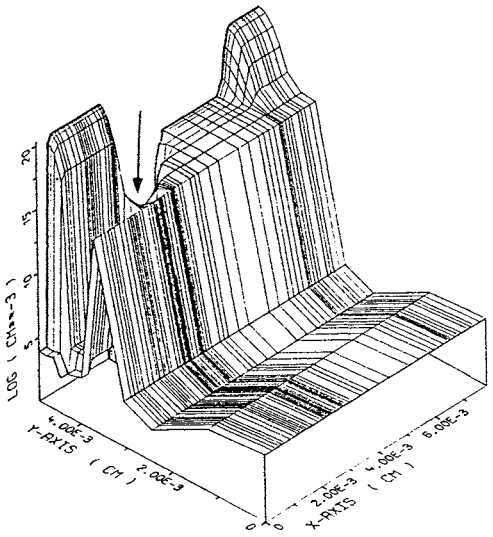

Fig.(8) Electron concentration ($U_{Gate} = -1V$, $U_{Drain} = 60V$)

Next we have analyzed the device avoiding punch-through. For these simulations we have assumed a substrate doping concentration of $1.2 \cdot 10^{14}$ cm^{-3} and an epitaxial doping concentration of $3.0 \cdot 10^{14}$ cm^{-3}, i.e. we have decreased the former values by a factor of 10. Even at $U_{Gate} = 0V$ and $U_{Drain} = 100V$ no punch-through could be observed. In Fig.(9) the total current density is shown. Note that the scales of Fig.(7) and Fig.(9) differ by more than a factor of 10^7. The peaks near the drain contact and the source contact result from small leakage currents spreading over the whole area of the device.

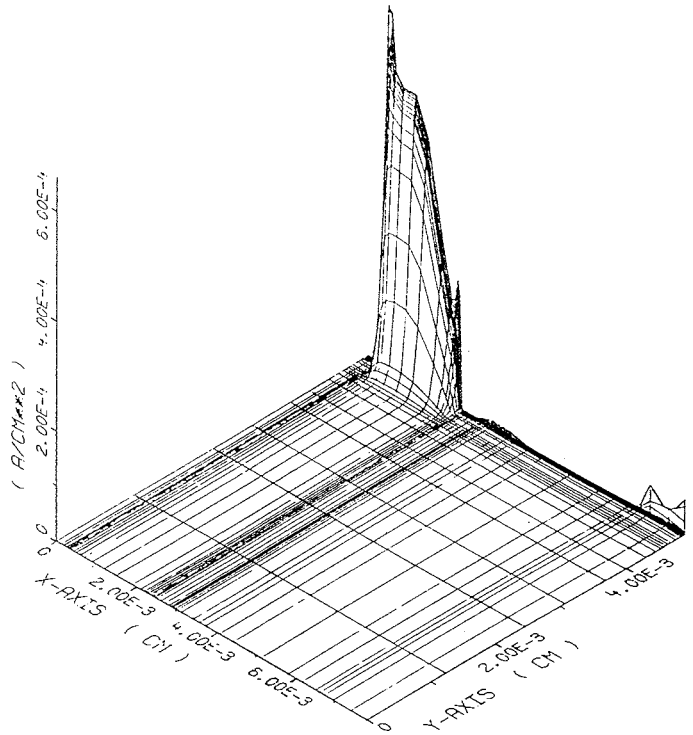

Fig.(9) Total current density without punch-through at $U_{Drain} = 100V$

3. Punch-through in ON-condition

Another point of our investigations is the behaviour of the MOS transistor in ON-condition depending on the parasitic channel. This simulation has been performed in order to analyze the influence of punch-through on the switching behaviour. First one may expect that the regular n-channel will not be built up, because the whole current flow might be concentrated in the parasitic channel.
We have not performed a transient analysis, since the results from transient and steady state computations are almost identical in this case.

We have started our simulation (assuming the first doping profile as described in paragraph 2) at $U_{Gate} = -1V$ and $U_{Drain} = 25V$ successively increasing the gate voltage while the drain voltage was held constant.
In Fig.(10), (11), (12) and Fig.(13), (14), (15) the hole concentration and the electron concentration, respectively, near the n-channel are shown. We have picked out three typical points in the switching: $U_{Gate} = 3V$ (OFF-condition), $U_{Gate} = 6V$ (near threshold voltage) and $U_{Gate} = 9V$ (ON-condition).
One can nicely see that at $U_{Gate} = 3V$ there are only few electrons in the channel while there is a high hole concentration. At $U_{Gate} = 9V$ the electron concentration in the p^+-doped channel is as large as in the n-doped areas on the left and the right hand side. There are almost no holes in the channel.
The onset of the parasitic channel could be observed at a gate voltage of about 0V, but in spite of its existence the regular n-channel has been built up in the same manner as with the doping profile that avoids punch-through. This means that in ON-condition the parasitic channel is indeed only

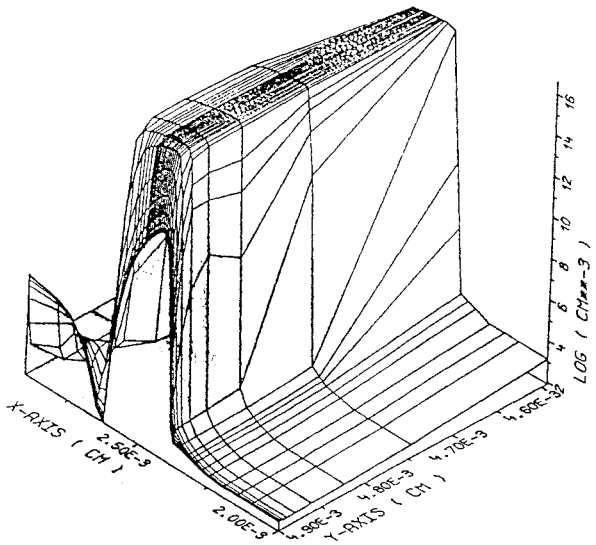

Fig.(10) Hole concentration in the channel at $U_{Gate} = 3V$ ($U_{Drain} = 25V$)

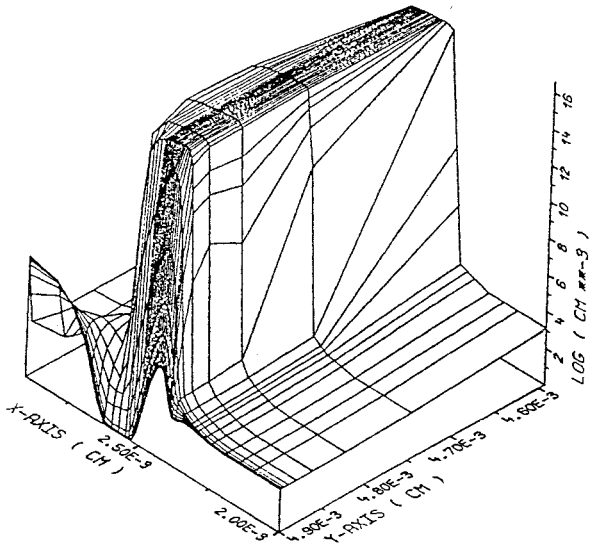

Fig.(11) Hole concentration in the channel at $U_{Gate} = 6V$ ($U_{Drain} = 25V$)

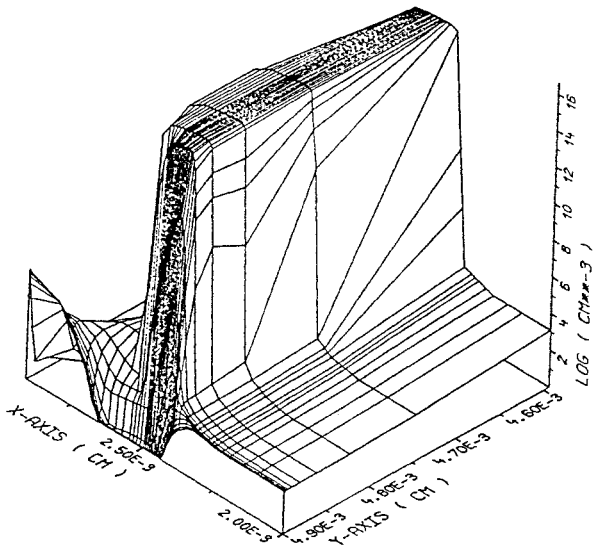

Fig.(12) Hole concentration in the channel at $U_{Gate} = 9V$ ($U_{Drain} = 25V$)

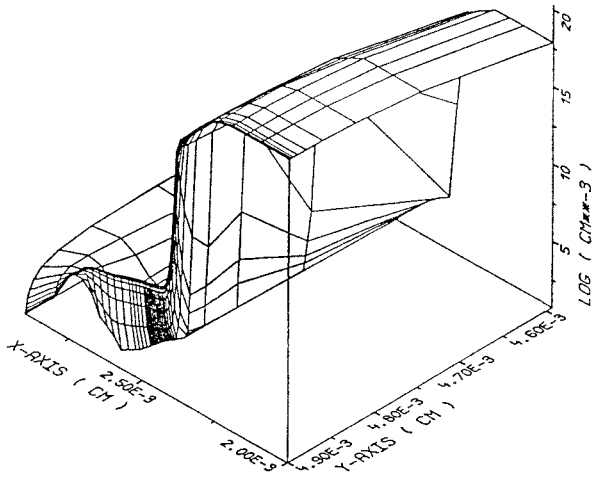

Fig.(13) Electron concentration in the channel at $U_{Gate} = 3V$ ($U_{Drain} = 25V$)

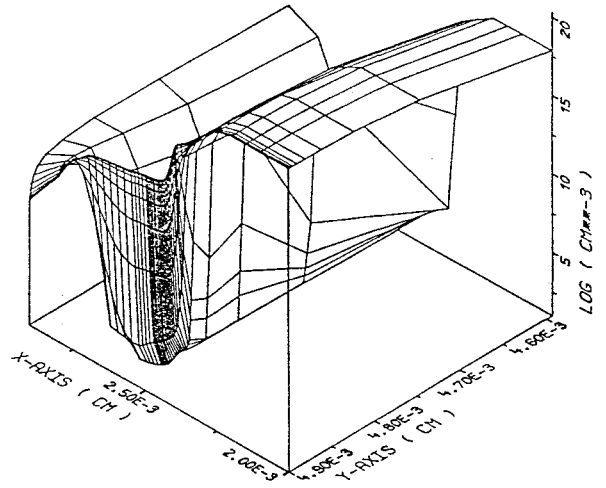

Fig.(14) Electron concentration in the channel at $U_{Gate} = 6V$ ($U_{Drain} = 25V$)

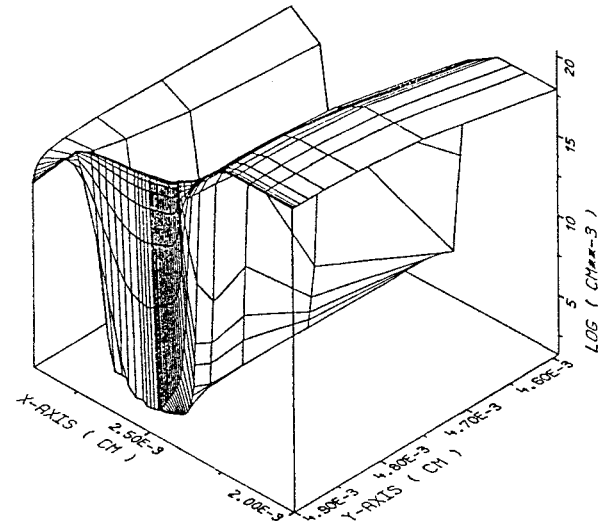

Fig.(15) Electron concentration in the channel at $U_{Gate} = 9V$ ($U_{Drain} = 25V$)

a local effect. It does not disturb the switching behaviour of the MOS transistor in a critical way. On the other side the device might be destroyed by the parasitic channel. An analysis of the switching off behaviour of the MOS transistor has not been performed.

4. Conclusion

We have presented a fully two-dimensional analysis of breakdown phenomena by punch-through in lateral DMOS devices. These effects cannot be explained by one-dimensional models. Furthermore it is shown that this kind of transistor is highly sensitive to the doping profile. Even at concentrations taken from recent publications punch-through may occur, if the npn-junction - in particular the curvature - is not designed very carefully. An analysis of high voltage breakdown by impact ionization may be subject to another paper.

6. Acknowledgements

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7. References

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