COMPARISON OF LONG- AND SHORT-CHANNEL MOSFET'S CARRIED OUT BY 3D-MINIMOS

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An accurate three-dimensional simulation program for MOSFET devices has been developed by extending MINIMOS (vers. 4) in 3D. The physical model is based on the 'hot-electron-transport model', which includes the Poisson equation, the continuity equations and a selfconsistent set of equations for the currents, mobilities and carrier temperatures. The standard finite difference discretization and the SOR (successive over relaxation) method are utilized to reduce computational time and memory requirements. Adaptive grid refinement is used to equidistribute the discretization errors. Three-dimensional effects like threshold shift for small channel devices, channel narrowing and the accumulation of carriers at the channel edge have been successfully modeled. Our comparison of several MOSFET's make clear that three-dimensional calculations are most important for accurate device modeling.

1 Introduction

The shrinking dimensions of the elements of IC's require for accurate simulation suitable device models in physics and mathematics. The two-dimensional device simulations performed in earlier times described the electrical characteristics for large transistors well but the advanced VLSI technology led to serious problems in modeling such devices and therefore a great demand appeared for 3D simulations.

The three-dimensional effects in MOSFETs like the increasing threshold voltage and the shift of the breakdown voltage caused by the finite channel width are not taken into account by the two-dimensional simulations [1]; the 2D programs are meanwhile state of the art. Accurate investigations of the previously stated effects and the knowledge of increased current densities under certain bias conditions at the channel edge are important not only for studying the electrical device characteristics but also for aging effects [2]-[3]. Therefore we have extended the two-dimensional MINIMOS to a three-dimensional simulation program. A realistic physical model and suitable mathematical algorithms have been developed to simulate the previously stated three-dimensional effects.

We shall report in Chapter 2 about the physics and the mathematics on which the simulations are based.

The results of our simulations carried out by 3D MINIMOS are reported in Chapter 3 and will be discussed there, too. We shall show that the three-dimensional simulations are indispensable for the advance from VLSI- to ULSI technology.

2 The Physical Model and the Mathematical Algorithms for the Three-Dimensional Simulation

The physical model for the simulation program is given by the Poisson and the continuity equations and the drift-diffusions model for the carrier current densities.

$$div\ grad\ \psi = \frac{q}{\varepsilon}(n - p - C) \tag{1}$$

$$div\ J_n = qR \tag{2}$$

$$div\ J_p = -qR \tag{3}$$

$$J_n = -q\mu_n(n\ grad\ \psi - grad\ (U_{t_n} n)) \tag{4}$$

$$J_p = -q\mu_p(p\ grad\ \psi + grad\ (U_{t_p} p)) \tag{5}$$

The Poisson equation (1) will always be solved fully

three–dimensionally; the continuity equations (2) and (3) at the first level of sophistication are solved two–dimensionally in the middle of the channel width. The carrier distribution in the whole volume will be calculated by the assumption of negligible current flow in the third direction $J_{n_z} = J_{p_z} = 0$. Assuming the validity of Boltzmann statistics the previous statement is equal to constant quasi Fermi levels in the direction of the channel width

$$\frac{\partial \varphi_n}{\partial z} = \frac{\partial \varphi_p}{\partial z} = 0$$

So we can write

$$n_{x,y,z} = n_{x,y,\frac{w}{2}} \cdot exp(-\frac{1}{U_t} \cdot (\psi_{x,y,\frac{w}{2}} - \psi_{x,y,z})) \quad (6)$$

$$p_{x,y,z} = p_{x,y,\frac{w}{2}} \cdot exp(+\frac{1}{U_t} \cdot (\psi_{x,y,\frac{w}{2}} - \psi_{x,y,z})) \quad (7)$$

The index $\frac{w}{2}$ denotes the middle of the channel width.

The second level of sophistication is obtained by assuming negligible current flow in the third dimension for the majorities and solving the continuity equation for the minorities fully three–dimensionally.

The third level is the fully three–dimensional solution of the continuity equations for both the minorities and the majorities.

For solving the previously specified set of equations we apply for discretization the standard finite difference method. The grid generation will be performed by an automatic mesh refinement algorithm which equidistributes the discretization error.

The linearized equations are essentially solved with an iterative algorithm. In our case we apply the SOR (**S**uccessive **O**ver **R**elaxation) method. The general iterative algorithm:

$$B \cdot x^{(n+1)} = (B - A) \cdot x^{(n)} + b$$

is solved with the matrix $B = (\frac{1}{\omega} \cdot D - L)$. D is the diagonal part of A which is transformed to the unity matrix while L is the lower triangular part of A. With respect to the special linearization method one unknown reduces to:

$$\begin{aligned} x_i^{(n+1)} = (1-\omega) \cdot x_i^{(n)} + \omega(b_i - \\ - x_{i-1}^{(n+1)} \cdot a_{i-1} - x_{i-NX}^{(n+1)} \cdot a_{i-NX} - \\ - x_{i-NXY}^{(n+1)} \cdot a_{i-NXY} - \\ - x_{i+1}^{(n)} \cdot a_{i+1} - x_{i+NX}^{(n)} \cdot a_{i+NX} - \\ - x_{i+NXY}^{(n)} \cdot a_{i+NXY}) \end{aligned} \quad (8)$$

in which $i = 1...NX \cdot NY \cdot NZ$ (NX points in $x-$direction, NY points in $y-$direction and NZ points in $z-$direction).

The advantage of this method is given by the small amount of memory requirement, precondition work and relatively fast convergency,as well. Through an adaptive determination algorithm for the optimum relaxation factor ω we use only a moderate amount of CPU time [5]. The system of the coupled nonlinear difference equations are solved with Gummel's iterative method.

3 The Numerical Results and Discussion

With the previously given physical model a three–dimensional MOSFET simulation program has been developed. We have investigated several MOSFETs with this program, two of the investigated devices are presented in comparison and the results discussed.

Both investigated devices are of the same geometrical shape and dimensions (Fig. 1 and Fig. 2) except the channel lengths which are $5\mu m$ and $1\mu m$ for of device 1 and 2,respectively. The channel widths are $1\mu m$,the gate oxide thickness $15nm$, the substrate doping $2 \cdot 10^{16} cm^{-3}$ and the source/drain doping $1.69 \cdot 10^{20} cm^{-3}$. In Fig. 1 and Fig. 2 the field oxide which limites the channel in the third dimension, can be seen at the backside of the MOS model. The contacts of source and drain which are left and right in the figures 1 and 2, extend over the channel width, whereas the gate contact covers the channel and the field oxide. The shape of the field oxide in our case is approximated by a rectangular geometry.

The potential distribution at the bias condition $U_{DS} = 2.0V$, $U_{BS} = 0.0V$ and $U_{GS} = 3.0V$ can be seen in Fig. 3 and Fig. 4. The threshold voltages

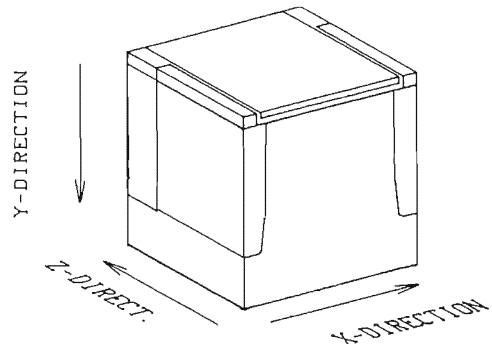

Fig.1: Perspective view of the three-dimensional MOS-FET structure with channel length of $5\mu m$ and channel width of $1\mu m$.

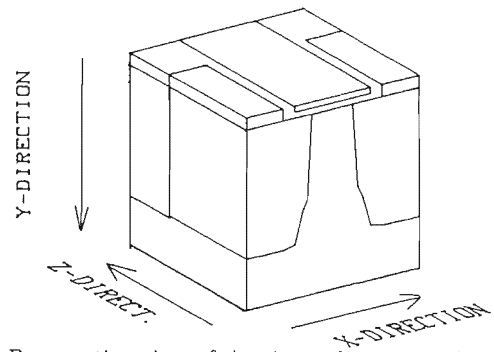

Fig.2: Perspective view of the three-dimensional MOS-FET structure with channel length of $1\mu m$ and channel width of $1\mu m$.

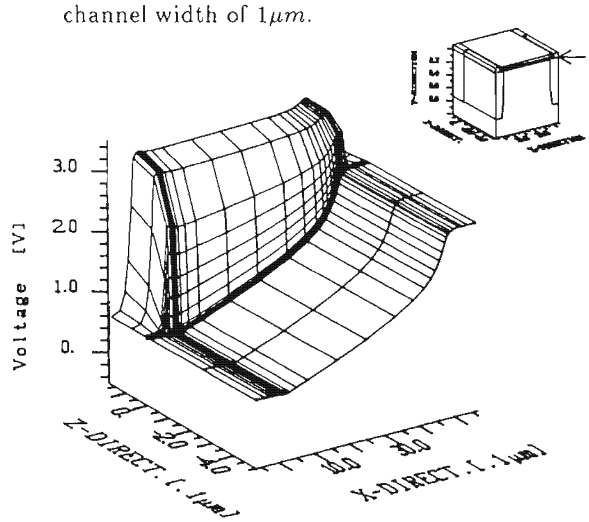

Fig.3: 3D-plot showing a detailed view of the surface potential at the channel edge along the channel length for device 1 at bias $U_{DS} = 2.0V, U_{BS} = 0.0V, U_{GS} = 3.0V$.

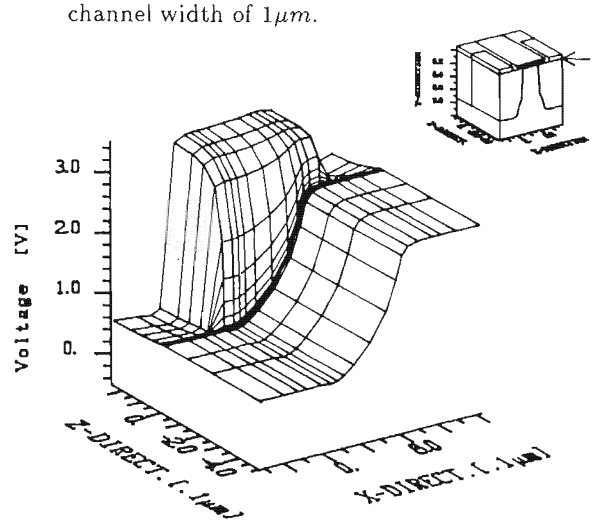

Fig.4: 3D-plot showing a detailed view of the surface potential at the channel edge along the channel length for device 2 at bias $U_{DS} = 2.0V, U_{BS} = 0.0V, U_{GS} = 3.0V$.

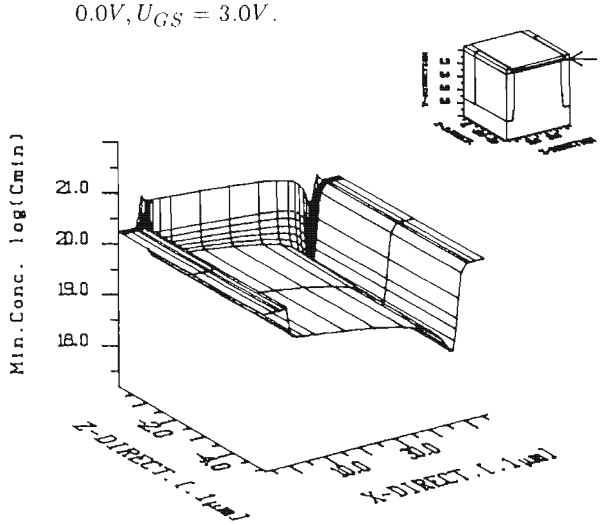

Fig.5: 3D-plot showing a detailed view of the minority density at the channel edge along the channel length for device 1 at bias $U_{DS} = 2.0V, U_{BS} = 0.0V, U_{GS} = 3.0V$.

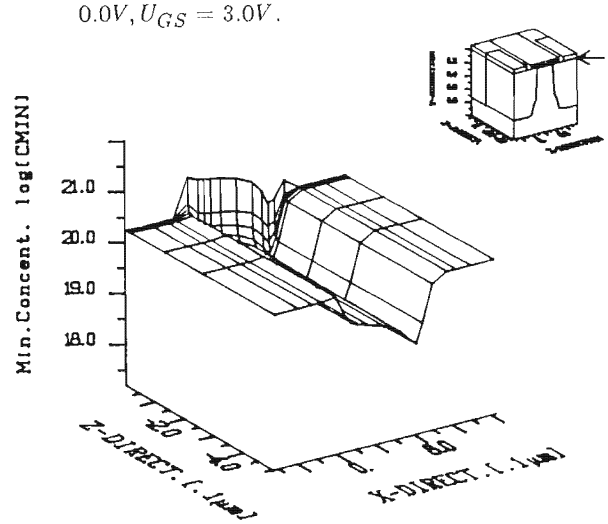

Fig.6: 3D-plot showing a detailed view of the minority density at the channel edge along the channel length for device 2 at bias $U_{DS} = 2.0V, U_{BS} = 0.0V, U_{GS} = 3.0V$.

are $U_{th} = 0.74V$ and $U_{th} = 0.62V$ for device 1 and 2, respectively. That means that we are far above threshold. Note the strong increase of the potential in the field oxide. The minority (electron) distributions (Fig. 5 and Fig. 6), show a very interesting effect. The carrier densities in the short channel MOSFET (device 2) is much higher compared to that of the long channel MOSFET (device 1). The accumulation of the minorities at the channel edge at the given bias condition is based on the limitation of the channel width and the high potential in the oxide region. In the subthreshold region this effect will change into its opposite. The currents calculated by two-dimensional simulations at the previously described bias conditions will be much smaller compared to that of three-dimensional simulations. These effects increase with shrinking device dimensions. Both short and small channel devices will be very sensitive on geometrical changes in respect to their electrical characteristics. Especially we expect that the increase of minorities at the channel edge influences the reliability and safety of devices.

Not only the previously discussed effects but also other three-dimensional effects like the shift of the threshold voltage and the increased breakdown voltage at small channel MOSFETs have been simulated with our program. All these effects are known from theory and from practical measurement but not satisfactorily modeled until now.

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