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ON-RESISTANCE IN THE ALDMOST

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Abstract — Recently a new lateral power MOSFET named *accumulation lateral DMOS transistor* (ALDMOST) has been proposed. We have investigated the dependence of the ON-resistance of this type of device on the oxide thickness and the additional semi-insulating layer along the surface of the gate oxide above the drift region. This layer has been introduced in order to lower the high ON-resistance which is in general a disadvantage of this type of MOS transistors.

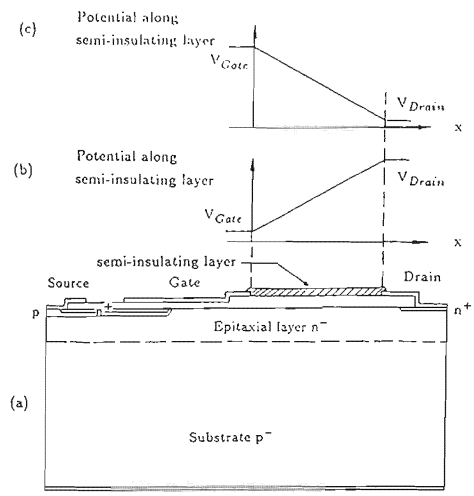

Fig. 1 Geometry and voltage distribution along semi-insulating layer
(a) Geometry
(b) Voltage distribution in OFF-condition
(c) Voltage distribution in ON-condition

(1) Supported by Siemens AG, Munich, West Germany
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1 - INTRODUCTION

In June 1987 a new lateral power MOSFET structure has been presented /1/. It is a modified lateral DMOS device with a semi-insulating poly-Si (SIPOS) layer along the surface of the gate oxide above the drift region. This additional layer has been introduced to lower the high ON-resistance of this type of device which is in general a disadvantage of high voltage power MOS transistors.

We have performed a comparison between a conventional LDMOS structure which we have investigated previously /2/ and the ALDMOST /3/. The geometry of our device and the voltage distribution along the semi-insulating layer in ON- and OFF-condition can be seen in Fig. 1. It is an n-channel device with a semiconductor area of $82\mu m \cdot 49\mu m$. A significant decrease of the ON-resistance could be observed for the ALDMOST.

We have simulated the behaviour of three different devices: First we have taken the geometry from Fig. 1 with an variable oxide thickness of $0.4\mu m$ and $0.2\mu m$, respectively. Since in /1/ an oxide thickness of $0.1\mu m$ or less is requested for a significant gain in efficiency we have reduced the oxide thickness to $0.2\mu m$ and 0.1μ (constant, without step). The doping profile is approximated by Gaussian distribution functions (maximum values: n^+: $2.0 \cdot 10^{20}$ cm^{-3}, p: $5.0 \cdot 10^{16}$ cm^{-3}, n^-: $3.0 \cdot 10^{14}$ cm^{-3}, p^-: $1.2 \cdot 10^{14}$ cm^{-3}).

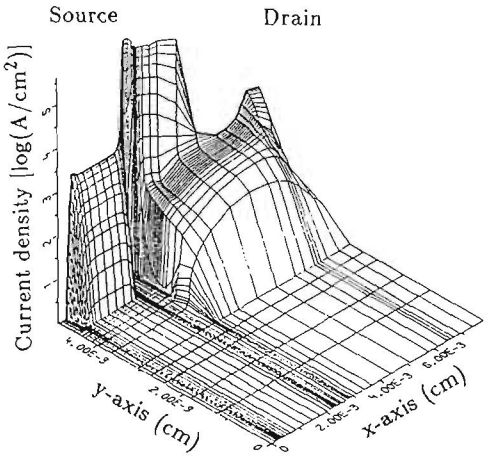

Fig. 2 Current density in ON-condition LDMOST
(V_{Drain} = 12.0V, V_{Gate} = 15.0V, oxide thickness $0.2\mu m$)

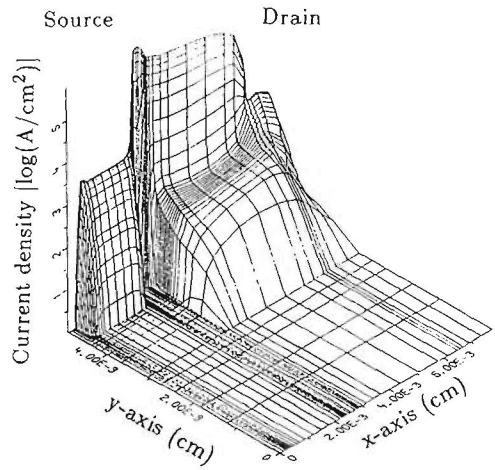

Fig. 3 Current density in ON-condition ALDMOST
(V_{Drain} = 12.0V, V_{Gate} = 15.0V, oxide thickness $0.2\mu m$)

2 - ON-RESISTANCE

The conventional LDMOS transistor has an oxide of variable thickness as it is shown in Fig. 1. A minimum oxide thickness is requested to guarantee the voltage stability by limiting the electrostatic field in the dielectric. This thickness also strongly influences the threshold voltage of the device.

For an oxide thickness of 0.4μm the threshold voltage will be approximately 6.0V, for 0.2μm the threshold voltage will only slightly change, for 0.1μm the threshold voltage will be about 2.2V.

The ON-resistance of the device mainly depends on the doping and the length of the drift region. High drift region doping lowers the ON-resistance but it results in punch-through /2/, a short drift region will lower the breakdown voltage /4/.

By the positive bias of the semi-insulating layer a strong electron accumulation under the drift region oxide will be enabled thus reducing the ON-resistance. Furthermore an additional path for the current flow close to the interface of the dielectric and the semiconductor region will be provided.

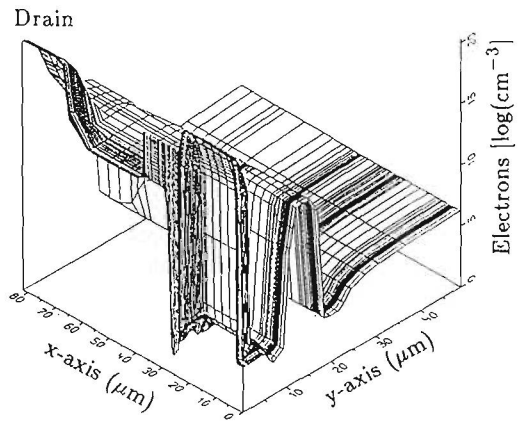

Fig. 4 Electron concentration LDMOST
(V_{Drain} = 5.0V, V_{Gate} = 6.0V, oxide thickness 0.1μm)

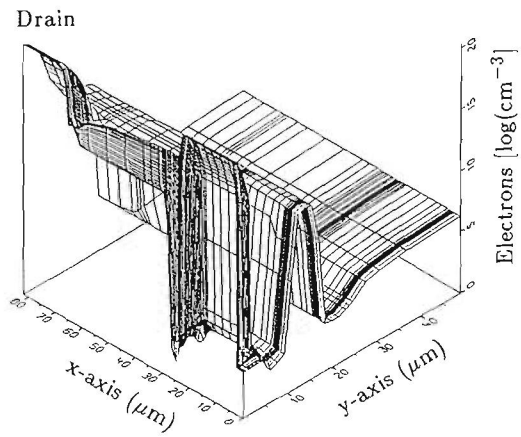

Fig. 5 Electron concentration ALDMOST
(V_{Drain} = 5.0V, V_{Gate} = 6.0V, oxide thickness 0.1μm)

3 - NUMERICAL RESULTS

The mechanism of the SIPOS layer has been discussed in /5/. We have handled the SIPOS layer as an additional Ohmic contact at the surface of the oxide between the gate and the drain contact with a linear variation of the applied potential with respect to space. It should be remarked that this smooth transition of the boundary conditions furthermore enhances the convergence speed of the Newton cycle.

During the simulation it has turned out that even for an oxide thickness of 0.4 μm above the drift region the ON-resistance is reduced by a factor of 1.5. This gain of efficiency will be increased for an oxide thickness of 0.2μm and 0.1μm. According to our results the ON-resistance will be lowered in these devices by a factor of 2 and more.

In Fig. 2 and Fig. 3 the total current densities of a conventional LDMOST and the ALDMOST, respectively, with an oxide thickness of 0.2μm are shown (V_{Gate} = 15V, V_{Drain} = 12V). It can clearly be seen how the current density leaks far into the drift region because of the additional bias provided by the semi-insulating layer above the depletion region.

In Fig. 4 and Fig. 5 the electron concentrations of the two devices are shown (oxide thickness: 0.1μm, V_{Gate} = 6V, V_{Drain} = 5V). The new path for the current flow because of the strong electron accumulation along the interface between the dielectric and the semiconductor can nicely be seen.

Our computations have been carried out with our two-dimensional device simulator BAMBI which solves the three basic semiconductor equations simultaneously in a totally selfconsistent way utilizing a 'Finite Boxes' grid /6/.

4 - CONCLUSIONS

The additional SIPOS layer provides a significant reduction of the ON-resistance in lateral DMOS transistors. Even for an oxide thickness greater than 0.1μm there is a gain in efficiency. Because the avalanche breakdown behaviour will almost not be changed by the SIPOS layer /3/ the lower ON-resistance of the ALDMOST is a real advantage compared to a conventional lateral DMOS transistor.

ACKNOWLEDGEMENTS
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REFERENCES

/1/ Habib, S.E.-D., *The ALDMOST: A new power MOS transistor*, IEEE Electron Device Letters EDL-8, No. 6, pp. 257-259 (1987)

/2/ Nanz, G., Dickinger, P., Kausel, W., Selberherr, S., *Punch-through in resurf devices*, Proc. of the AMSE-conference at Karlsruhe 1987, pp. 63-70

/3/ Nanz, G., Dickinger, P., Kausel, W., Selberherr, S., *Avalanche Breakdown in the ALDMOST*, to be presented at SISDEP 1988, September 26–29, 1988, Bologna, Italy

/4/ Colak, S., Singer, B., Stupp, E., *Lateral DMOS power transistor design*, IEEE Electron Device Letters EDL-1, No. 4, pp. 51-53 (1980)

/5/ Mukherjee, S., Chou, C.J., Shaw, K., McArthur, D., Rumennik, V., *The effects of SIPOS passivation on DC and switching performance of high voltage MOS transistors*, IEDM Tech. Dig., pp. 646-649 (1986)

/6/ Selberherr, S., *Analysis and simulation of semiconductor devices*, Wien, New York: Springer 1984