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TWO-DIMENSIONAL TRANSIENT SIMULATION OF THE TURN-OFF BEHAVIOR OF A PLANAR MOS-TRANSISTOR

W. KAUSEL, H. POETZL, G. NANZ and S. SELBERHERR
Institut für Allgemeine Elektrotechnik und Elektronik, Department for CAE, Technical University of Vienna, Gußhausstraße 27-29, A-1040 Vienna, Austria

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Abstract—A two-dimensional transient simulation of the turn off behavior of a short channel NMOS transistor with $L_{eff} = 0.68\ \mu m$ and $d_{ox} = 100$ Å, has been carried out with the simulation program BAMBI. For the first time an external drain resistor is accounted for in this fast switching calculation. The computation starts with a steady state bias point in the triode region. The gate voltage is pulsed from $V_{gs} = 5$ V to $V_{gs} = 0$ V immediately.

The paper presents the transient response of all physical quantities during the time after the switching. The simulation shows how the inversion layer is slowly reduced from both the source and the drain side whereas the lateral space-charge regions of both reverse biased *pn*-junctions build up quickly. Even at a time when lateral current has already vanished, electrons still remain in the channel region. They diffuse into the bulk, although the channel length is very short in comparison to the bulk depth. The electrons in the bulk slowly vanish by recombination.

It should be pointed out, that our results are based on a totally selfconsistent solution.

1. INTRODUCTION

The switching behavior of MOS-transistors is of considerable interest because of a wealth of work aimed at the increase of integrated circuit switching speeds.

Therefore many transient analyses and analytical models have been published, that describe and explain what happens during the switching process of MOS-transistors[1–3]. These publications deal with transistors with long channel lengths or work out one dimensional models, which loose validity for channel length shorter than 3 μm.

In contrast this paper is the first to present the switching process for a realistic short channel device. We shall show the results of a complete transient 2-D simulation of a MOS-transistor with oxide thickness $d_{ox} = 100$ Å, channel doping under the oxide $N_A = 1.10^{17}\ cm^{-3}$ and substrate doping $N_A = 6.10^{15}\ cm^{-3}$. With a gate length of $L = 0.85\ \mu m$ and a lateral extension of the drain and source diffusion areas of $\Delta L = 85$ nm under the gate contact the transistor has an effective channel length of $L_{eff} = L - 2 \cdot \Delta L = 0.68\ \mu m$. Both diffusion areas have a depth of 227 nm. The doping profile is seen in Fig. 1. The lateral direction corresponds to the x-coordinate. The vertical direction corresponds to the y-coordinate. The threshold voltage of the device is $V_t = 0.8$ V.

Our analysis has been carried out by applying the 2-D device simulator BAMBI[4] which solves the three basic semiconductor eqns (1)–(3) together with the two transport eqns (4) and (5) discretized on a rectangular grid.

$$\Delta\psi = -\frac{q}{\epsilon}(p - n + N_D - N_A) \tag{1}$$

$$\nabla J_n = q\left(\frac{\partial n}{\partial t} + R_n\right) \tag{2}$$

$$\nabla J_p = -q\left(\frac{\partial p}{\partial t} + R_p\right) \tag{3}$$

$$J_n = qD_n\nabla n - q\mu_n n\nabla\psi \tag{4}$$

$$J_p = -qD_p\nabla p - q\mu_p p\nabla\psi. \tag{5}$$

The local discretization is accomplished by means of the method of Finite Boxes[5]: lines are terminated in regions where the discretization error becomes small enough, so that no additional discretization points in those regions are necessary to obtain the accuracy required for the calculations. Hence the number of discretization points could be dramatically reduced compared to the method of finite differences. The three basic semiconductor equations are solved simultaneously by a Newton-iteration algorithm which guarantees a totally selfconsistent solution. Time discretization is accomplished by the fully implicit backward-Euler method[6,7].

The transient calculation starts at a bias point in the ohmic part of the $I_d V_d$-characteristic with $V_{gs} = 5$ V gate–source voltage and $V_{sb} = 0$ V source–bulk voltage. The supply voltage of 5 V is applied to the drain contact by including a serial resistor of 8 kΩ. The drain current is about 0.5 mA and thus, the drain–source voltage is about $V_{ds} \approx 1$ V. Using that steady-state start solution the simulation was started with a gate–voltage ramp down from $V_{gs} = 5$ V to $V_{gs} = 0$ V within 50 ps (Fig. 2) obtaining the contact current characteristics of Fig. 3. Two major effects can be observed namely a sign reversal of the

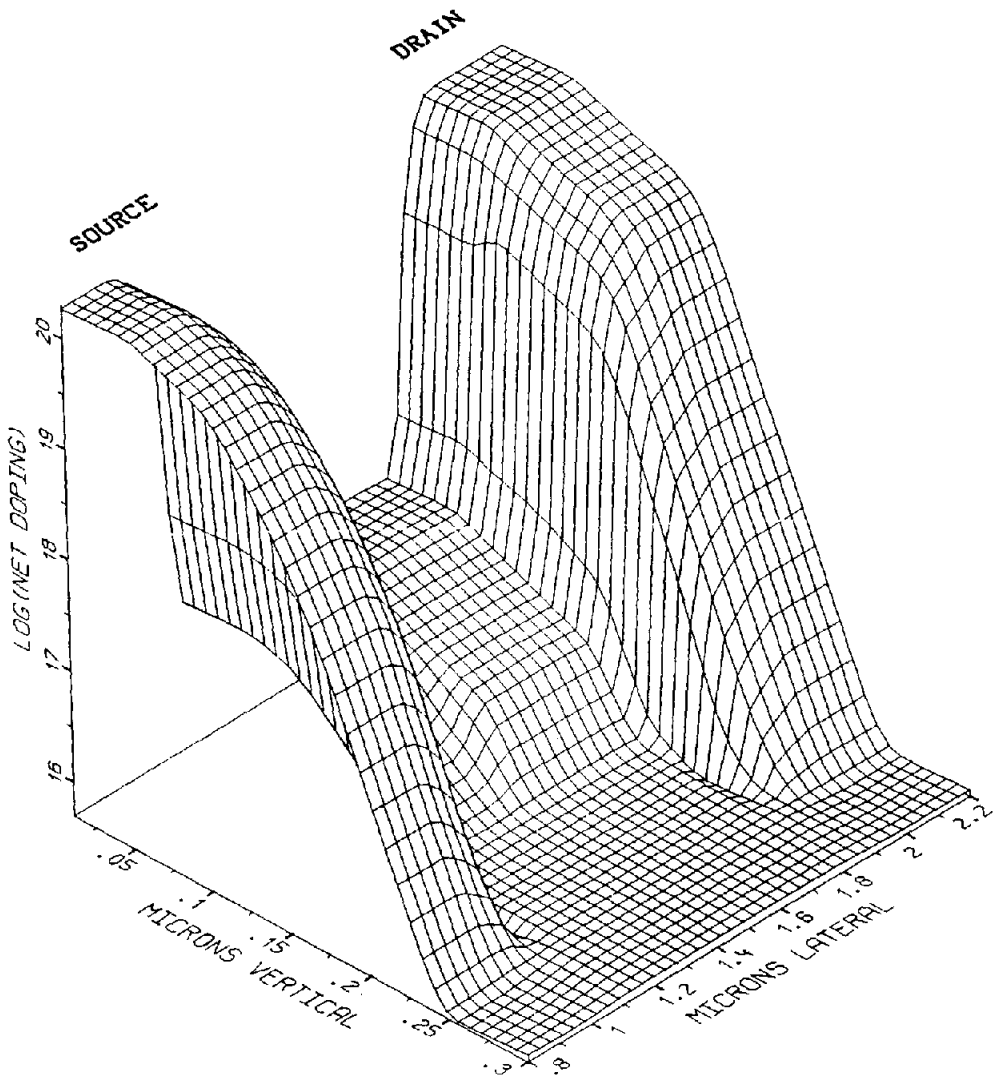

Fig. 1. Doping profile of the simulated structure (channel region).

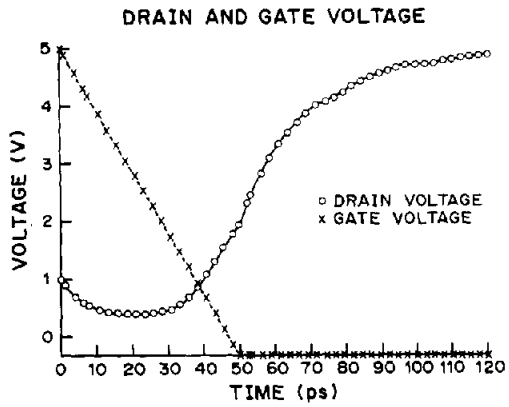

Fig. 2. Voltage of the drain contact and the gate contact vs time.

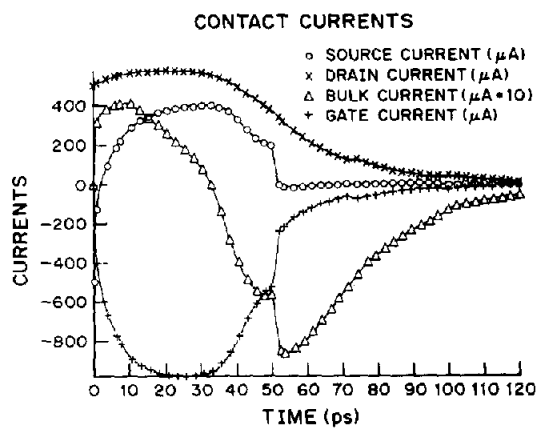

Fig. 3. Terminal currents vs time during and after the gate voltage ramp.

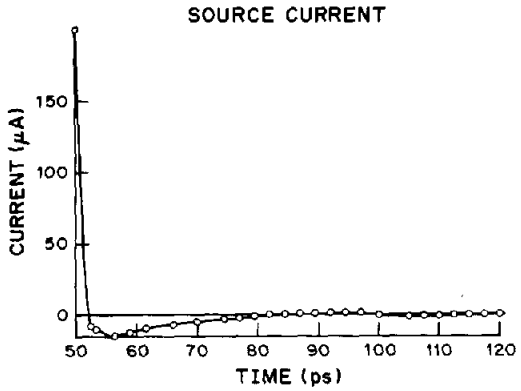

Fig. 4. Source contact current vs time after the gate voltage ramp.

bulk current after 33 ps and a sign reversal of the source current after the end of the gate-voltage ramp (Fig. 4). In order to separate the inherent transient processes in the channel region from the influence of the gate voltage ramp we decided to simulate the process with an almost abrupt gate-voltage pulse. Being aware of the fact that we use an unrealistic steep ramp we pulsed the gate voltage immediately down from $V_{gs} = 5$ to $V_{gs} = 0$ V, a value beyond the threshold voltage. The transient response to that pulse has been simulated with time steps of 0.5 ps in the beginning increasing up to 10 ps at the end of the computation.

In the following chapters we present the transient behavior of all interesting physical quantities (i.e. electron and hole concentration, potential, field, electron and hole current densities).

2. ELECTRON DISTRIBUTION

The well known steady-state electron distribution of the channel region before switching makes it obvious that the amount of negative storage charge between source and drain under the channel is quite high (Fig. 5). Therefore it can be expected that the turn-off behavior will be mainly influenced by diffusion and recombination. This has been proved by our simulation.

Already the figure after 1 ps (Fig. 6) shows that electrons are diffusing back into the bulk. This diffusion process takes place on the source side of the channel region only.

Besides this diffusion current, a lateral field forces the electrons to flow into the drain and source diffusion regions on both sides of the channel and consequently the inversion layer shows a reduction in concentration on both sides compared to the level in the center. However, the drain current is limited due to the drain resistor. Thus, the pinch off on the source side is significantly higher. The high field currents on both sides of the channel give rise to the positive contact current at source and drain. Positive contact current means that the electrons are flowing out of the device.

After 25 ps the process has continued and it can be seen, that more electrons are now flowing towards drain according to the high electric field. The channel is deeply pinched off on the drain side (Fig. 7). The diffusion has carried on and distributed the minorities over the bulk where they slowly vanish by recombination. The diffusion process has obviously decreased on the source side whereas it has developed on the drain side of the channel region. The following figures prove that the process slows down significantly since the field current rapidly decreases and diffusion becomes more and more dominant.

After more than 100 ps the field current has completely vanished. At that time no contact current is flowing but the electron concentration in the channel region is still up to $10^{12}\,\mathrm{cm}^{-3}$ under the gate and about 4 magnitudes higher in the bulk than in steady-state condition (Fig. 8). The carrier lifetime now determines when the equilibrium concentration will be reached by recombination.

3. HOLE DISTRIBUTION

At the bias point in the triode region the entire area between source and drain is totally depleted from holes according to the high vertical field (Fig. 9). The space charge region of the drain–bulk diode can clearly be seen. Immediately after the voltage pulse the holes diffuse towards the semiconductor surface to fill up the depletion region under the gate since the inversion field decreases. The holes flow towards the semiconductor–oxide interface with the dielectric time constant $\tau_\epsilon = \epsilon/\sigma \approx 0.13$ ps and form an electron–hole plasma there. The figure at 10 ps shows a significant rise of the hole concentration up to $10^6\,\mathrm{cm}^{-3}$ after the switching (Fig. 10).

A time constant of $\tau(t) = C(t) \cdot R_b > 1$ ps is valid from now on slowing down that process. This becomes apparent from figures that are not included because of space limitations.

Two major effects can be studied now. Comparing the hole concentration of Fig. 10 with that of Fig. 9 a hole injection from bulk into the drain region can be observed indicating a forward biased drain–bulk diode. This indeed is confirmed by the value of the drain–source voltage of $V_{ds} = -0.8$ V at 10 ps. On the other hand the source–bulk diode reacts as a reverse biased *pn*-junction showing an increasing depletion.

This situation has completely changed after 25 ps (Fig. 11). A depletion process between drain and bulk has started as well as between drain and the channel region. With $V_{ds} = 1.9$ V at the drain contact the drain–bulk diode actually is reverse biased. Looking at the source–bulk diode we now recognize hole injection from the bulk there. The hole concentration in the channel region has reached a value of $10^{10}\,\mathrm{cm}^{-3}$ immediately under the oxide interface and a maxi-

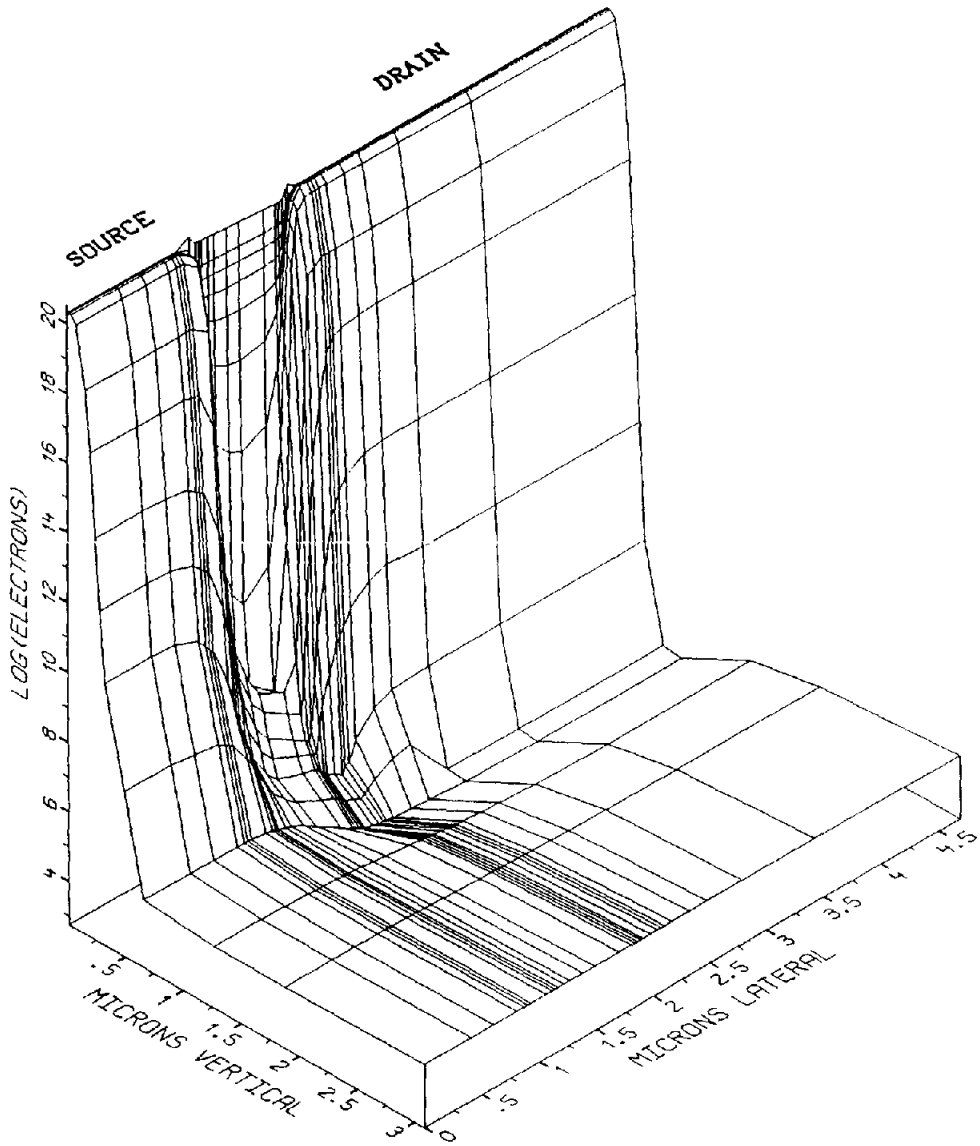

Fig. 5. Steady-state electron distribution in the whole device before switching.

mum of $5 \times 10^{16}\,cm^{-3}$ a little bit deeper under the surface due to the channel doping.

Figure 12 shows the hole distribution in the channel region after 100 ps. The concentration under the oxide semiconductor interface has been further increased to $4 \times 10^{14}\,cm^{-3}$. The distribution in the channel region still shows a depletion under the gate due to the gate voltage of 0 V compared with the flat-band voltage of -0.3 V.

Depletion at the drain–bulk diode has further continued and a deep depletion region has been established around the drain diffusion area.

On the other hand the process has turned again at the source–bulk diode and we see depletion there as well. Both charge pumping effects concerning the drain–bulk diode and the source–bulk diode will be further explained by the following chapters.

4. POTENTIAL AND ELECTRIC FIELD

Figure 13 presents the potential distribution immediately after the gate voltage pulse. Compared with the steady-state condition before switching it shows a significant change after 1 ps. The potential jumps with the voltage pulse from positive to negative values, reaches -3 V at drain and even -3.8 V in the middle of the channel region (Fig. 13). The explanation for this dramatic behavior is the capacitive effect by the gate potential which lowers the potential of the channel region and the drain voltage as well as the potential between source and bulk. Neither the homogeneous potential drop over the whole channel region according to the homogeneous negative storage charge nor the voltage drop over the space-charge region between drain and bulk has been changed. As

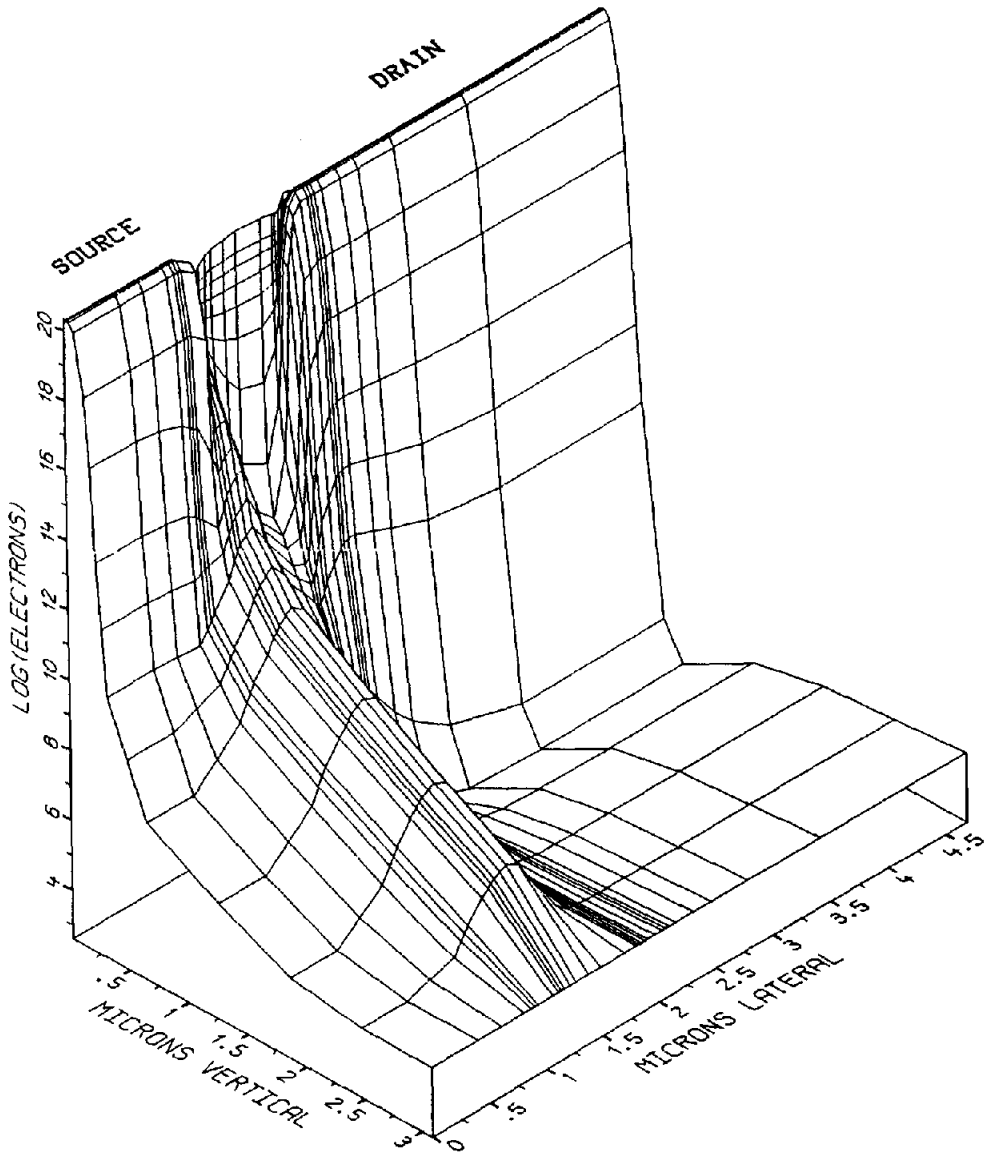

Fig. 6. Electron distribution in the whole device 1 ps after the gate voltage pulse.

a result the potential distribution over the entire device area (Fig. 13) shows significant minima.

Since the source voltage remains constant the electric field showing from source to the channel region is dramatically increased causing a high lateral displacement and field current in negative x-direction that results in a high positive current peak at the source contact (Fig. 27). The space charge region between source and the channel region builds up very quickly. The field on the drain side remains constant still showing from drain to the channel region. Last but not least a field in negative y-direction has been formed in the bulk region that is relatively high compared with the steady-state situation.

Additional results not presented in that paper show the steady increase of the drain voltage which finally reaches 5 V as well as the slow flattening of the potential distribution within the channel region and the region between source and bulk. Thus, the inversion field steadily decreases, the field between drain and the channel region increases whereas that one between source and the channel region is reduced at the same time. The displacement currents over both space charge regions are therefore flowing in negative x-direction after 3 ps. That means that the displacement current has changed sign on the source side of the channel region very quickly.

The potential minimum between source and bulk turns into a maximum after 25 ps thus initiating an oscillation process.

The behavior of the potential directly defines and explains the switching behavior of that device.

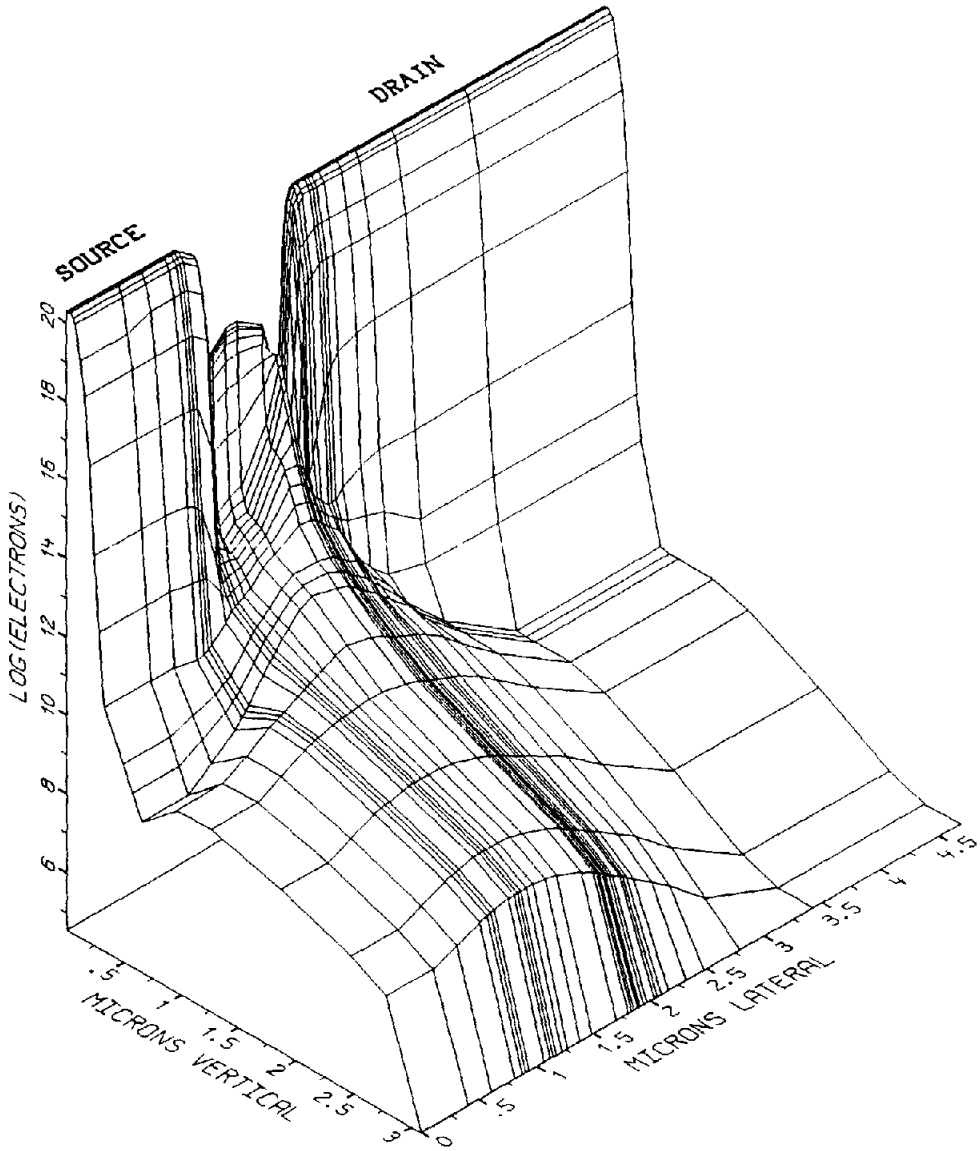

Fig. 7. Electron distribution in the whole device 25 ps after the gate voltage pulse.

5. THE CURRENT DENSITIES

The two following figures show the modulus of the electron current density in the channel region after 1 ps (Fig. 14) and after 10 ps (Fig. 15). Due to the lateral field a current is flowing at the semiconductor surface immediately. We observe a minimum which indicates a sign reversal near the middle of the channel, according to the fact that electrons leave the channel both towards drain and source. The modulus of the electron current density has its maxima exactly at the *pn*-junctions. The maximum on the source side is significantly higher in Fig. 14 than that on the drain side leading to a higher source contact current at that time. However, within the next 9 ps the modulus of the electron current density is dramatically reduced (Fig. 15). The maximum on the drain side is the higher one at 10 ps corresponding to the faster decrease of the source contact current.

The figures of the hole and the convection current densities perfectly describe the behavior of *pn*-junctions which mainly define the switching behavior of the device itself. The modulus of the hole current density at 1 ps is presented in Fig. 16. It shows a peak of $4.5 \times 10^3\,\mathrm{Acm}^{-2}$ at the entrance of the channel region. In the bulk region the density is $3.5 \times 10^3\,\mathrm{Acm}^{-2}$ being reduced to zero immediately at $y = 0.5\,\mu\mathrm{m}$ under the drain. Looking at the direction of the hole current over the entire device area (Fig. 17) we see that holes coming from the bulk contact as well as from the source junction are flowing towards the drain junction and into the channel region.

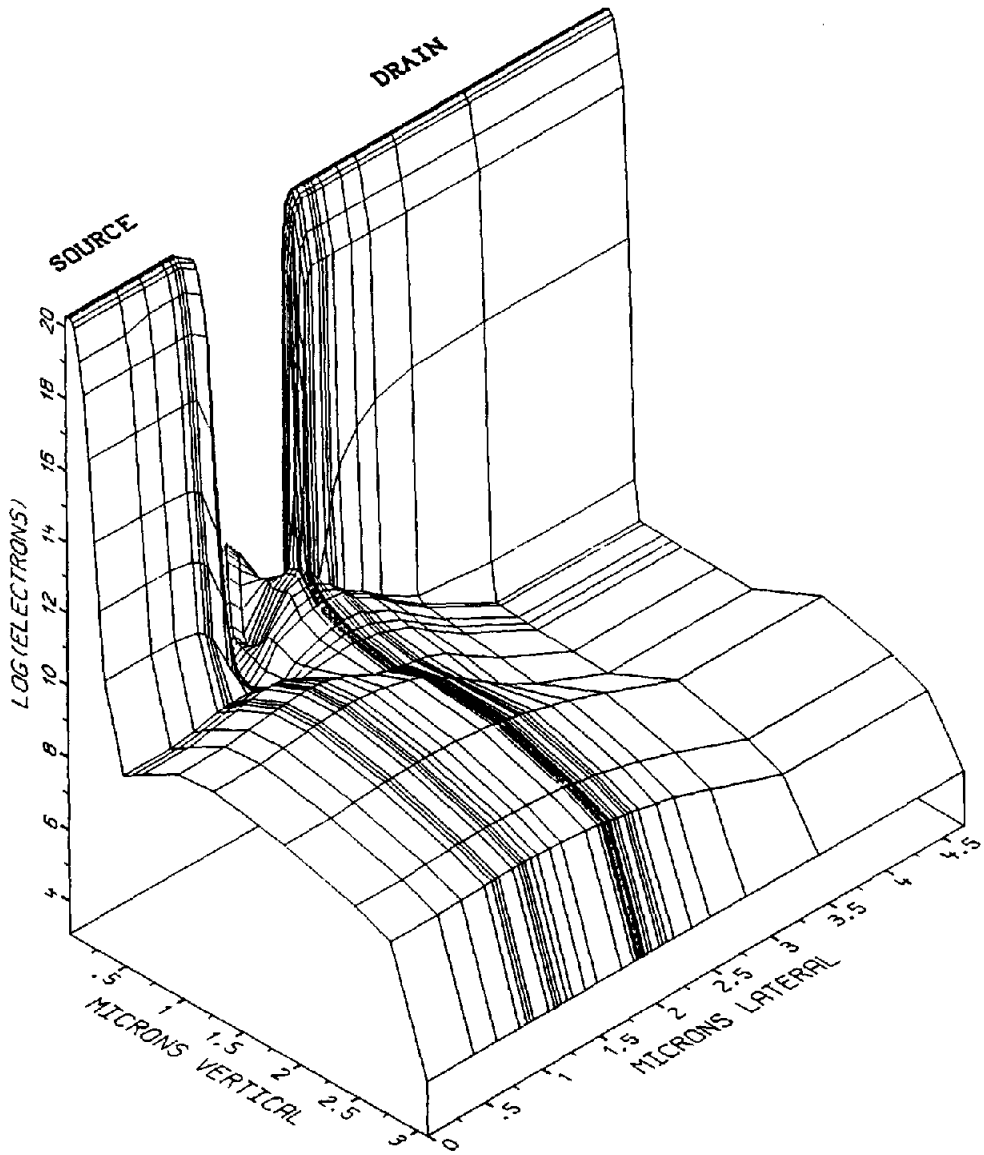

Fig. 8. Electron distribution in the whole device 100 ps after the gate voltage pulse.

To explain the current flow the direction of the total convection current at 1 ps is presented in Fig. 18. The source–bulk diode is reverse biased. A displacement current in positive y-direction passes the junction and continues as hole field current. Following the lateral field the hole current flows towards the channel region and the drain junction.

With $V_{ds} = -3$ V the drain–bulk diode is strongly forward biased. Since the field changes sign at $y = 0.9\,\mu$m the hole field current continues as diffusion and displacement current. A hole and electron injection from both sides respectively reduces the space charge region and the field. Thus, the displacement current in negative y-direction causes a corresponding electron current within the drain diffusion region that supports the reduction of the channel charge on the one hand and flows out of the drain contact on the other hand. Consequently we recognize a sign reversal of the contact current density at $x = 2.6\,\mu$m at the drain contact. Since the current from the channel region is several magnitudes higher we still have positive drain current.

Within the channel we recognize the high lateral field current and the vertical diffusion current as described above.

Two picosecond later (at 3 ps) the situation has changed at the source diode (Fig. 19). The field, still having a positive y-component as far as $y = 1.2\,\mu$m, is decreasing now. Thus, the displacement current has changed its sign flowing into negative y-direction. Within the bulk it overcompensates the hole current that flows in opposite direction, passes the space charge region and continues as electron current beyond the junction within the source diffusion

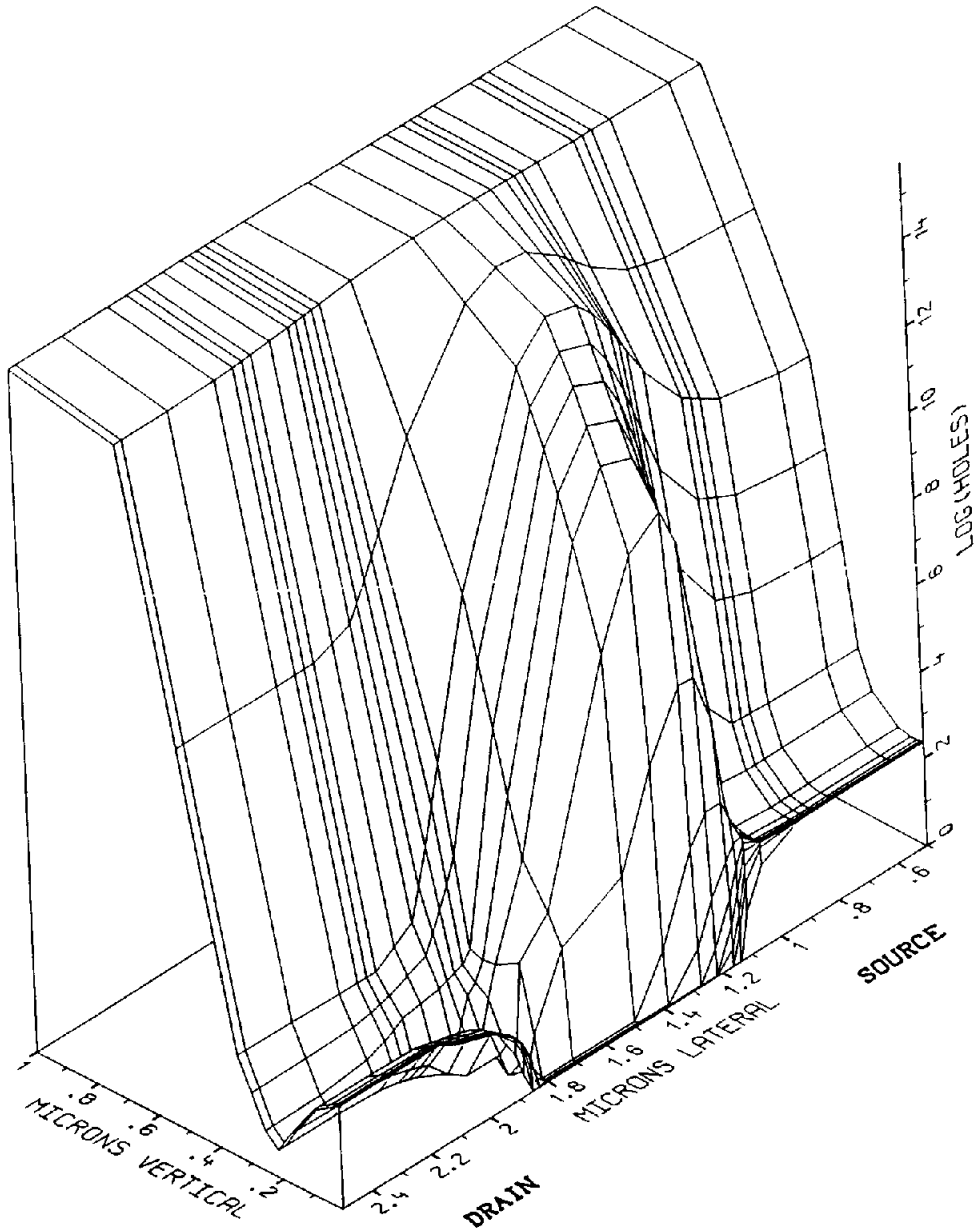

Fig. 9. Steady-state hole distribution in the channel region before switching.

region. The source electron current completely flows into the channel region at 3 ps.

At 10 ps the bulk contact current has almost reached its zero crossing. The modulus of the hole current density shows its strong reduction in the bulk as well as in the channel region. However, the peak has moved towards the surface (Fig. 20). Holes are flowing from the bulk contact towards both junctions and into the channel region (Fig. 21). The source–bulk junction now acts as a forward biased diode (Fig. 22). Carriers are injected from both sides respectively and space charge region and field are further decreased. The negative displacement current continues as electron current and partially reaches the source contact. We recognize a sign reversal of th current density at the source contact at $x \approx 0.5\,\mu$m

The negative current densities at the drain contac have vanished completely in the meantime. Th voltage drop in the space charge region has bee reduced to the built-in voltage of 0.5 V. At 10 p space charge region and field are already increasin as indicated by the electron current flowing fro drain towards the junction. This current continues a displacement current over the space charge regio according to the increasing field. It overcompensate the negative hole field current within the bulk, tur towards the channel region and continues as a ho current towards the interface. Beneath the junctio

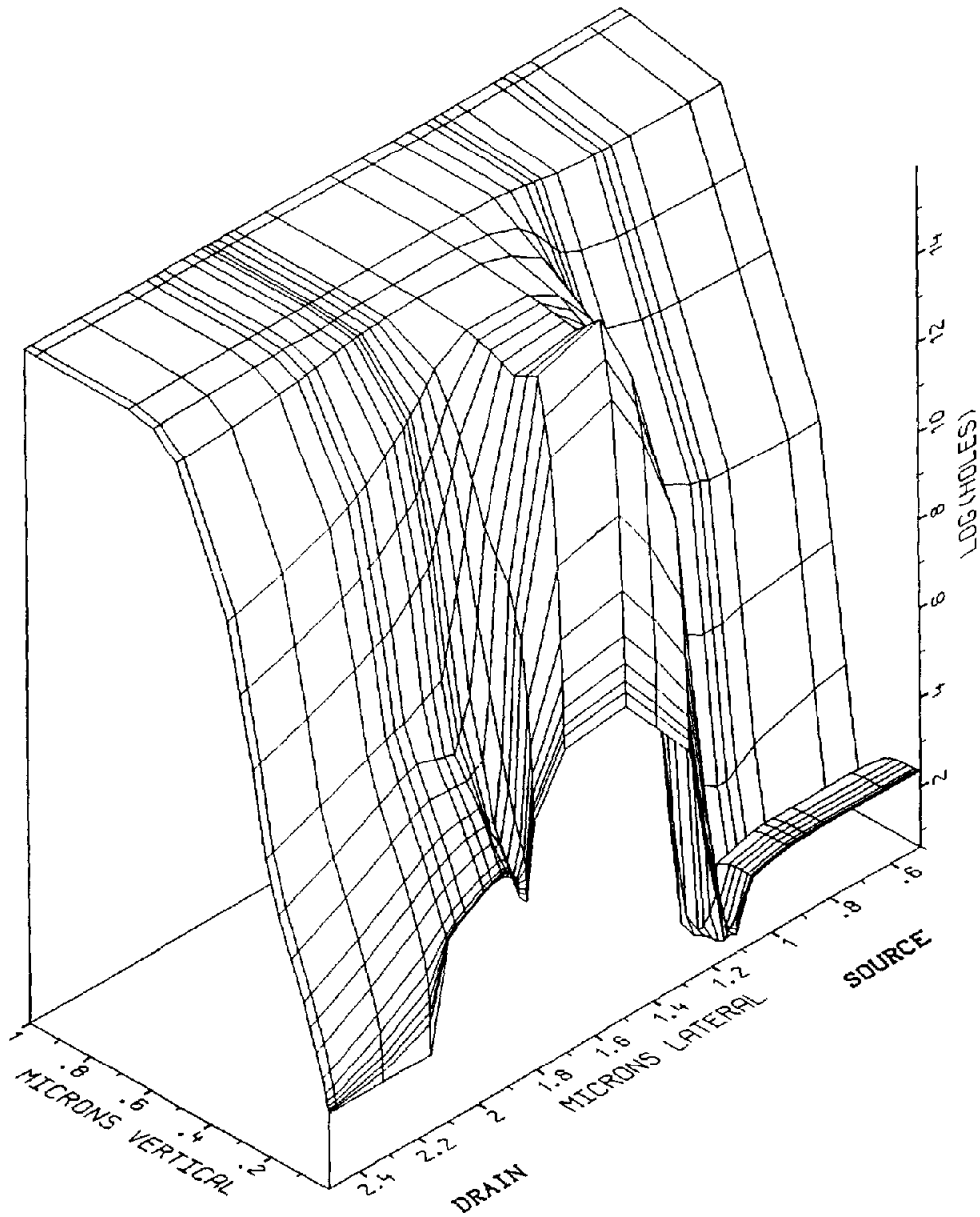

Fig. 10. Hole distribution in the channel region 10 ps after the gate voltage pulse.

holes flow towards drain due to the small but still existing negative field in the bulk region.

At 25 ps the bulk contact current reaches its negative maximum. The hole current density peak within the channel region, situated significantly closer to the surface again, has been increased from $2 \times 10^3\,\mathrm{Acm}^{-2}$ to $2.5 \times 10^3\,\mathrm{Acm}^{-2}$ (Fig. 23). The figure of the hole current direction (Fig. 24) shows that the drain junction acts as a hole current source, thus speeding up the injection of holes into the depletion region at the surface of the channel region. The hole current is flowing into the channel region and to the bulk contact as well as towards the source junction.

The potential shows a slight maximum at $y = 1.5\,\mu\mathrm{m}$ between source and bulk at 25 ps. Thus, the resulting field causes a field current towards the source junction. The source–bulk diode is still forward biased (Fig. 25). The main part of the diode current reaches the source contact causing negative source contact current at 25 ps (Fig. 27).

With $V_{ds} = 1.9\,\mathrm{V}$ the drain–bulk diode is strongly reverse biased (Fig. 25). The resulting diode switch-off current removes the storage charge and builds up the space charge region steadily. Thus, the field is increased until the voltage drop of 5 V is finally reached at the end of the switching process. The current passes the junction as displacement current thus supporting the hole diffusion current in the

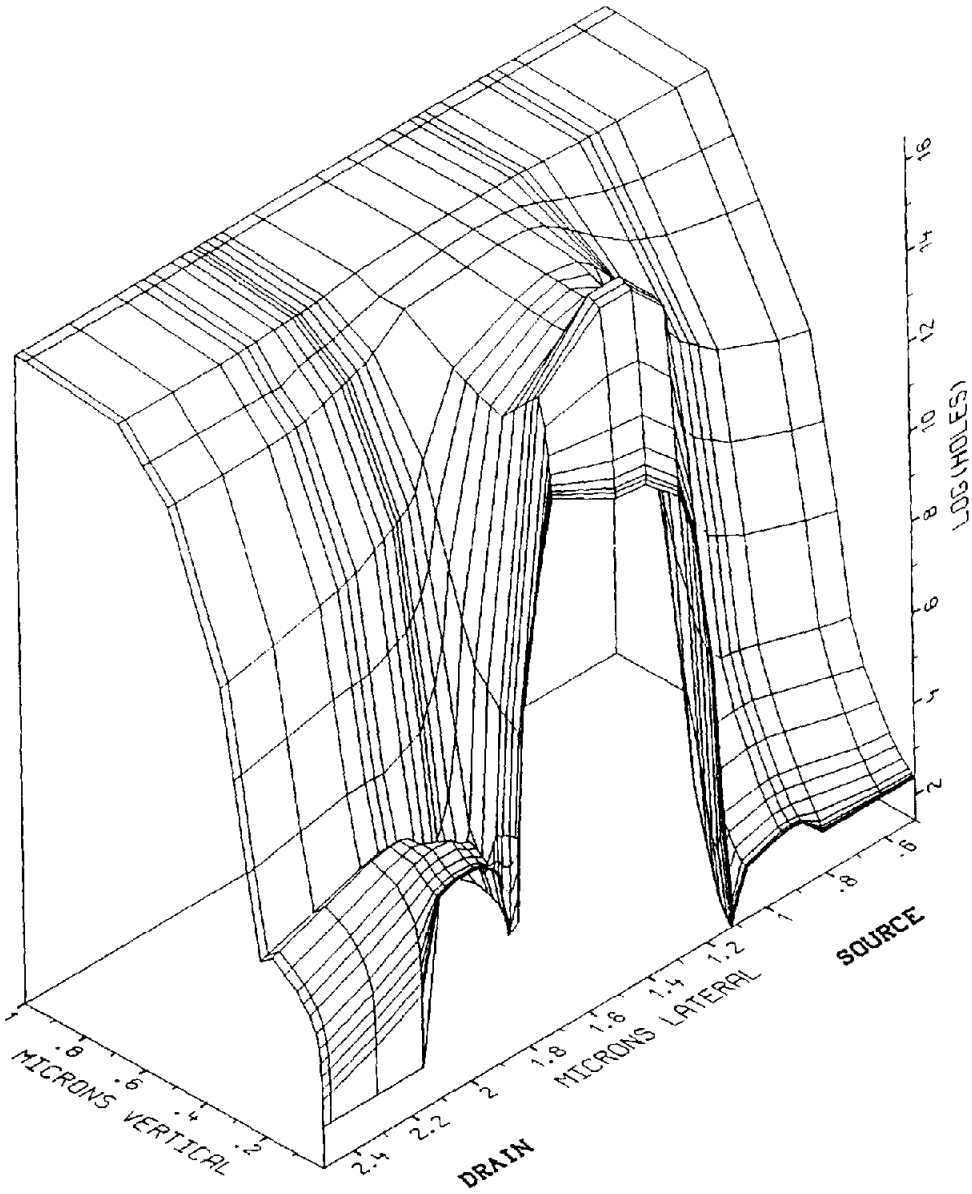

Fig. 11. Hole distribution in the channel region 25 ps after the gate voltage pulse.

channel region on the one hand and causing the negative source and bulk contact currents on the other hand.

6. DRAIN VOLTAGE AND CONTACT CURRENTS

In steady-state condition prior to the switching, the drain voltage was $V_d = 1$ V corresponding to the drain current of $I_d = 0.5$ mA. Due to capacitive effects the drain voltage jumps to -3 V (Fig. 26). Increasing almost exponentially to the final value of 5 V it reaches 90% after 60 ps with the zero crossing at 14 ps.

Looking at the terminal currents (Fig. 27) we see that source-, drain- and bulk-contact currents are flowing into the device summing up to a high displacement current that passes the oxide and flows out of the gate contact.

The source current has a high peak due to the strong field increase between source and the channel region and the corresponding displacement current over the space charge region. This displacement current decreases quickly. Changing its sign after 3 ps it reduces the source terminal current. Thus, the source current shows a significantly small time constant. It becomes smaller than the drain current after 6 ps at a time when the drain voltage still is below zero. Since the currents strongly deviate from a single exponential behavior it is difficult to obtain relevant time constants. For the source current a time constant of approximately $\tau_1 = 4$ ps seems appropriate

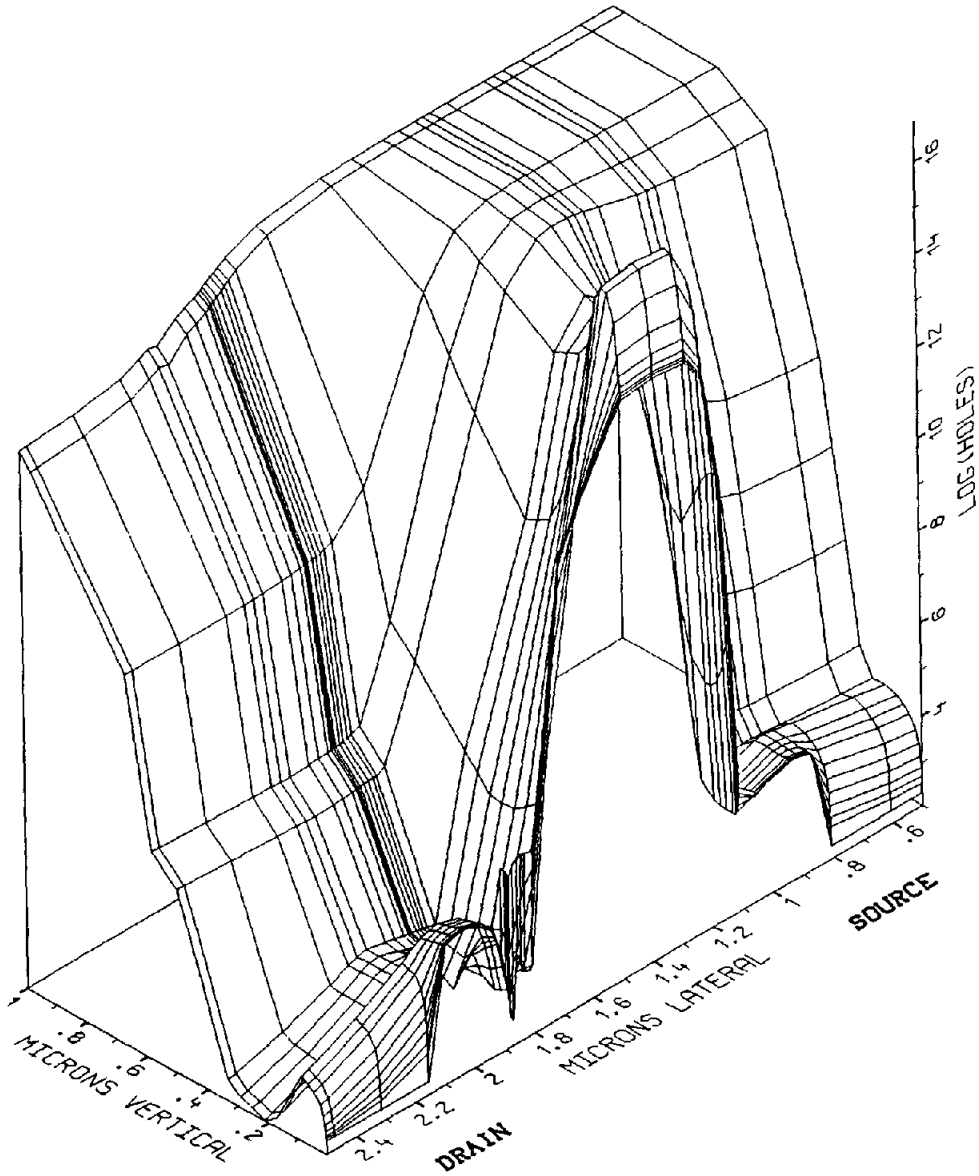

Fig. 12. Hole distribution in the channel region 100 ps after the gate voltage pulse.

while the decrease of drain current is considerably slower.

The gate current is a pure displacement current that crosses the oxide region. Since it corresponds to the source current in the beginning it shows a corresponding high negative peak and a similar time constant. After the disappearance of the source current it simply represents the continuation across the oxide region of the hole and electron current into the channel region.

The drain current initially jumps by a factor two to $I_d = 1$ mA. Its time constant is about $\tau_2 = 32$ ps corresponding to the drain resistor of 8 kΩ.

The negative bulk current after the zero crossing at exactly 12 ps originates from the hole charge in the drain–bulk diode and is not caused by a hole reflow from the channel region (Fig. 24). It is rather related to the zero crossing of the drain voltage which takes place at 14 ps and the subsequent switch off of the drain–bulk diode. This behavior is distinctly different from the switching processes of long channel devices[3].

Finally the enlarged figure of the source current shows how the terminal current follows the potential oscillations at the source–bulk diode (Fig. 28). It shows its first zero crossing after 25 ps followed by further sign reversals after 49, 81 and 96 ps.

7. CONCLUSIONS

This paper presents for the first time a complete history of all events during the turn off of a short

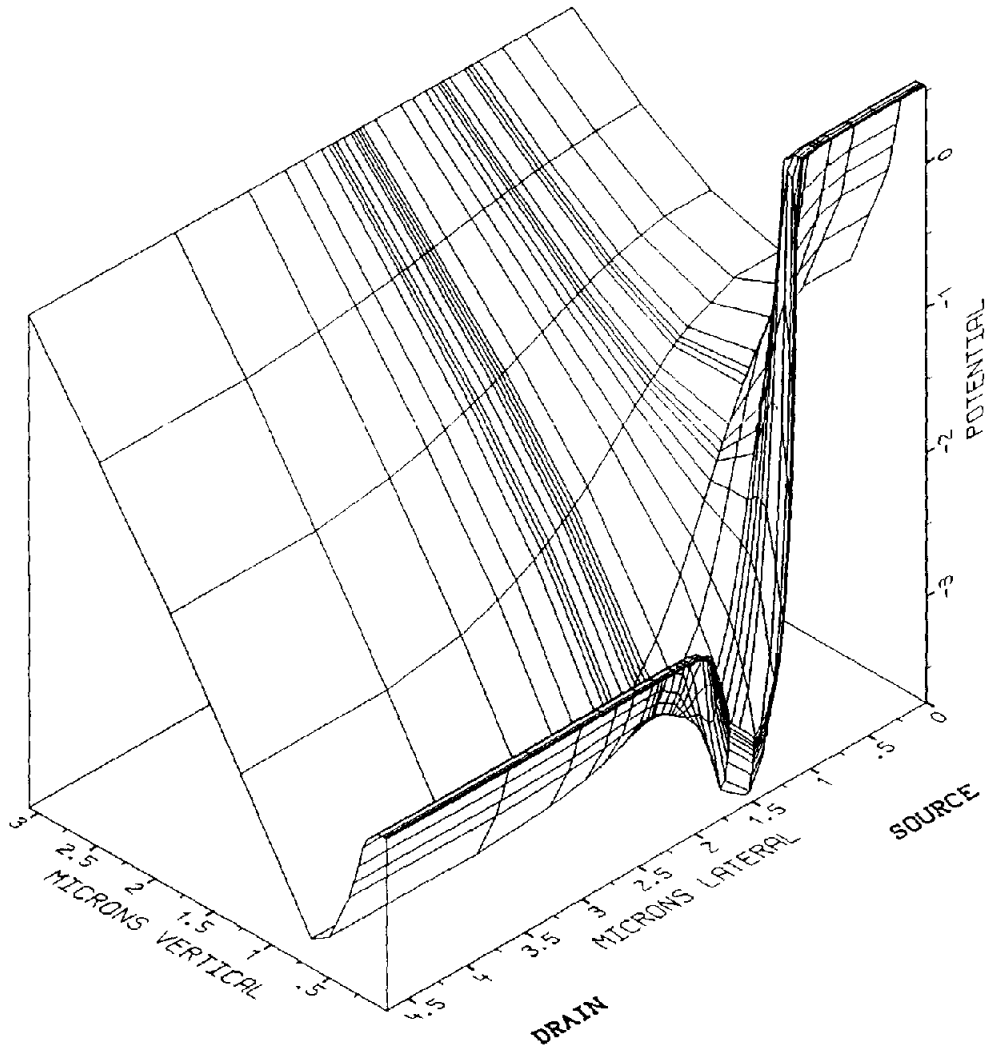

Fig. 13. Potential distribution in the whole device 1 ps after the gate voltage pulse.

channel MOS-transistor under the influence of an external drain resistor. Our simulation showed that diffusion and recombination during turn off is not at all negligible. Compared to the turn on case it takes significantly more time to reach steady state conditions[8] and again the hole current decreases slower than the electron current. The removal of the high channel charge is supported by a lateral field, strongly increased compared to the steady state condition, on both sides. This increased lateral field is caused by the significantly low values of the potential resulting from the capacitive effect. Simultaneously electrons diffuse into the bulk and spread over the whole device. In contrast to further investigations concerning a long channel device[3] no back-current from the channel region towards bulk can be observed. Holes are flowing towards the semiconductor–oxide interface during the whole process. The behavior of the bulk terminal current is mainly defined by a charge pumping current over the drain–bulk diode which is switched from a forward into a reverse biased state.

Additional results which are not presented here because of space limitations show qualitatively exactly the same behavior for the turn-off process with a 50 ps gate–voltage ramp. Processes all described above do occur in that case in the same way. Therefore the above conclusions can be used for the explanation of the terminal currents in the realistic case (Fig. 3) as well. Due to the gate–voltage ramp the currents do not jump but steadily increase to a maximum value. After the end of the ramp the gate, the source, and the bulk current show an immediate change providing that the main part of the displacement current through the oxide region came from the source contact. However a significant part of the transient gate current during the gate voltage ramp is contributed by the holes that flow back towards the semiconductor surface. At the end of the ramp this current is completely supplied by the drain contact. When the gate voltage stops decreasing the hole current towards the surface of the channel region is reduced immediately and the bulk contact current

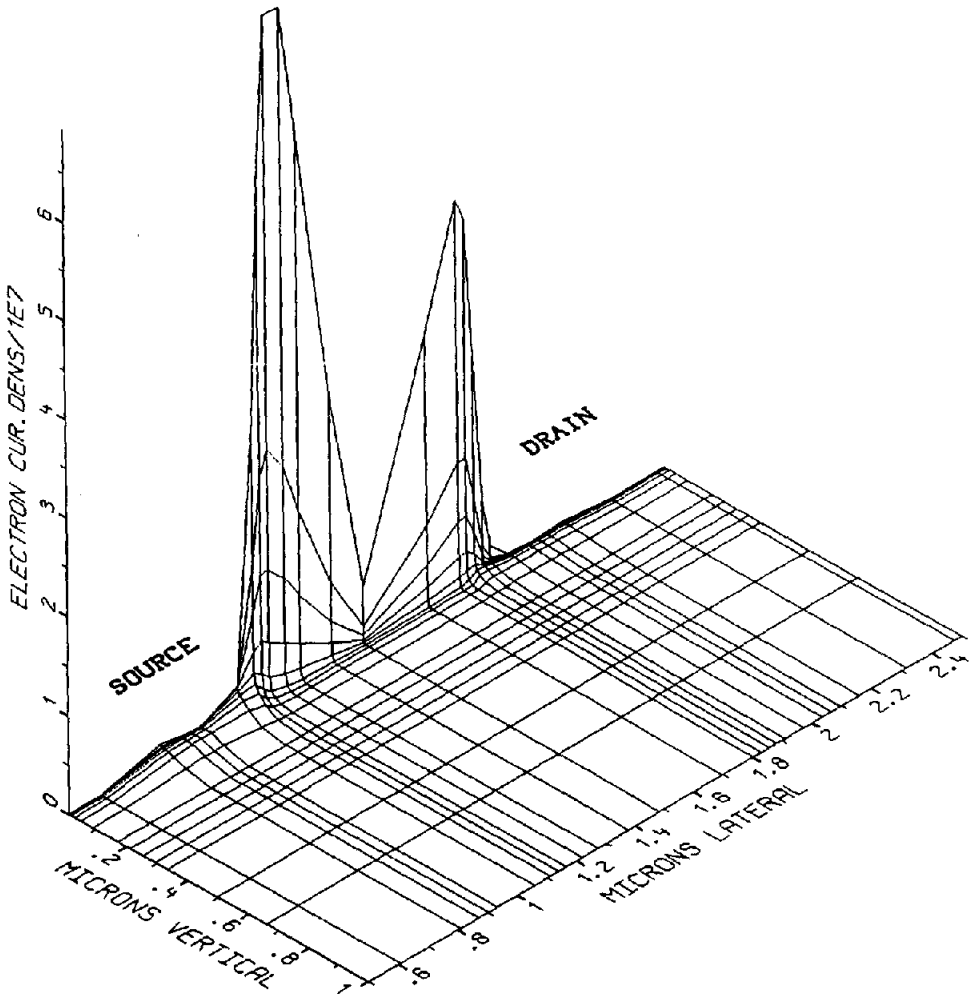

Fig. 14. Modulus of electron current density in the channel region 1 ps after the gate voltage pulse.

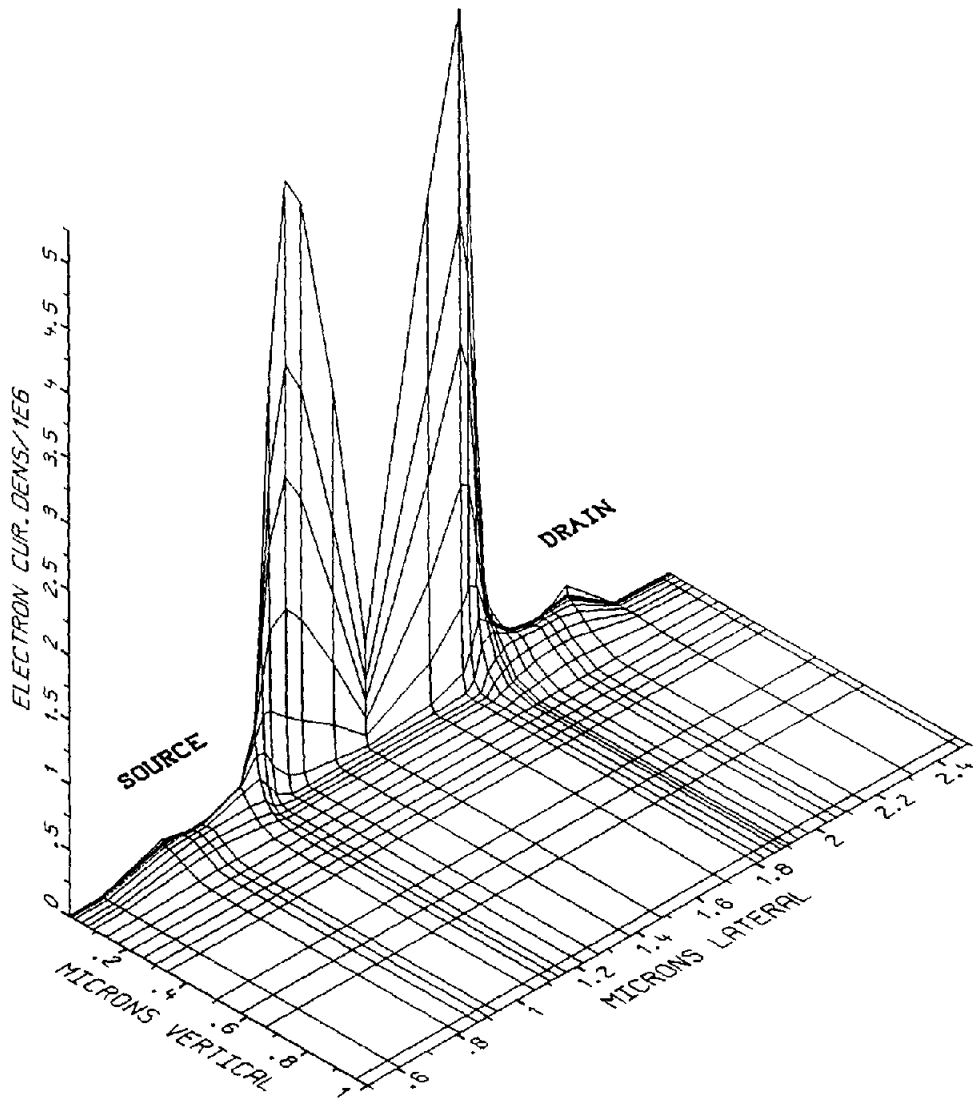

Fig. 15. Modulus of electron current density in the channel region 10 ps after the gate voltage pulse.

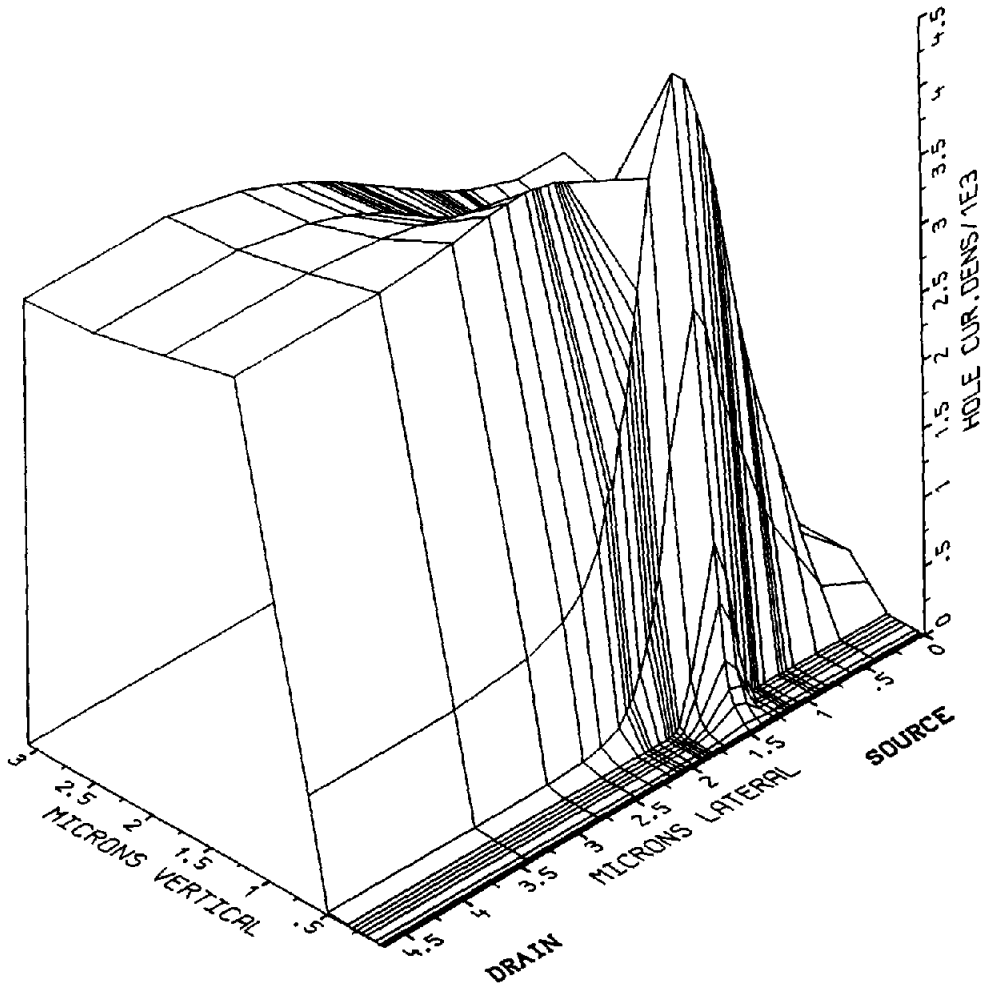

Fig. 16. Modulus of hole current density in the whole device 1 ps after the gate voltage pulse.

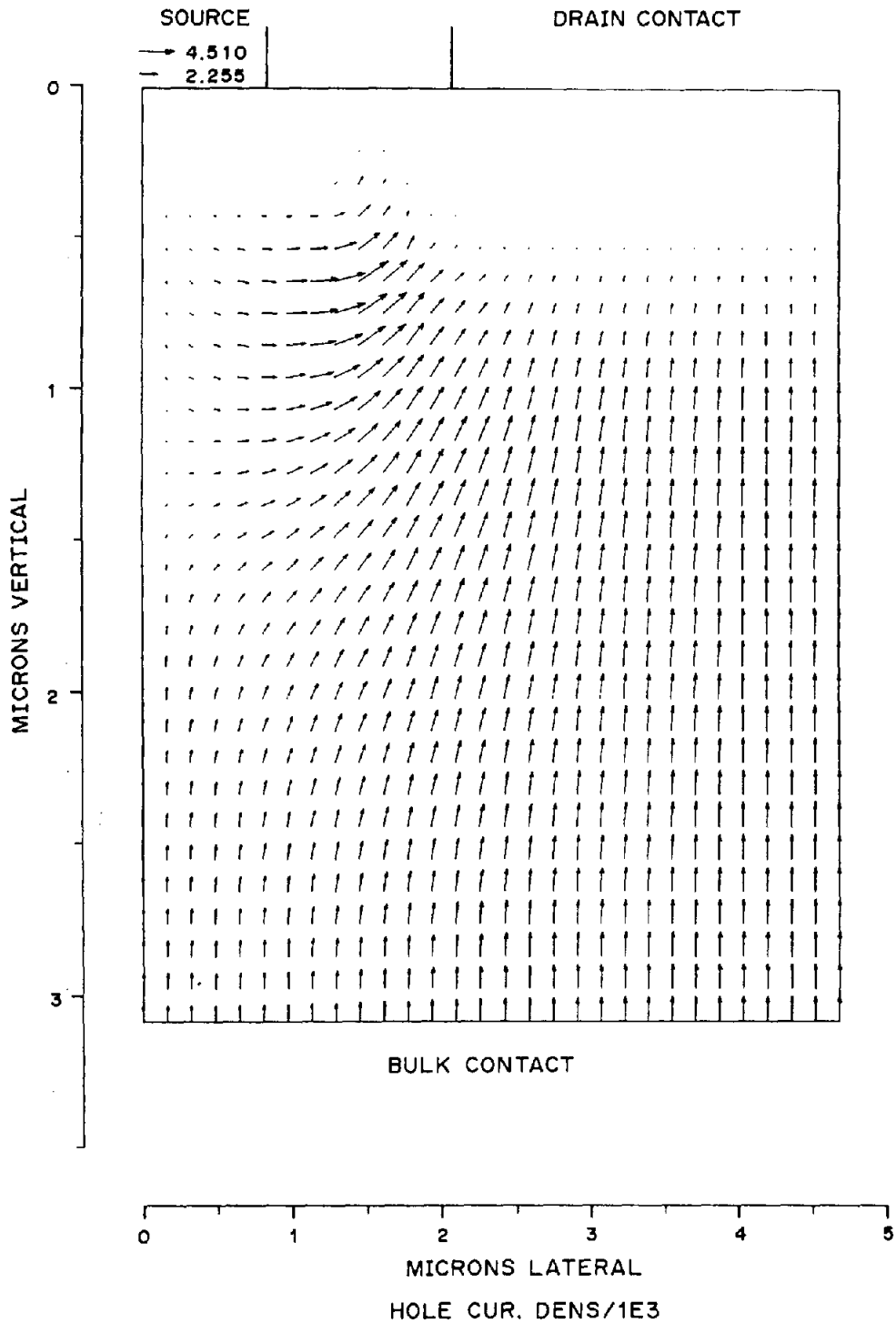

Fig. 17. Direction of the hole current density in the whole device 1 ps after the gate voltage pulse. The length of the arrows corresponds to the modulus of the hole current density in 10^3 Acm^{-2} at each point as indicated in the left upper corner.

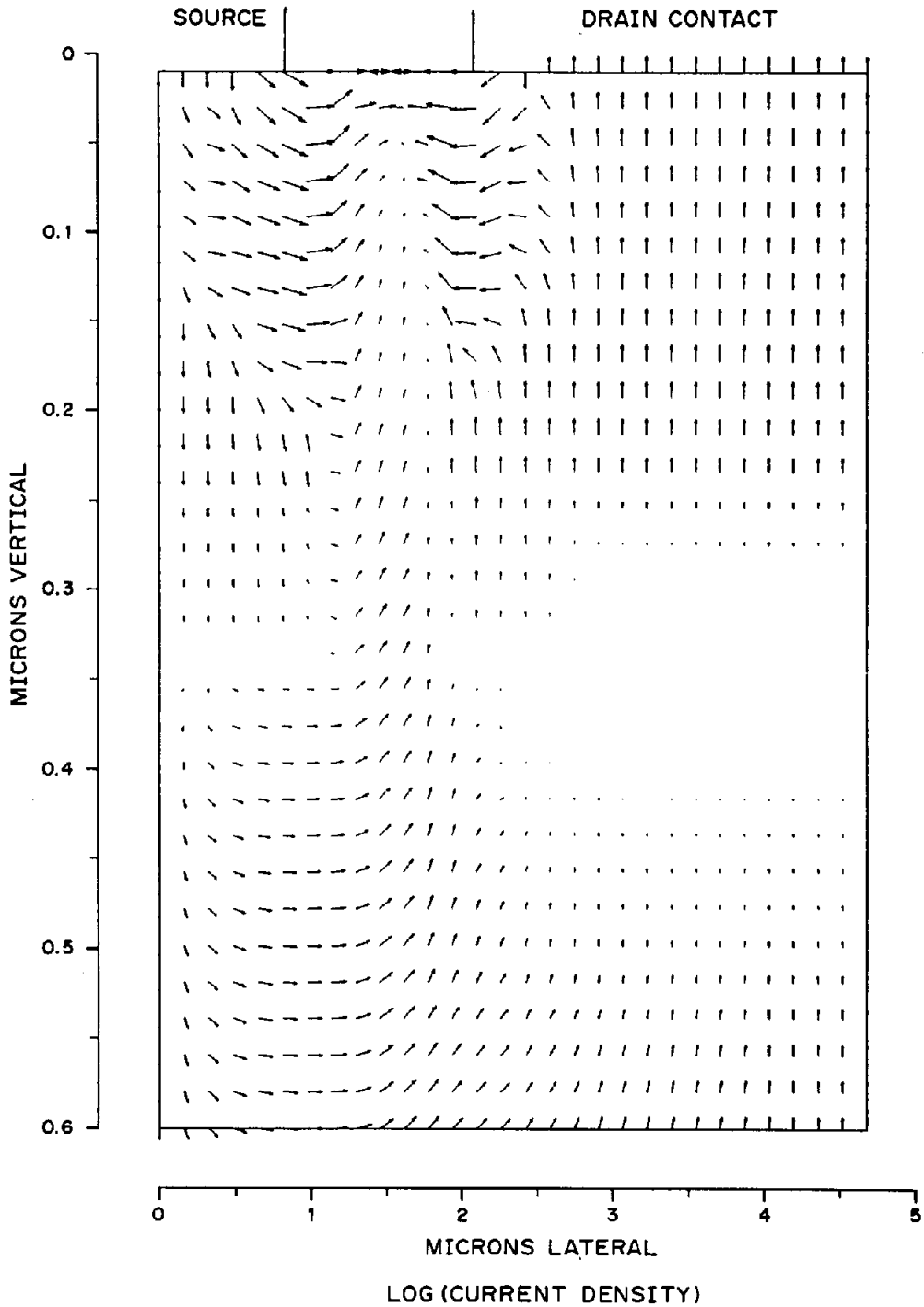

Fig. 18. Direction of the convection current density in the upper part of the device 1 ps after the gate voltage pulse.

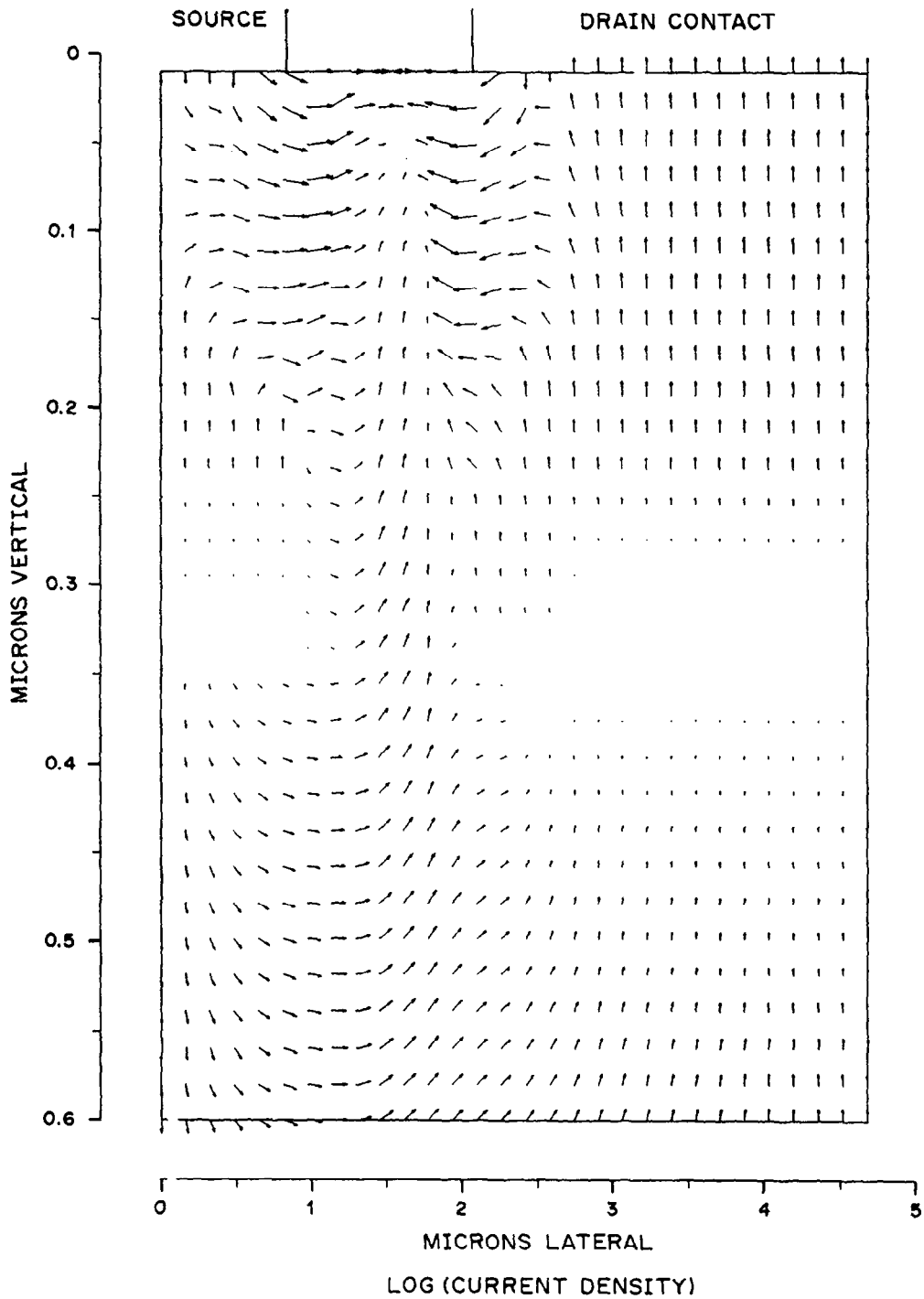

Fig. 19. Direction of the convection current density in the upper part of the device 3 ps after the gate voltage pulse.

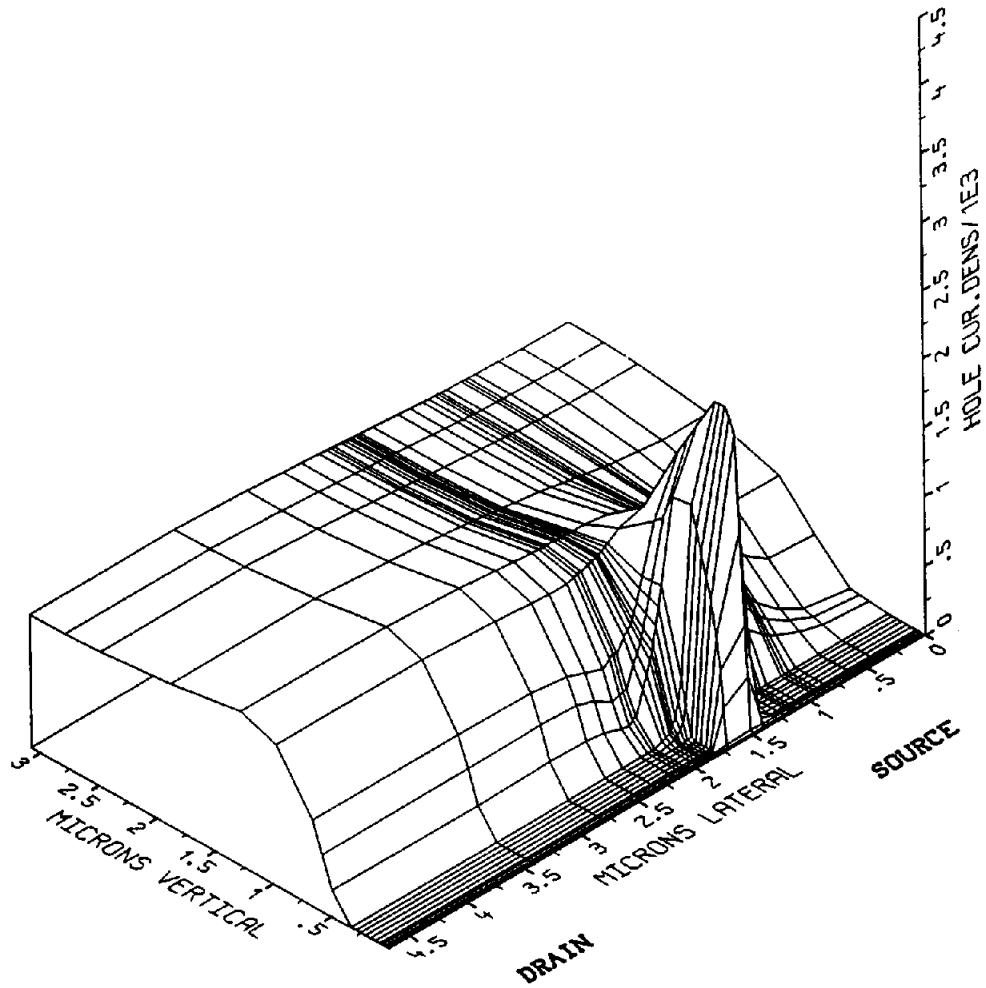

Fig. 20. Modulus of the hole current density in the whole device 10 ps after the gate voltage pulse.

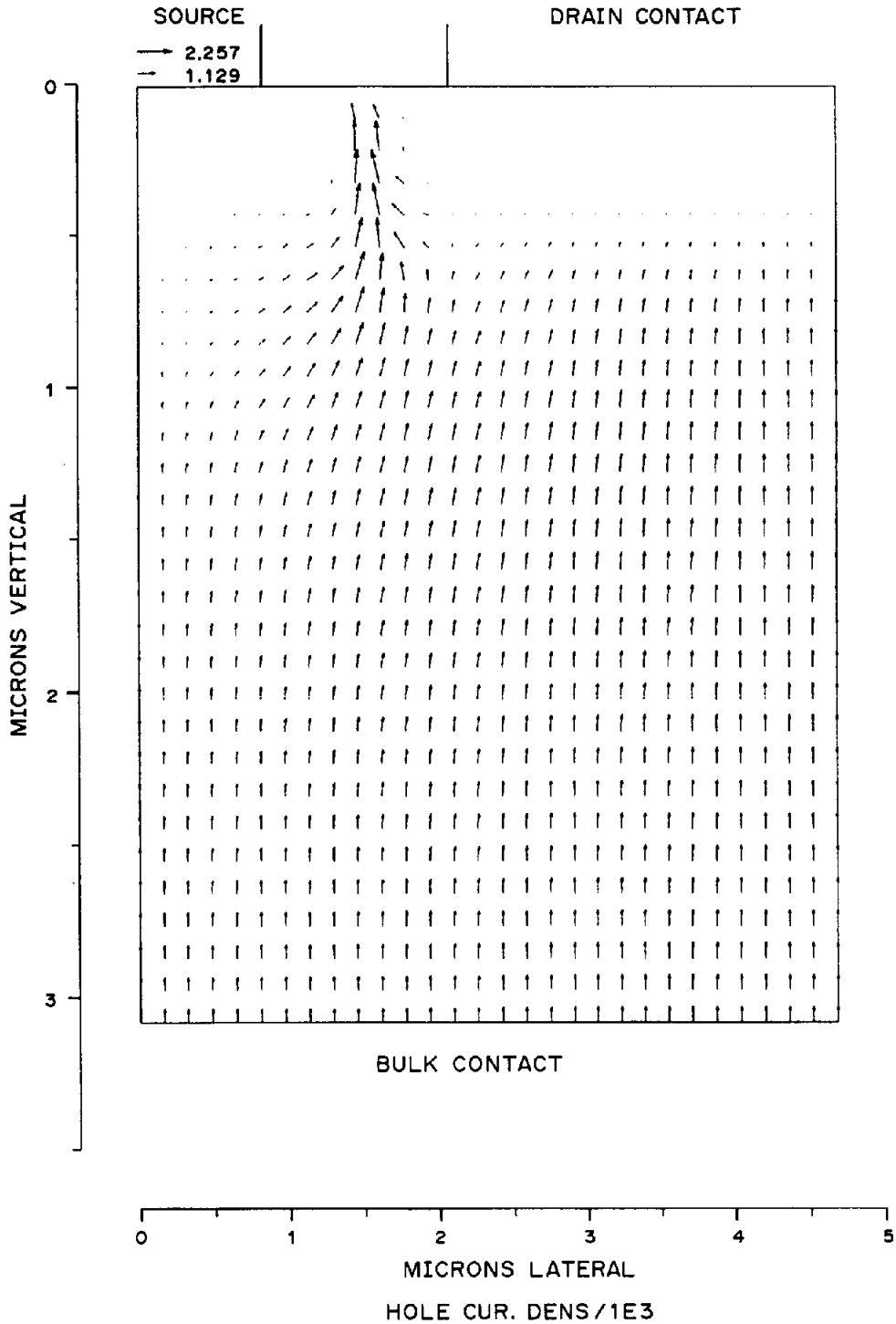

Fig. 21. Direction of the hole current density in the whole device 10 ps after the gate voltage pulse.

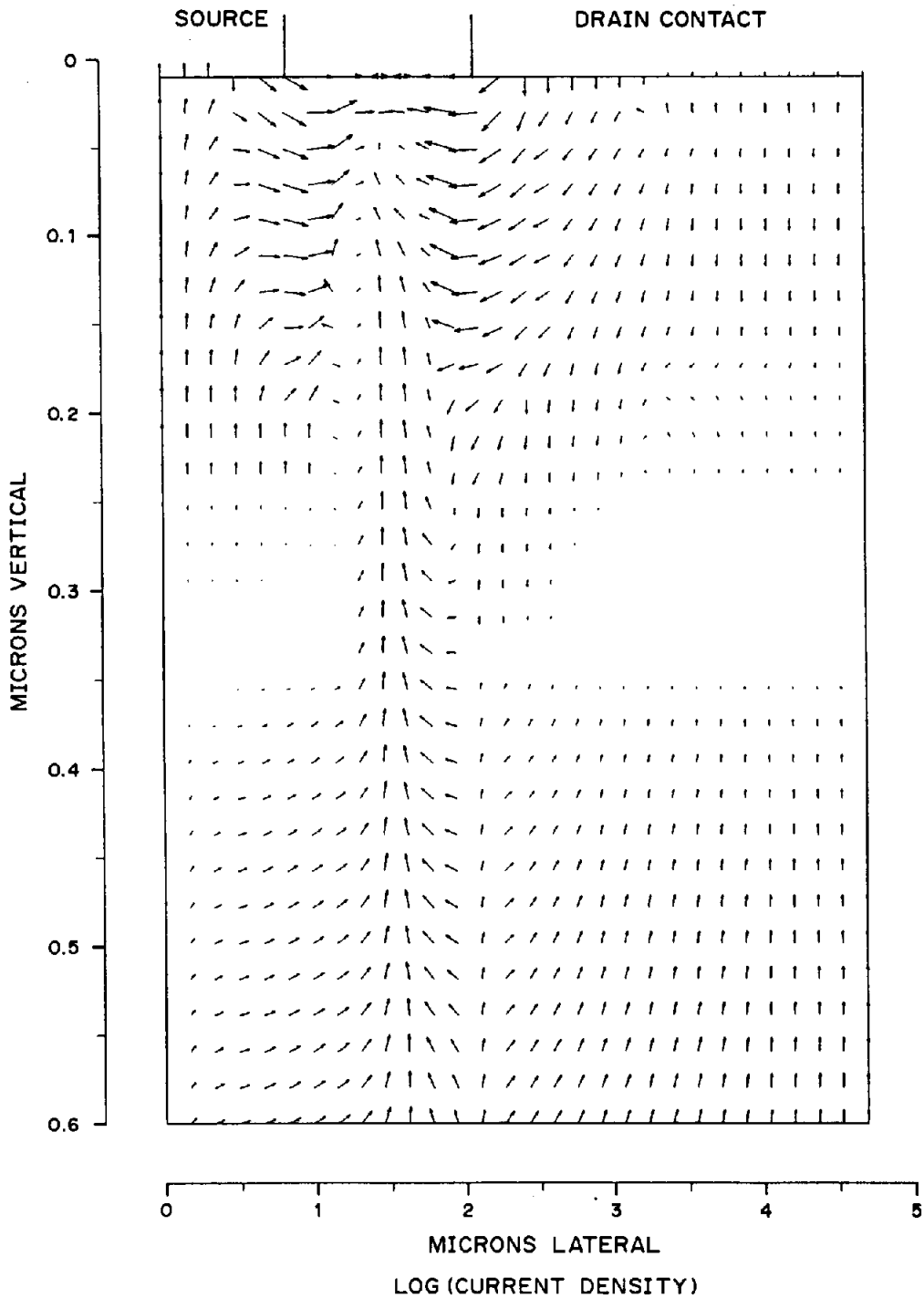

Fig. 22. Direction of the convection current density in the upper part of the device 10 ps after the gate voltage pulse.

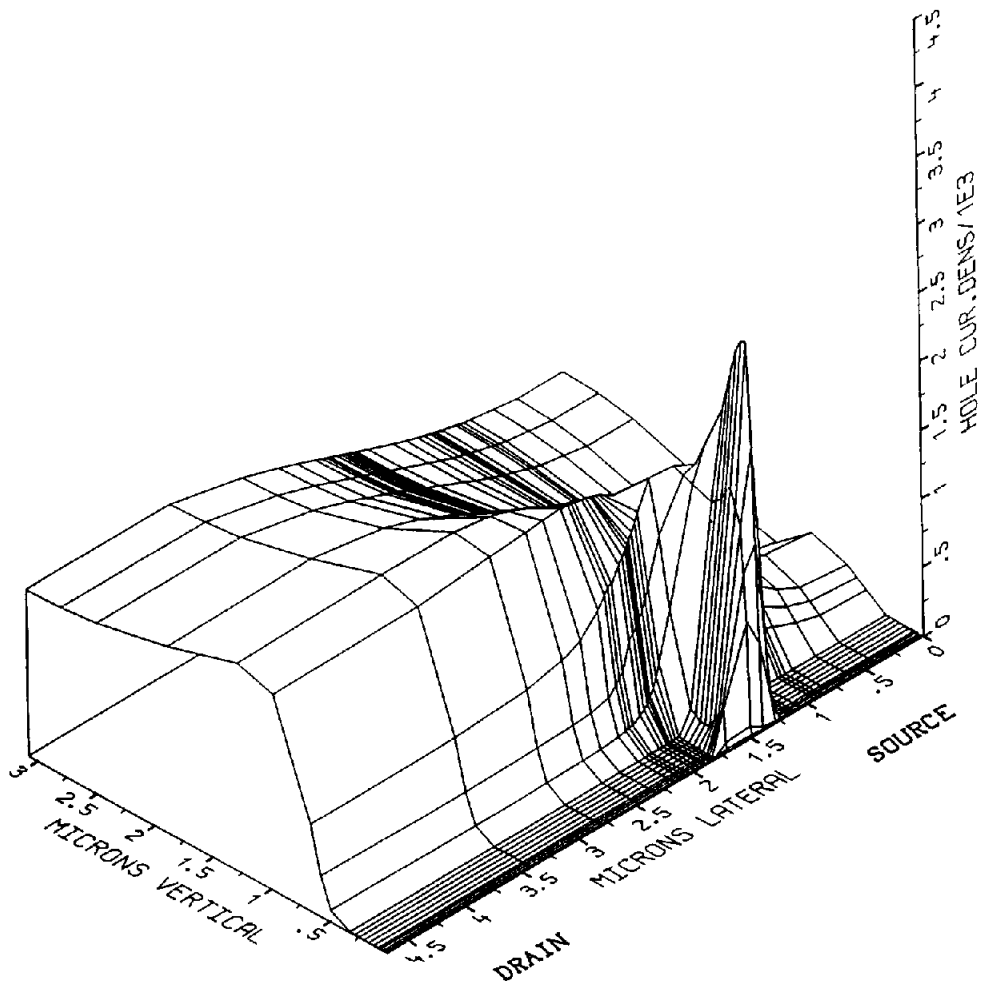

Fig. 23. Modulus of hole current density in the whole device 25 ps after the gate voltage pulse.

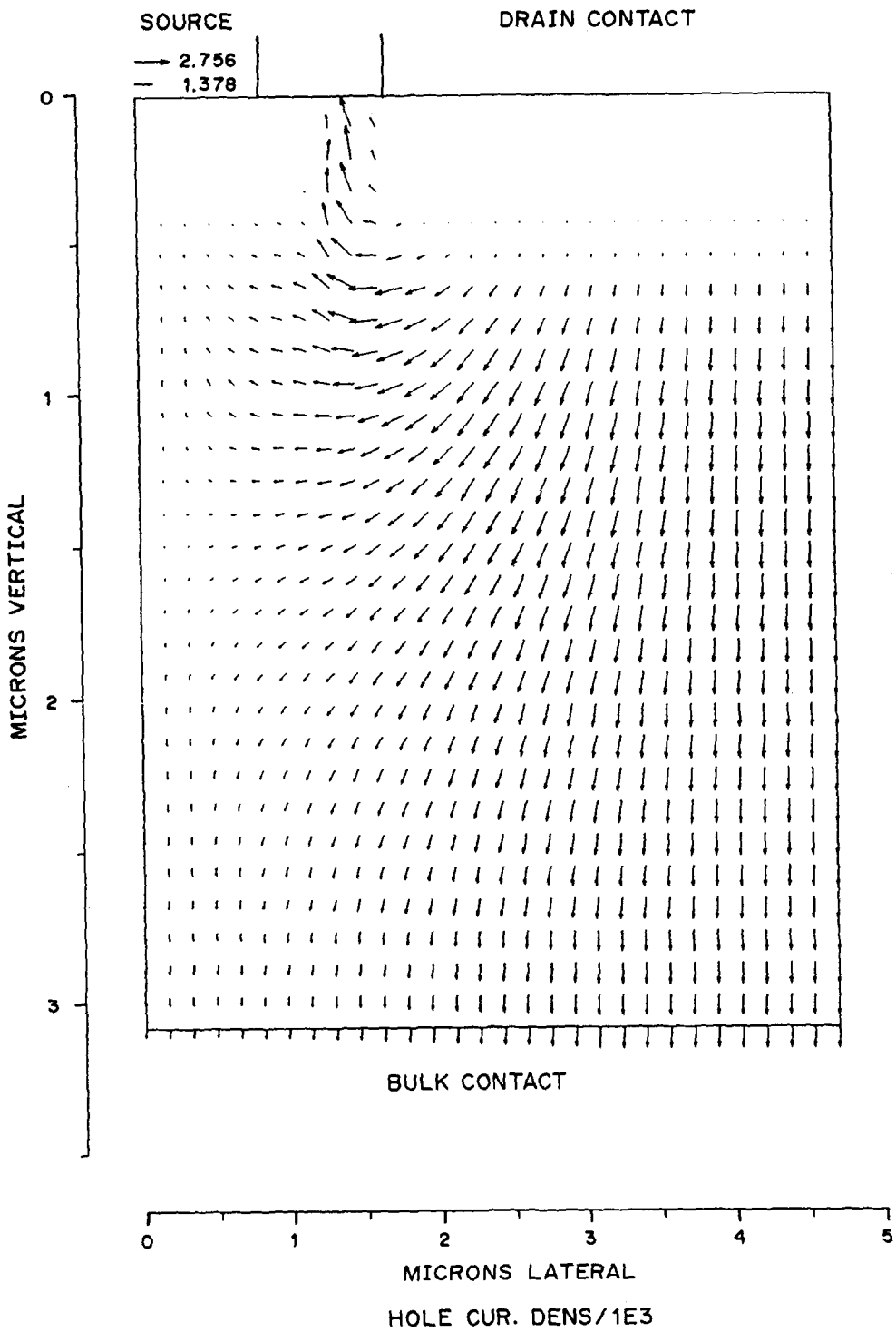

Fig. 24. Direction of the hole current density in the whole device 25 ps after the gate voltage pulse.

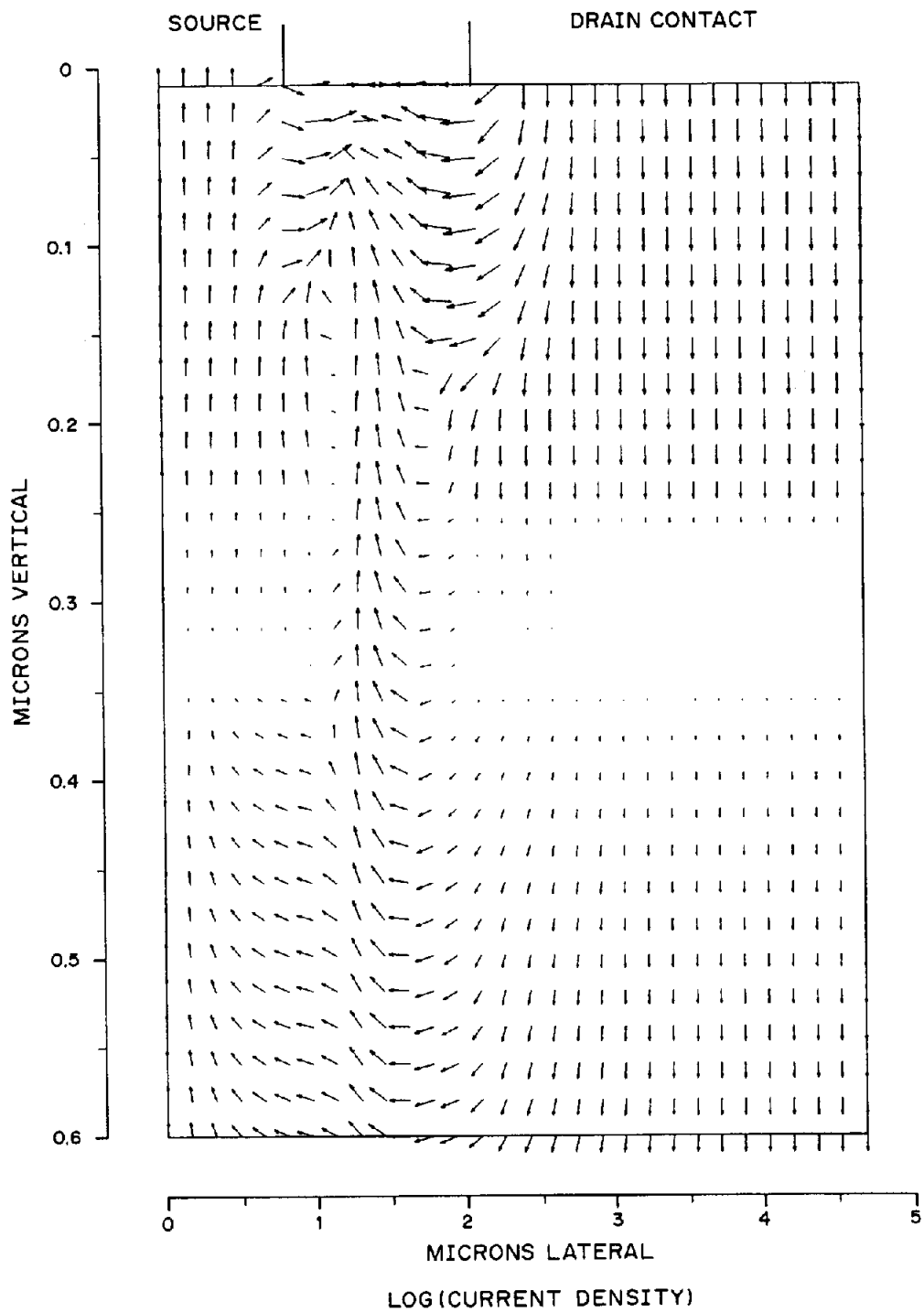

Fig. 25. Direction of the convection current density in the upper part of the device 25 ps after the gate voltage pulse.

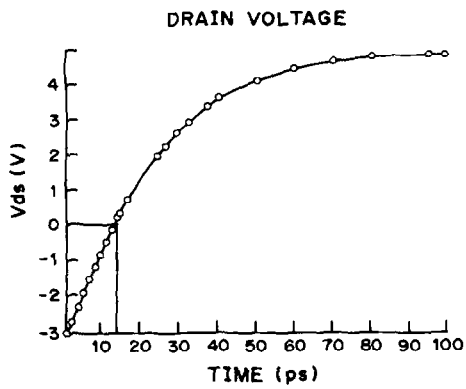

Fig. 26. Voltage of the drain contact vs time after the gate voltage pulse.

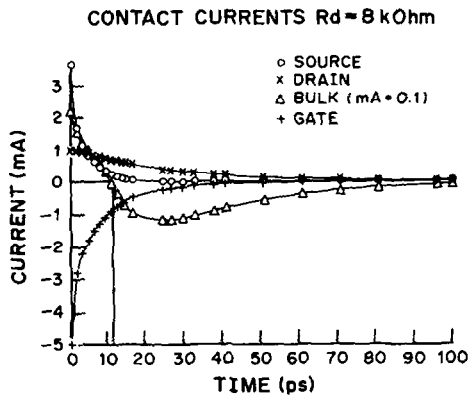

Fig. 27. Terminal currents vs time after the gate voltage pulse.

is increased by that part. After the ramp the gate voltage remains zero. The still existing negative gate current indicates that the potential at the semiconductor–oxide interface is negative.

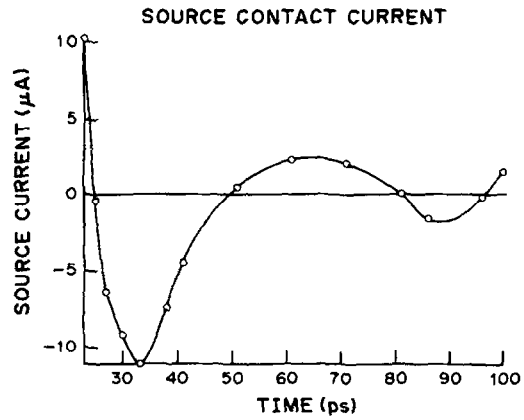

Fig. 28. Source contact current vs time after 20 ps.

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