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Two-Dimensional Simulation of a Bipolar Dynamic Memory Cell

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Abstract — A two-dimensional transient analysis of a I^2L dynamic memory cell is presented. The behaviour of this particular bipolar device at various operating conditions has been investigated.

Introduction

Bipolar transistors are used in many dynamic memories. In these devices the stored charge of a capacitor determines the information, in contrast to static Flip-Flop devices. A two-dimensional transient analysis of a I^2L dynamic memory cell is presented. The behaviour of this particular bipolar device at various operating conditions has been investigated.

Operation of the memory cell

In Fig. 1 a cross sectional view of a dynamic I^2L-cell is shown. The word line W_p is connected to the p-type injector, the row-select line is the collector terminal of the npn-transistor (Fig. 2). The heavily doped buried n^+-region represents the column select line. The logic is determined by presence or absence of charge stored in the emitter junction depletion layer capacitance C_1 of the npn-device. A junction voltage of 3V denotes a logical 1, a voltage of 0V a logical 0, respectively.

The capacitance of C_1 can be discharged by leakage currents through the reversed biased junctions. So periodic refreshing at short intervals (1ms) is required. These simple cells cannot be read without destroying the information, therefore after each reading step the information must be renewed by writing. The cells of a column are seperated from each other by recessed - oxide isolation walls.

To write a logical 1 into the cell or to read, the row select line is lowered to a voltage of 0V. Transistor T_2 conducts in inverse mode, charging C_1 to about 3V. If a logical 1 is stored, there is no transient current in the column select line, the capacitance C_2 discharges through T_2 and the voltage across C_1 is almost 3V. Otherwise if a logical 0 is stored, this is indicated by the current that is necessary to charge C_1. There is no need of sensitive read amplifiers because this current (base current of T_2) is amplified by T_2, inducing a voltage decrease of about 200mV [1] at the column select line. A refresh cycle is accomplished by a read operation followed by a rewrite if the stored bit was a logical 0.

To write a logical 0, the column select line is lowered to about 2.25V, W_p is raised from 0V to 3V. Transistor T_2 is in active operation mode with V_1 equal to -0.75V, at resuming standby C_1 discharges through T_2 making V_1 to 0V.

Simulations

Our simulations have been performed by the two dimensional transient device simulator BAMBI, which solves the three basic semiconductor equations utilising a 'Finite Boxes' [2] discretization. The results are based on a totally selfconsistent solution. The timing diagrams (Fig. 3, Fig. 4) of write 1 / read (0ns - 60ns) and write 0 / read operation (70ns - 250ns) show the applied voltages and the resulting transient currents at the different contacts. Before the first read operation a logical 1 was stored (no appreciable transient current), before the second read operation a logical 0 was stored (transient current in column select line, see arrow). The electron- and hole-distributions, respectively, the potential in the device at logical 1 (Fig. 5, 6, 7) and logical 0 (Fig. 8, 9, 10) condition show nicely the different operating conditions. The absence of current during the read operation after a stored 1 and the apparent current in the column select line after a stored 0 are in excellent agreement with literature [3].

Conclusion

We have presented a fully two-dimensional analysis of the transient behaviour of a dynamic I^2L-storage cell. Based on such simulations the layout of this type of devices can be optimized in a short time. One transient computation took 12 hours CPU-time on a VAX-8800. An analysis of a static I^2L-storage is under investigation.

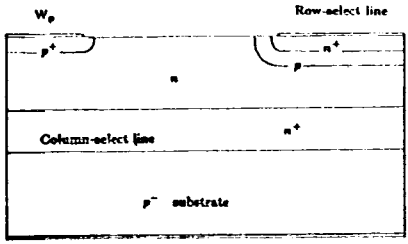

Fig.(1) Geometry

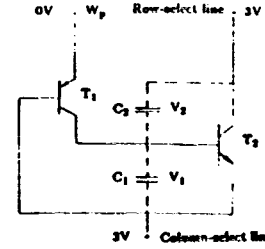

Fig.(2) Cell schematic with standby voltages

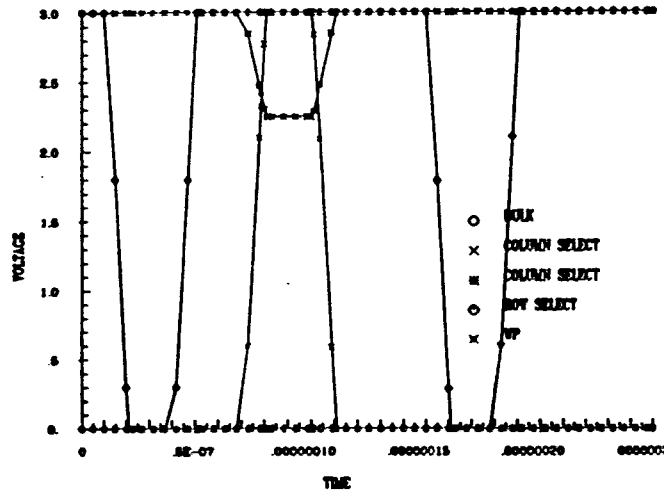

Fig.(3) Voltage / time diagram

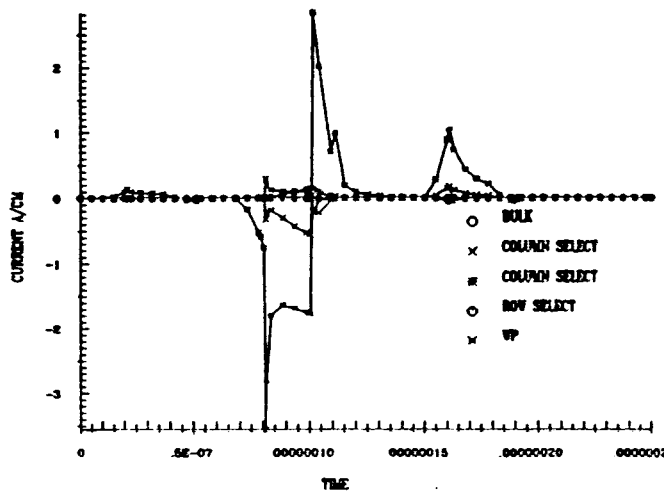

Fig.(4) Current / time diagram

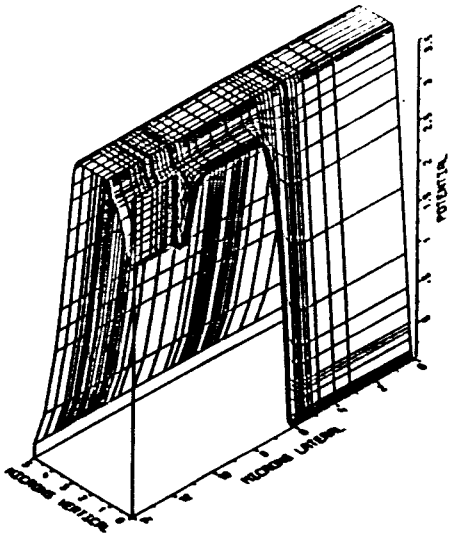

Fig.(5) Potential at logical 1

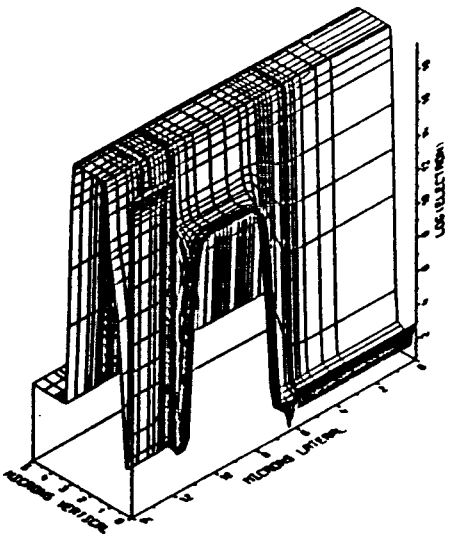

Fig.(6) Electron distribution at logical 1

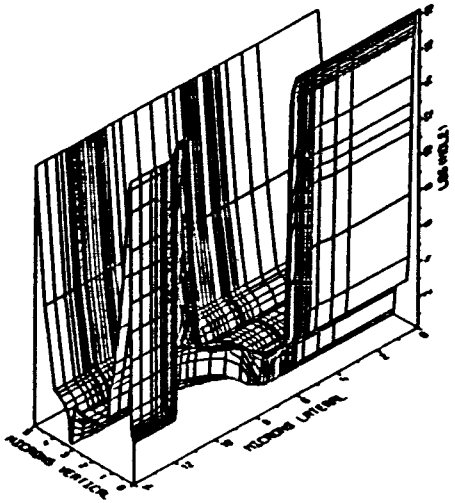

Fig.(7) Hole distribution at logical 1

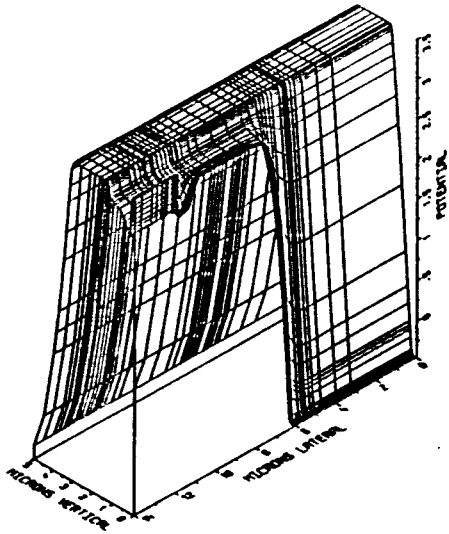

Fig.(8) Potential at logical 0

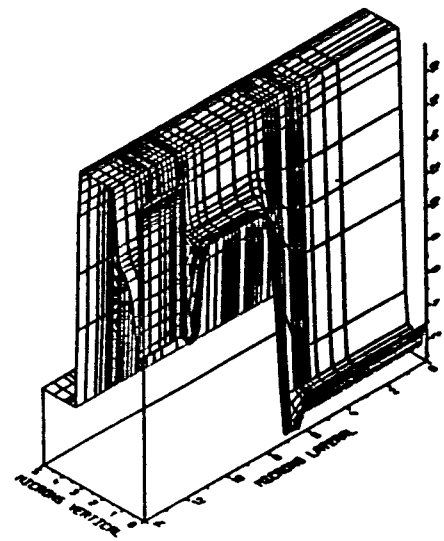

Fig.(9) Electron distribution at logical 0

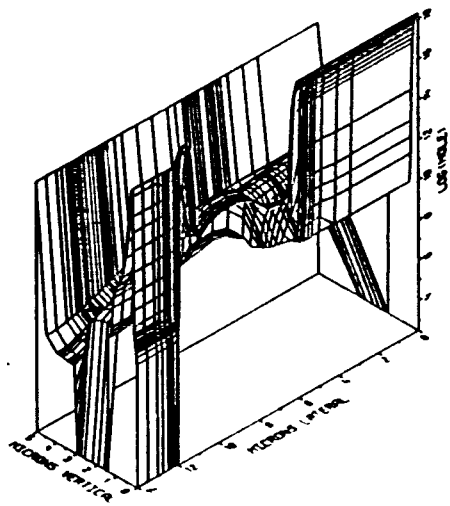

Fig.(10) Hole distribution at logical 0

Acknowledgements

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