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Numerical simulation of MOS devices with non-degenerate gate

Predrag Habaš and Siegfried Selberherr
Institute for Microelectronics
Gußhausstrasse 27-29, 1040 Vienna, Austria

Abstract. In order to analyze implanted polysilicon-gate devices our MOS-device simulator MINIMOS has been extended to solve the basic semiconductor equations also in the poly-gate area self-consistently. Heavy doping effects in the gate as well as surface charge at the gate/oxide interface have been taken into account. The impact of some technological parameters related to the poly-gate effect on MOS-device performance is studied.

1. Introduction

Implanted gate MOS-devices have become common in submicron technologies. Due to higher diffusivity of the impurities along the grain boundaries in polysilicon compared to the single crystal it is possible to achieve high chemical concentration of the impurities near the gate/oxide interface, although the poly-gate thickness is larger than source/drain junctions depth. However, a significant part of the impurities (phosphorus or arsenic) segregate at grain boundaries and remain there non-activated after annealing (Mandurah et al. 1980). Therefore, the activated impurity concentration at the gate/oxide interface in N-type gates can be significantly lower than the chemical concentration (Sun et al. 1988), which depends on many parameters of the technological process (e.g. type of impurity, grain size, annealing cycle). The chemical concentration of impurity in P-type gates is usually lower than in N-type. Schwalke et al. (1988) report a saturation of boron chemical concentration at $1 \div 2 \cdot 10^{19} cm^{-3}$ in silicide/polysilicon gate structures. Therefore, in spite of high activation of boron (the absence of boron segregation at grain boundaries has been reported by Mandurah et al. 1980), the final activated impurity concentration in P-type gate can be low, too.

Shift of the high-frequency C-V curve (Wong et al. 1988) as well as the degradation of the quasi-static C-V curve (Chapman et al. 1988, Lu et al. 1989) has been experimentally observed in implanted poly-gate devices. The latter effect suggests a reduction of the driving capabilities of implanted gate devices in comparison with their degenerate-gate counterparts. These experimental findings have been related to shift of the Fermi level in poly-gate and depletion in the poly-gate near the oxide due to the penetration of the electric field into the gate (Chapman et al. 1988, Wong et al. 1988) or/and the existence of acceptor type interface traps at the gate/oxide interface (Lifshitz et al. 1983). An additional effect may be boron penetration (e.g. Tseng et al. 1990).

Consequently, the implanted (non-degenerate) poly-gate can no longer be assumed an equipotential area, especially in the modeling of thin oxide devices. We have published a 1D analytical model of thin oxide devices accounting for the potential drop in the poly-gate elsewhere (Habaš et al. 1990). In this paper, the numerical modeling of the poly-gate effect is presented, and this enables us to account for realistic doping profiles and 2D effects in submicron devices.

2. Model

We have extended MINIMOS to solve self-consistently the basic semiconductor equations also in the poly-gate area (in fully non-planar geometry). Poisson's equation is solved usually in the whole simulation area (from y_t until y_B – Figure 1). For the continuity equations two (in steady-state equivalent) approaches have been implemented:
1) The solution of both discretized continuity equations in the poly-gate simultaneously with the bulk area (from y_G until y_B – Figure 1). Such an approach is interesting for the transient simulation.
2) In steady-state the poly-gate is in thermodynamic equilibrium (the leakage currents are negligible and net recombination vanishes) and the assumption of a constant Fermi level holds. As a consequence, the carrier concentrations in the poly-gate n,p can be calculated analytically as a function of the local potential Ψ. This approach performs the calculation in a significantly shorter computer-time than the first. It permits that the band gap narrowing and Fermi-Dirac statistics may be implemented in a simpler way. Assuming a rigid parabolic band model it follows for N-type gate:

$$n(\Psi) = N_c F_{1/2}\left[(\Psi - \Psi_G + \Phi_{fc} + \delta \mathrm{E}_c - \delta \mathrm{E}_{cG})/U_T\right] \quad ; \quad \Phi_{fc} = U_T F_{1/2}^{-1}\left(N_{gG}/N_c\right)$$

where N_c is the effective density of states for conduction band, $\delta \mathrm{E}_c$ is the local shift of the conduction band due to band gap narrowing, and N_g is the activated impurity concentration in the gate. The index G denotes the quantities at the gate–polysilicon contact (y_G at Figure 1). For $p(\Psi)$ an analogous relation holds. The top gate potential (boundary condition) is given by

$$\Psi_G = \Phi_{fc} - \delta \mathrm{E}_{cG} + U_{GS} + (\mathrm{E}_{co} - \mathrm{E}_{io})$$

with respect to the Fermi level in the source, where U_{GS} is the terminal voltage and E_{co},E_{io} denote the conduction band edge and the intrinsic level in the ideal silicon band. These equations account properly for a position dependent band gap narrowing, and ensure that the potential Ψ is continuous in the total simulation area. The analogous model has been implemented for a P-type gate. Fermi integrals $F_{1/2}$ can be calculated efficiently by analytical approximations (e.g. Blakemore 1982).

The charge at the polysilicon-gate/oxide interface affects the field in the gate at the gate/oxide interface, and changes remarkably the potential drop in the gate (Habaš et al. 1990). Therefore, a fixed oxide charge and interface trapped charge at the polysilicon/oxide interface have been incorporated in simulation. If N_g is several times higher than the equivalent volume trap density in polysilicon, the trapped charge is negligible compared to the space charge due to impurity ions. Since we restrict ourselves to $N_g > 10^{18} cm^{-3}$, the traps at the grain boundaries have not been taken into account in the present model.

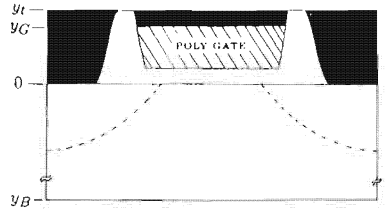

Figure 1: Simulation area

3. Simulation results and discussion

Figure 2 shows the distribution of the potential and the electron and hole concentrations in the gate of N-channel/N-gate device. Due to thin oxide ($8nm$), low ionized impurity concentration at the gate/oxide interface ($5 \cdot 10^{18} cm^{-3}$) and high gate bias ($U_{GS} = 5V$), a significant potential drop appears in the gate (inversion in the gate). In spite of high drain bias ($U_{DS} = 5V$) (which reduces the gate–channel potential difference), there is inversion in the gate along a significant part of the channel, due

to the convex shape of the channel potential. The threshold voltage and the potential drop in the poly-gate versus ionized impurity concentration N_g are shown for a P-gate/P-channel device in Figure 3. The charge at the gate/oxide interface Q_{go} (here assumed as fixed) has a strong influence on the threshold voltage. There is not much information about the nature of Q_{go} in literature. Yaron et al. (1980) obtained experimentally a positive total (fixed and trapped) interface charge of order $\sim 10^{12} cm^{-2}$ for the polysilicon deposited over thermally grown oxide. Such a large positive charge lowers significantly the field penetration into the gate in N-channel devices, but it increases the potential drop in the gate in P-gate/P-channel devices (Habaš et al. 1990). It is necessary to account for this charge in the analysis of the threshold voltage instability of thin oxide devices.

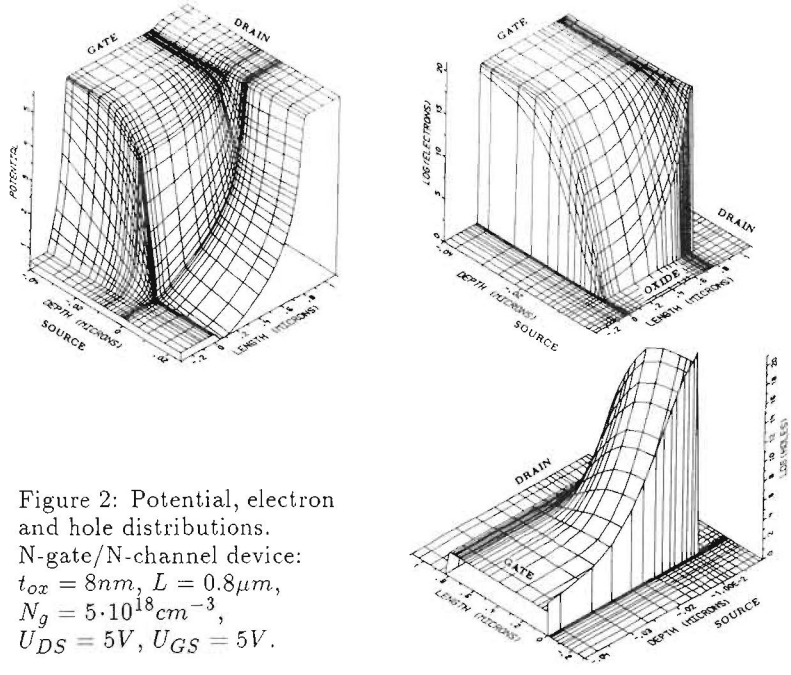

Figure 2: Potential, electron and hole distributions. N-gate/N-channel device: $t_{ox} = 8nm$, $L = 0.8\mu m$, $N_g = 5 \cdot 10^{18} cm^{-3}$, $U_{DS} = 5V$, $U_{GS} = 5V$.

The fall-off of the drain current in the linear region with N_g as parameter is shown in Figure 4. The charge Q_{go} has a minor influence, and N_g is the main parameter in determination of the drain current degradation. The inversion in the gate causes a kink in the curve 10^{18}, leading to the recovery of the transconductance (experimental finding by Lu et al. 1989). There is a recovery of the quasi-static C-V curve, too (obtained experimentally by Chapman et al. 1988, Lu et al. 1989). In order to suppress the reduction of the gate drive, the activated impurity concentration in the gate at the gate/oxide interface must be higher than $10^{19} cm^{-3}$ for $10nm$-oxide devices. Note that the Fermi-Dirac statistics has a small influence on the analysis performed.

The poly-gate effect depends approximately on $t_{ox}^2 N_g / U_{GS}$. It seems that it will not become more severe in deep submicron devices, because of the restricted reduction of the oxide thickness (down to $\sim 5nm$) and significant reduction of the supply voltage established in literature. However, Okazaki et al. (1990) have recently reported a $3.5nm$-thick oxide subquarter-μm CMOS technology with $2V$ proposed supply voltage.

The N_g necessary to suppress the gate effect at the supply voltage is for such a device at least four times higher than for the device at Figure 4. The gate effect will be also important regarding the possible application of Ta_2O_5 as gate-insulator (see e.g. Nishioka et al. 1987), because the gate effect depends on the square of the insulator permittivity.

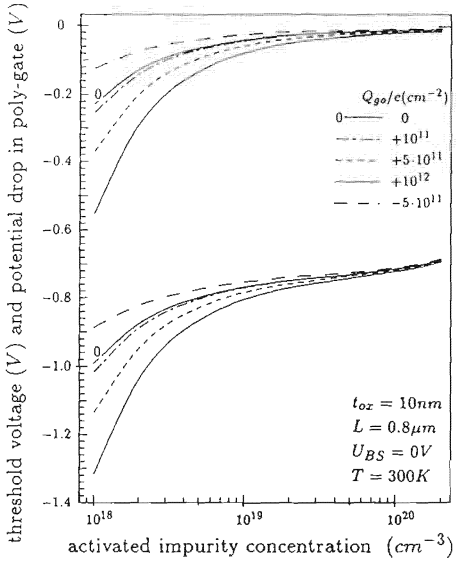

Figure 3: Threshold voltage dependence. Parameter Q_{go} is fixed charge density at gate/oxide interface.

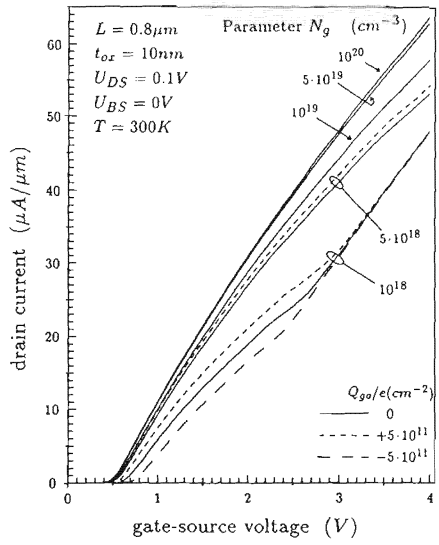

Figure 4: Linear region characteristics

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