Two Dimensional Simulation of Thermal Runaway in a Nonplanar GTO-Thyristor

H. Brand and S. Selberherr
Institute for Microelectronics, Technical University of Vienna
Gußhausstraße 27-29, A-1040 Vienna, Austria

Abstract

The problem of electrothermal stability due to different cooling conditions has been investigated by computation of thermal transients of a nonplanar GTO-thyristor. In the first simulation an equilibrium situation occurs with the heat sink removing all the dissipated power. In the second simulation the internal behaviour of the GTO-thyristor during severe thermal runaway is analyzed to explain its basic mechanisms.

1 Introduction

Thermal runaway is a phenomenon of electrothermal interaction where the dissipation of electrical energy causes a temperature rise over an extended area of the device resulting in increased current flow and further dissipation until unrecoverable device failure or burn out of the device occurs. In this paper 'global' thermal runaway due to bad cooling conditions will be focused, in contrast to secondary breakdown which often is explained as 'localized' thermal runaway.

2 The mathematical model

Accurate simulation of transient self-heating effects in semiconductor devices requires the self-consistent solution of the semiconductor equations and the heatflow equation in space and time.

The gradients of the lattice temperature, the carrier concentrations and an effective electric field act as driving forces for the electron $\vec{J_n}$ (1) and hole $\vec{J_p}$ current density (2) [5]. The effective electric field describes bandgap narrowing effects. The simple model for the heatflow J_{th} in equation (3) does not include the Peltier effect.

$$\vec{J_n} = qn\mu_n(\vec{E} - \frac{kT}{q}\text{grad}(\ln n_{ie})) + qD_n\text{grad}\, n + qnD_n^T\text{grad}\, T \tag{1}$$

$$\vec{J_p} = qp\mu_p(\vec{E} + \frac{kT}{q}\text{grad}(\ln n_{ie})) - qD_p\text{grad}\, p - qpD_p^T\text{grad}\, T \tag{2}$$

$$\vec{J_{th}} = -\kappa\text{grad}\, T \tag{3}$$

TH0424 - 2/92/0000-0129 $1.00 © 1992 IEEE

μ_n and μ_p are the mobilities, D_n and D_p the diffusivities. D_n^T and D_p^T denote the thermal diffusion coefficients. κ is the thermal conductivity.

The electrical system is coupled to the thermal system because recombination, mobility and intrinsic carrier density depend on temperature [5], the temperature gradient acts as a driving force and the heat generation is a function of electrical variables [7].

As no experimental data are available the modeling of physical parameters in the high temperature regime is problematic. Further investigations are necessary. The dependence of the recombination rate and the mobility on temperature has been taken from [5]. The effective intrinsic carrier density n_{ie} as a function of temperature has been fitted to the data from [6]. Furthermore Auger recombination and carrier-carrier scattering - known as limiting physical effects for high injection conditions in power semiconductor devices [1] - have been taken into account. The heat generation model G_{th} includes Joule heat and recombination heat, but not Thomson heat.

For the electrical subsystem either ohmic contacts or homogenous Neumann boundaries are assumed. Mixed boundary conditions (4) for the heatflow equation are mandatory to allow modeling of realistic imperfect cooling conditions (backside mounting or flip chip mounting, thermally active multilayer structures towards the bulk). h denotes the heat sink thermal conductance, T_{sink} is the ambient temperature of the heat sink.

$$J_{th} = h(T - T_{sink}) \tag{4}$$

The proper modeling of imperfect cooling conditions is of special importance for transient electrothermal simulations as the time constant for self heating increases with increasing external thermal resistances.

Usually the characteristic time for the electrical and the thermal subsystem differ by several orders of magnitude. Thus a device is in steady state from the electrical point of view, whereas thermally it is still in transition. Therefore the electrical transient can be neglected with respect to the thermal transient, an assumption which is well satisfied in practice [2], [3].

Spatial discretization is done with finite boxes [5], time discretization with backward Euler method. The electrothermal problem is computed selfconsistently following a decoupled approach. At each timestep the electrical subsystem is solved first regarding the lattice temperature as an independent variable. Then the temperature distribution is updated by solving the heatflow equation. Newton's method and LU-decomposition is used to solve the electrical and thermal subsystem alternately until convergence.

3 Results

A GTO-thyristor is investigated. The data are taken from [4]. First the electrical steady state is computed for the thyristor in the on-state, where significant current filamentation occurs. The anode voltage is 3.3 V, the anode current 28 A. Then the subsequent thermal transients are calculated. The heat sink temperature is 300 K. Double sided cooling is assumed.

The heat sink thermal conductance is 50 W/cm^2K in the first simulation. Fig. 1 shows the evolution of the internal maximum and minimum temperature in time. Thermoelectric

equilibrium is reached after 3 milliseconds with the heat sinks removing all the dissipated power P_d.

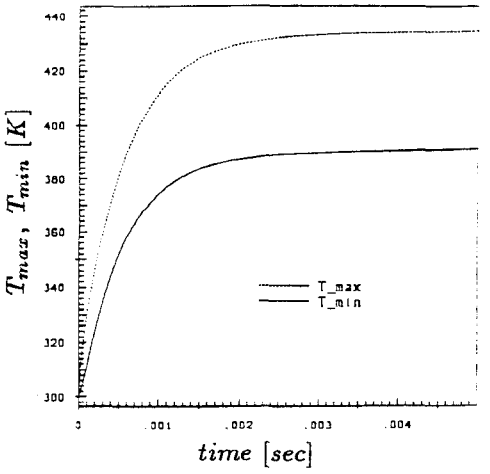

Fig. 1: time evolution of maximum and minimum temperature when the heat sink thermal conductance is 50 $Wcm^{-2}K^{-1}$ and the heat sink temperature is 300 K

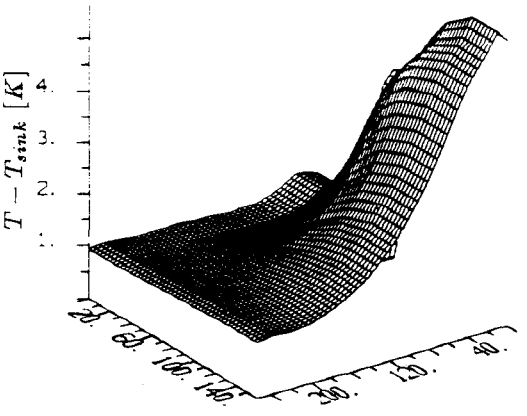

Fig. 2: increase of lattice temperature in Kelvin after 10^{-5} seconds

The data correspond very well to the analytic solution of an equivalent thermal network, consisting of thermal capacitor and thermal resistor. Equation (5) describes the step response of the temperature in time.

$$\Delta T = R_{th} P_d (1 - \exp(-\frac{t}{R_{th} C_{th}})) \tag{5}$$

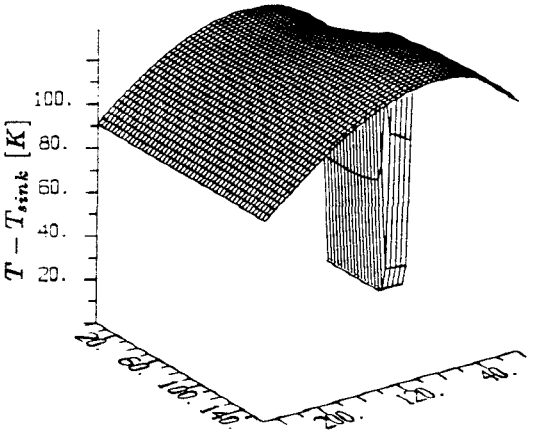

Fig. 3: increase of lattice temperature in Kelvin after 5 milliseconds

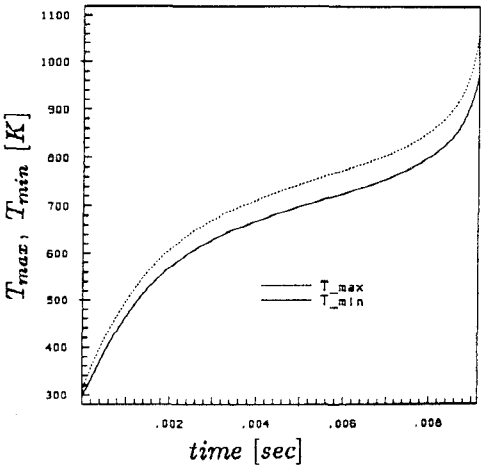

Fig. 4: time evolution of maximum and minimum temperature when the heat sink thermal conductance is 5 $Wcm^{-2}K^{-1}$ and the heat sink temperature is 300 K (thermal runaway)

Figs. 2-3 are snapshots of the internal lattice temperature distribution after 10^{-5} and 0.005 seconds.

In order to induce severe thermal runaway, bad cooling conditions are defined by choosing 5 W/cm^2K for the heat sink thermal conductance. Fig. 4 shows the exponential increase of the temperature. The device is destroyed when the melting point of silicon is reached.

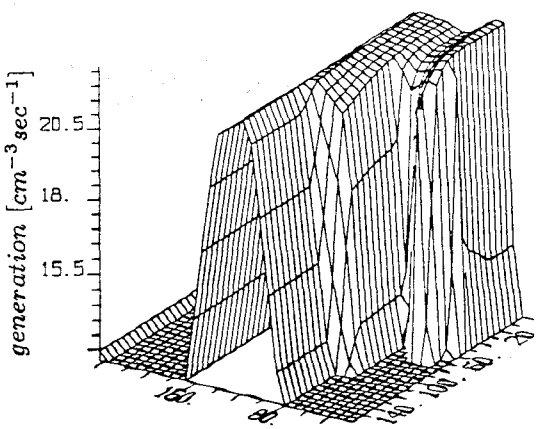

Fig. 5: thermal generation of carriers per cubic centimeter and second in case of thermal runaway after 8.65 milliseconds

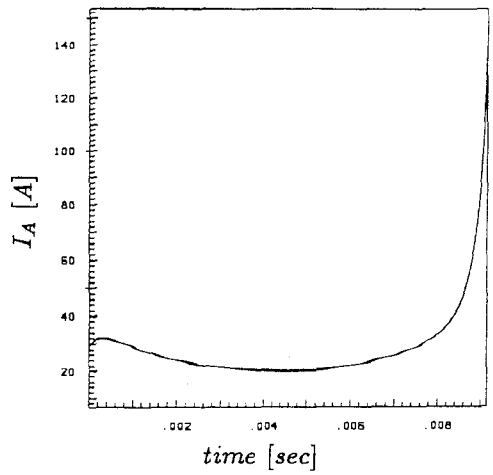

Fig. 6: time evolution of anode current in case of thermal runaway

The onset of thermal runaway occurs when thermal generation of carriers takes place not only in the small p-base region near the gate contact but covers a considerable part of the whole device. Fig. 5 shows the thermal generation after 8.65 milliseconds. Carriers are already generated thermally across the whole base of the thyristor. Fig. 6 shows the corresponding exponential increase of the anode current. The mobility dependence on temperature tends to enhance the thermal stability of the GTO. Thus the anode current temporarily decreases in Fig. 6.

In Figs. 7-10 the evolution of the dependent variables ψ, n, p and T in time is shown. The device has been cut at the center of the emitter for these plots. As the lattice temperature increases in time the doping profile loses its implication in device operation. Only the high emitter doping continues to determine the carrier densities. The rest of the device is flooded with electrons and holes which have been generated thermally. The space charge disappears as the temperature profile rises. Thus Poisson's equation degenerates to Laplace's equation and the potential drops linearly between the anode and emitter contact as can be seen in Fig. 9. The GTO thyristor structure behaves as an ohmic resistor which shorts under the given bias because of the increasing thermal conductivity modulation. Note that the boundary conditions for the potential and the carrier densities change in time due to different values of the intrinsic carrier concentration determing the built-in potential and the equilibrium concentration of electrons and holes at the contacts.

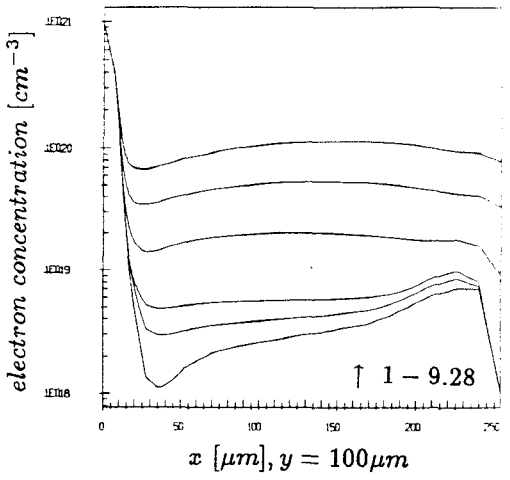

Fig. 7: electron concentration at the center of the emitter after 1 microsecond and 1, 8.2, 9.0, 9.2, 9.28 milliseconds in case of thermal runaway

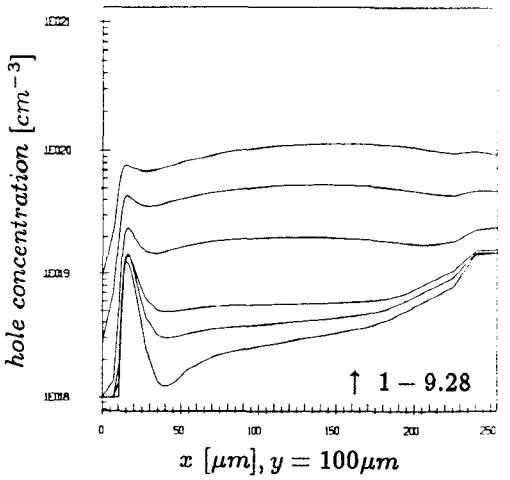

Fig. 8: hole concentration at the center of the emitter after 1 microsecond and 1, 8.2, 9.0, 9.2, 9.28 milliseconds in case of thermal runaway

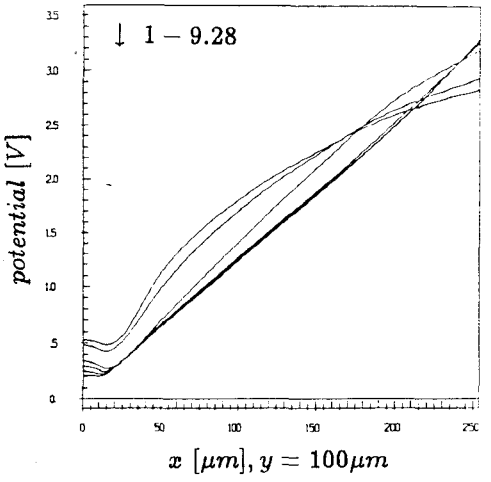

Fig. 9: potential at the center of the emitter after 1 microsecond and 1, 8.2, 9.0, 9.2, 9.28 milliseconds in case of thermal runaway

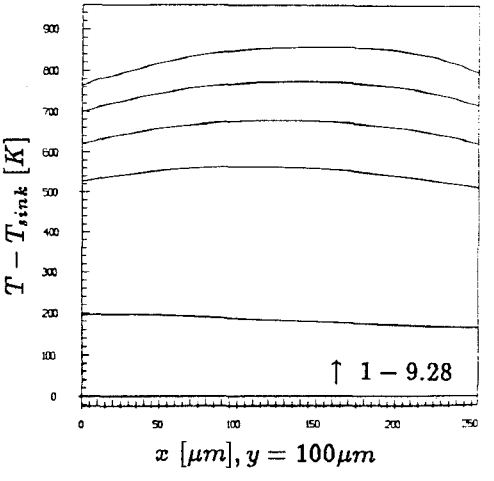

Fig. 10: increase of lattice temperature at the center of the emitter after 1 microsecond and 1, 8.2, 9.0, 9.2, 9.28 milliseconds in case of thermal runaway

As the current rises the Joule heating increases too, further raising device temperature. The instability condition is met when the increase of dissipated power with temperature is higher than the increase of dissipated power removed from the device by the heat sinks. The nonplanar device geometry between emitter and gate contact represents a perturbation of the electric field and the current densities. Thus the edge is a center of very high Joule

heating assisting thermal runaway.

The resulting temperature distribution in Fig. 10 is almost homogeneous. Most of the thermal drop is external to the device. Therefore the impact of the temperature gradient in the current relations (1), (2) is small. Only at very high temperatures thermal runaway is accellerated by a significant reduction of thermal conductivity of silicon. Thus the temperature drop within the device increases again in the upper temperature regime.

4 Conclusions

Detailed investigations of thermal stability problems of a GTO in the on-state have been presented. For the first time the internal behaviour of a thyristor during severe thermal runaway is revealed. It has been found that thermal runaway - once induced by bad cooling conditions - is dominated by the strong dependence of the intrinsic carrier density on temperature. The intrinsic carrier density follows the increase in temperature instantaneously and turns out to be the most crucial physical parameter during thermal runaway. Furthermore the simulation results allow extraction of the thermal relaxation time, the total thermal resistor and capacitor for the equivalent thermal circuit model of the device under investigation.

References

[1] M. Adler, "Accurate Calculations of the Forward Drop and Power Dissipation in Thyristors", *IEEE Trans. Electron Devices,* vol. ED-25, pp. 16-22, January 1978.

[2] A. Chryssafis, W. Love W, "A Computer-Aided Analysis of One-Dimensional Thermal Transients in $n-p-n$ Power Transistors", *Solid-State Electronics,* vol. 22, pp. 249-256, 1978.

[3] S. P. Gaur, D. H. Navon, "Two-Dimensional Carrier Flow in a Transistor Structure Under Nonisothermal Conditions", *IEEE Trans. Electron Devices,* vol. ED-23, pp. 50-57, January 1976.

[4] A. Nakagawa, D. H. Navon, "A Time- and Temperature-Dependent 2-D Simulation of the GTO Thyristor Turn-Off Process", *IEEE Trans. Electron Devices,* vol. ED-31, pp. 1156-1163, September 1984.

[5] S. Selberherr, *Analysis and Simulation of Semiconductor Devices.* Wien-New York: Springer, 1984.

[6] Sze S. M, *Physics of Semiconductor Devices.* New York: John Wiley, 1981.

[7] G. Wachutka, "Rigorous Thermodynamic Treatment of Heat Generation and Conduction in Semiconductor Device Modelling", *IEEE Trans. on CAD,* vol. 9, pp. 1141-1149, November 1990.