Investigation of the Physical Modeling of the Gate-Depletion Effect

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Abstract—**The physical modeling of the gate for the analysis of the gate-depletion effect is investigated. The accuracy of the assumed rigid-parabolic-band model is examined by comparing the numerical simulation with the experimental *C–V* data. Disagreement between calculation and measurement is observed and several physical phenomena which may be responsible for it are proposed. An engineering approach to remove the disagreement is given. The presented investigations may be of general interest for modeling of heavily doped space-charge regions.**

I. Introduction

ION IMPLANTATION has become a common way to dope the polysilicon gates in submicrometer MOSFET processes. Unlike conventional $POCl_3$-doped gates, implanted polysilicon gates may be nondegenerately doped, depending on process conditions. If the implanted gate is not doped to degeneracy, it can no longer be assumed to be an equipotential area. This is especially true when modeling thin oxide devices, since the depletion capacitance in the polygate then becomes comparable with the oxide capacitance. Nondegenerately doped gates produce several effects on MOS device characteristics: distortion of the high-frequency and the quasi-static (QS) *C–V* curves (including shift of the flat-band and threshold voltages), and reduction of the inversion layer charge and therefore drain current. These effects have been experimentally investigated in, e.g., [1]–[9], and modeled analytically in [1], [10, and references cited therein] and numerically in [11], [12]. In addition, it is necessary to account for the reduction of the oxide field (due to voltage drop in the gate) in the analysis of the Fowler–Nordheim tunneling [13] and band-to-band tunneling. In this paper, first, we present a short description of the model for the polygate area based on the rigid-parabolic-band model. This approach is examined by comparing the numerical simulation with the experimental data in Section III. This section also discusses more complex physical phenomena that come into play in the polygate, but are not included in the presented model.

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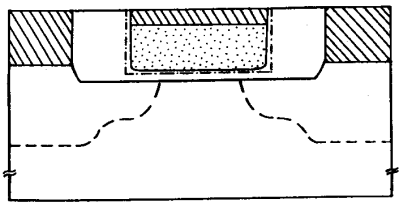

Fig. 1. Total simulation area. Dotted area is the polysilicon gate. The dot-dashed curve is the contour referred to the field flux calculation.

II. Model

If we restrict ourselves to the steady state, a thermodynamic quasi-equilibrium holds in the polysilicon gate (dotted area in Fig. 1). As a consequence of a unique and constant Fermi level, the carrier concentrations in the gate n and p can be modeled analytically as a function of the local potential Ψ. The rigid-parabolic-band model is assumed to hold at doping concentrations of interest ($\leq 10^{20}$ cm^{-3}) [14]. This is a reasonable approach to modeling of a quasi-neutral region; the same approach is often used to model heavy doped emitter and base of bipolar transistors. Regarding the modeling of a heavy doped space-charge region, there are likely to be limitations to this approach because of deep band-tails—a detailed discussion is given in Section III. Taking Fermi–Dirac statistics into account, it follows that

$$n(\Psi) = N_c \cdot F_{1/2}\left[\frac{\Psi - U_{GS} - (E_{c0} - E_{i0} - \delta E_c)/e}{U_T}\right] \tag{1a}$$

$$p(\Psi) = N_v \cdot F_{1/2}\left[\frac{U_{GS} - \Psi - (E_{i0} - E_{v0} - \delta E_v)/e}{U_T}\right] \tag{1b}$$

where $F_{1/2}$ is the Fermi integral of order $1/2$, e is the elementary charge, U_T thermal voltage, N_c and N_v are the effective density of states for conduction and valence bands, Ψ is the local potential (of the intrinsic level in the ideal band) with respect to the Fermi level in the source, the U_{GS} is the terminal voltage. E_{c0}, E_{i0}, and E_{v0} denote the energy level of the conduction band edge, intrinsic level, and valence band edge in the ideal band, respectively. Shift of the conduction band edge downward and the valence band edge upward due to bandgap narrowing is described by δE_c and δE_v. A detailed description of the

model and its implementation into MINIMOS is given in [12]. Note that we have not accounted for the traps at grain boundaries in the polysilicon gate (see Appendix).

III. Comparison with Experiment and Discussion

In this section the approach (1a), (1b) with $\delta E_{c,v}$ dependent solely on the activated impurity concentration N_g (a model often assumed in device modeling) is examined. Henceforward, a constant N_g is assumed in the whole gate area. Bandgap narrowing has a direct influence on the threshold voltage and the flat-band voltage. We assume for $\delta E_{c,v}$ an expression which agrees with rather scattered experimental data from the literature. The influence of the bandgap narrowing is, however, negligible far above the threshold and below the flat band.

Integral quantities like inversion layer charge density Q_i or bulk surface field E_{ys} are less influenced by an error in the polygate model than the differential quantities like gate capacitance C_g. Actually, the quasi-static capacitance is a sense of an inaccuracy in the space-charge model and/or interface trap model.[1] Therefore, the QS C–V curve is chosen for the comparison. We examined several p-gate/p-channel devices (t_{ox} = 9.0, 9.8, 10.5, 11.5, and 12.5 nm) and two n-gate/n-channel device (t_{ox} = 3.8 and 10.8 nm). One of these comparisons is given in Fig. 2(a)–(c). The split C–V technique is used. Both measured gate–channel C_{gc} and gate–bulk C_{gb} capacitances are corrected due to overlap and parasitic capacitances. Total capacitance is $C_g = C_{gc} + C_{gb}$. From max C_{gb} in the strong accumulation it follows $t_{ox} \le L' \times W \times \epsilon_{ox}/\max C_{gb}$, where W is the channel width, and L' is the effective channel length. We estimate t_{ox} = 9.8 nm. The QS gate capacitance is calculated by MINIMOS using the method.

$$C_g(U_{GS}) = \frac{\partial Q_g}{\partial U_{GS}} \approx \frac{\Delta Q_g}{\Delta U_{GS}} = \frac{Q_g\left(U_{GS} + \frac{\Delta U_{GS}}{2}\right) - Q_g\left(U_{GS} - \frac{\Delta U_{GS}}{2}\right)}{\Delta U_{GS}}. \quad (2)$$

Q_g is the total charge in the gate, obtained from the flux of the electric field through a contour in the oxide around the gate (Fig. 1). We used ΔU_{GS} = 25 mV, $|U_{DS}|$ = 1 mV and have frozen the grid. This simple technique is very accurate, as it has been proven by several comparisons with the analytical (exact) C_g [10]. For the comparison with experiment only the field flux from the source subdiffusion to the drain subdiffusion is included in Q_g. The channel doping profile is obtained by fitting the $C_g(U_{GS})$ from threshold to flat band (starting from a SUPREM profile). Note that the doping profile has a small

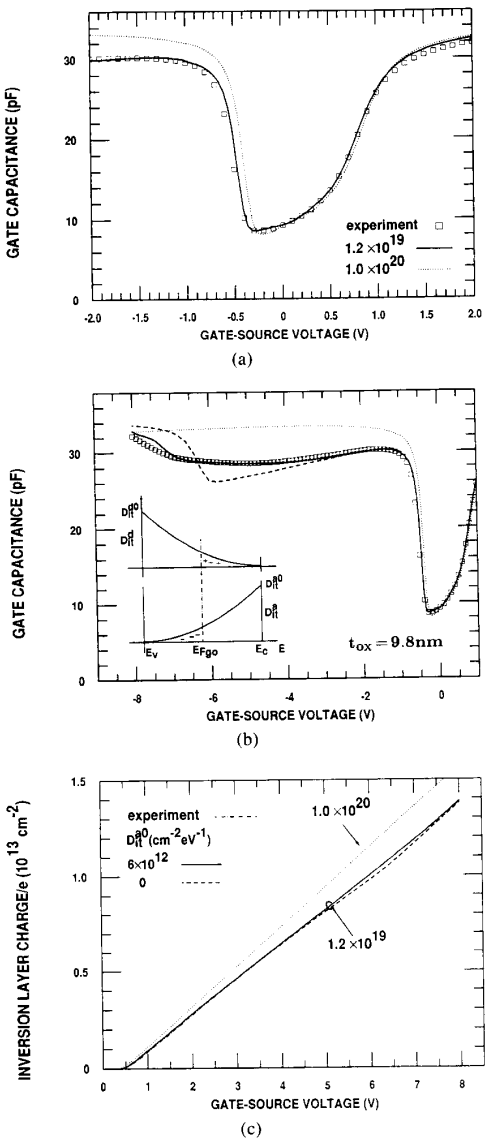

Fig. 2. Calculated QS gate capacitance against experiment. p-gate/p-channel device: L' = 99.3 μm, W = 100 μm, t_{ox} = 9.8 nm. N_g = 1.2 × 10^{19} cm^{-3} is assumed. T = 295 K. Dotted curve: heavy doped gate. Solid curve: $D_{it}^{a0} = 6 \times 10^{12}$ cm^{-2} eV^{-1}. Dashed curve: $D_{it}^{a} = 0$. For both curves: $D_{it}^{d} = 0$, $Q_{fGO} = 10^{12}$ cm^{-2} · e. (a) Region of small gate bias. There is a small discrepancy in the accumulation. (b) Inversion side of the C–V curve. Experiment shows a typical smooth inversion in the polygate, contrary to rigid-parabolic-band model: dashed curve. Assuming the acceptor-like interface traps with a simple parabolic density (inset) a good fit is possible; solid curve. (c) Inversion layer charge Q_i. Experimental Q_i is obtained by integration of the experimental gate-channel capacitance: dot-dashed curve. Numerical Q_i is calculated from the drain current as explained in the text. There is a negligible difference between the solid and the dot-dashed curve. With respect to (a) and (b) no additional fitting is performed.

[1]The relationship between the oxide field E_{ox} and the surface potential ϕ_s is

$$\int_0^{\phi_s} \rho(\phi)\, d\phi = -\epsilon_s(\epsilon_{ox}E_{ox}/\epsilon_s + Q_{it}/\epsilon_s)^2/2,$$

where ρ is the space charge and Q_{it} is the interface trapped charge. The semiconductor capacitance including interface traps is given by

$$C_s = \rho(\phi_s)/(\epsilon_{ox}E_{ox}/\epsilon_s + Q_{it}/\epsilon_s) + \partial Q_{it}/\partial\phi_s.$$

influence on the inversion side of the C–V characteristic far above threshold. N_g is estimated by matching simulated C_g with experiment at low gate bias.

Comparison of the simulations with measurements shows a disagreement between the rigid-parabolic-band model (1) (dashed curve in Fig. 2(b)) and the experiment on the inversion side. The slope of the calculated C–V curve is larger. In addition, the inversion in the polygate is smooth, while the calculation shows a fast recovery of the gate capacitance to the ϵ_{ox}/t_{ox} limit (for both MB and FD statistics). A simple engineering approach to remove this disagreement is to assume acceptor-like traps at the gate/oxide interface D_{it}^a (in the case of an n-gate, donor-like traps D_{it}^d would have to be assumed). We find that traps with a parabolic energy density (shown in Fig. 2(b))

$$D_{it}^a = D_{it}^{a0} \cdot \left(\frac{E - E_v}{E_c - E_v}\right)^2 \tag{3}$$

can reproduce well our experimental data. All considered p-gate/p-channel devices have been fabricated with the same process, except for the amount of final gate oxide grown. We were able to satisfactorily fit all C–V curves with the same values of N_g, Q_{fGO} (fixed charge at the gate/oxide interface), and D_{it}^{a0} (see Fig. 3). A small disagreement also exists at the accumulation side. The experimental data lie below the calculated curve (Figs. 2(a) and 4), although there is the agreement at the flat band and in the strong accumulation limit.

Comparison between the corresponding inversion layer charge density Q_i is given in Fig. 2(c). Experimental Q_i is calculated by integration of the experimental $C_{gc}(U_{GS})$ data and dividing the result by $L' \times W$. Simulated Q_i is calculated from the MINIMOS drain current using the relation $Q_i \approx L' I_D/(W\mu_s U_{DS})$ in the linear region. The dependence of μ_s on the normal field has been suppressed in the simulation. This has no influence on C_g and Q_i—the bulk is in quasi-equilibrium. The value of μ_s near the interface is known exactly, as this is an input to the simulation. No additional fitting has been performed. The agreement between the simulation and experiment is very good, even without assuming some interface traps (dashed curve). Note that the error in I_D is smaller than in Q_i in practice. Let us assume a positive error in Ψ at the gate/oxide interface. It produces a positive error in Q_i and E_{ys}. The surface mobility μ_s decreases because of the higher E_{ys} (at room temperature). The errors in Q_i and μ_s compensate partially each other, leading to a small error in the drain current $I_D = W\mu_s Q_i E_x$.

Measurements on n-gate/n-channel devices (Fig. 4), as well as the QS C–V data published in the literature: [5, fig. 5(a)], [7, fig. 1], [9, fig. 10], and [10, fig. 6] show similar deviations from the rigid-parabolic-band model. An inspection of the data shows that the observed deviations are reproducible, seem to be independent of the specific technological process and of the type of gate (n or p type, polysilicon or amorphous silicon). The disagreements are summarized below:

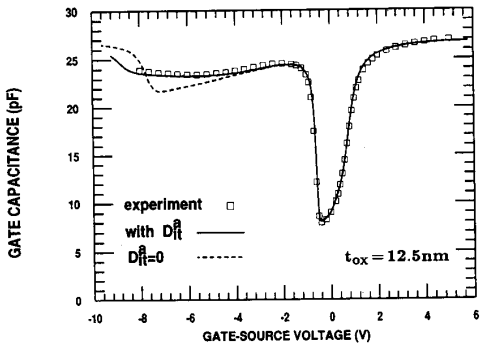

Fig. 3. Calculated QS gate capacitance against experiment. p-gate/p-channel device: t_{ox} = 12.5 nm. Other parameters are taken from Fig. 2 without additional fitting.

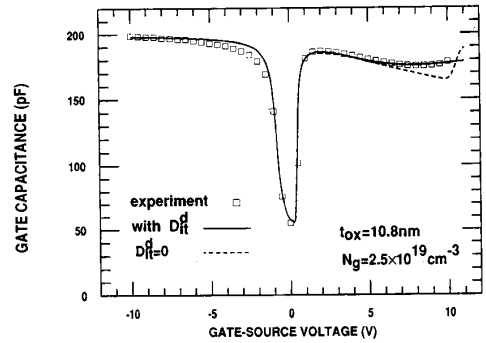

Fig. 4. Calculated QS gate capacitance against experiment. n-gate/n-channel device: $L' = 250\ \mu m$, $W = 250\ \mu m$, $t_{ox} = 10.8$ nm. $N_g = 2.5 \times 10^{19}$ cm^{-3}. $T = 295$ K. Solid curve: $D_{it}^{d0} = 10^{13}$ cm$^{-2} \cdot$ eV^{-1}. Dashed curve: $D_{it}^d = 0$. For both curves: $D_{it}^a = 0$, $Q_{fGO} = 5 \times 10^{11}$ cm$^{-2} \cdot$ e.

- Accumulation: the calculated C_g is higher than the experimental (while they agree at the flat band and in the ϵ_{ox}/t_{ox} limit).
- Gate depletion: experimental C_g is weakly dependent on U_{GS}, while the calculated decreases strongly with increasing U_{GS}.
- Gate inversion: contrary to experiment, which shows a smooth inversion, the calculation has a fast recovery to ϵ_{ox}/t_{ox}.

We propose several possible physical explanations for the above phenomena as follows:

1) *Quantum-effects in the strong accumulated layer* increase the surface potential and lower the semiconductor capacitance; e.g., for p-type low-doped silicon (2×10^{15} cm^{-3}) the effect becomes important at surface fields higher than ~ 150 kV/cm at room temperature [15]. The change of the semiconductor capacitance have a larger influence over the total capacitance when ϵ_{ox}/t_{ox} becomes comparable to the semiconductor capacitance—that means, at thin oxides. In the case of n(p)-gate/n(p)-channel devices, the semiconductor capacitance in the accumulation is lower in both gate and bulk leading to an enhanced deviation from the classical theory. This could be the expla-

nation for the very slow rise of C_g from depletion to heavy accumulation that is measured on the device with 3.8 nm oxide.

2) *Nonuniform dopant distribution* in the polygate: An increase of N_g from the gate/oxide interface into the gate can explain a low slope of the C_g versus U_{GS} curve, but cannot explain the smooth inversion in the poly-gate.

3) *Interface trapped charge* at gate/oxide interface with both donor and/or acceptor nature could reproduce a low slope of $C_g(U_{GS})$ curve, as demonstrated by Figs. 2(b), 3, and 4. With increase of N_g, however, it is necessary to assume a higher amount of traps to explain the experiment. In addition, we did not observe any significant change in the C–V curve the p-gate/p-channel devices by varying the signal from 1 kHz to 1 MHz QS. Therefore, if there are any traps at the gate/oxide interface, their repopulation must be very fast.[2]

4) *Deep band tails* occur in the heavy doped space-charge regions—a fact established both theoretically ([17]) and experimentally (very large δE_{c+v} [18]). When the polygate enters into weak depletion, the screening of ions becomes weak due to carrier-concentration-dependent screening length [19], and the lattice disorder increases. Many majority carriers remain localized in deep band states. Depletion is only partial, voltage drop in the gate increases, and the polygate capacitance becomes lower comparing to the parabolic-band model. The slope of $C_g(U_{GS})$ is reduced. At high U_{GS}, the minority carriers begin to fill the deep states in the corresponding, opposite tail leading to a smooth inversion (modeled by interface traps in Figs. 2(b), 3, 4). One approach to account for this effect could be the application of the well-known band-tail theory, [19]. Another view on the problem is the *point fluctuations of dopants*. Let us assume $N_g = 10^{19}$ cm^{-3}. It follows that $L_{Dg} = 1.3$ nm (Debye length) at 300 K. A parallelopiped with $10L_{Dg} \times 10L_{Dg}$ base and $5L_{Dg}$ height (comparable to the depth of the depletion region) contains only 11 atoms of dopant an average; namely, there are ~ 2 atoms in the first L_{Dg} from the gate/oxide interface. Any macroscopic approach to N_g and space-charge density is obviously no longer valid. Experiment and model calculation based on dopant fluctuations have shown that the stretch-out of the gate-channel capacitance of the MOS system has taken place already at a doping of 3×10^{18} cm^{-3} at room temperature [20] (see also [21]). By increasing the dopant concentration, the gate-channel capacitance becomes smoother. This can qualitatively explain [7, fig. 1] which shows a fast inversion in low doped gate and a smooth recovery for heavy doped one. We think the random distribution of dopants is an obvious explanation for the smooth inversion in the heavy doped gate.

[2]An additional conclusion is that the minority carriers in the gate can invert very quickly (see [16] also). This is opposite to the result for an n-gate/n-channel device given in [11, fig. 5], which shows evidently a finite time response for the minority carriers in the polygate. *Note added in proof:* The same result has recently been published by S.-W. Lee *et al.*, *IEEE Electron Device Lett.*, vol. 13, no. 1, pp. 2-4, 1992.

IV. Conclusion

For practical purposes the QS C–V characteristics of the implanted gate device can be well fitted assuming traps at the gate/oxide interface. This enables an accurate description of the integral quantities like inversion layer charge, oxide field, and drain current. There are additional physical phenomena in the polygate not included in the model. We think there is no reason to model polygate depletion, an essentially parasitic effect, assuming complex physical formulations. We would like to point out, however, that phenomenon 4) discussed in Section III may come into play in the bulk of future devices with scaled oxide and increased bulk doping. A more complete (both physical and engineering) description of the space-charge regions, including these phenomena, would be required to accurately model these devices.

Appendix

We have not accounted for the traps at grain boundaries. The validity of this approach depends on the equivalent volume trap density in the polysilicon near the gate/oxide interface $N_{t\text{vol}}$ (given by the quotient of the surface trap density at grain boundaries N_{tgb} and the average grain size l_g). If $N_g >> N_{t\text{vol}}$ holds, the charge trapped at the grain boundaries has a minor influence on the neutral Fermi level position and the average total space-charge density. Therefore, we can neglect it in a first approximation. Note that this is not case for the transport problem in polysilicon—small barriers at grain boundaries affect the current also if $N_g >> N_{t\text{vol}}$ holds. If N_g is comparable or less than $N_{t\text{vol}}$ the trap effect is dominant. A value $N_{tgb} \sim 2\text{–}3 \times 10^{12}$ cm^{-2} has been experimentally estimated for small-grain polysilicon in [22], [23, and references cited therein]. Assuming $l_g = 30$ nm it follows $N_{t\text{vol}} \sim 10^{18}$ cm^{-3}. For larger grain $N_{t\text{vol}}$ becomes smaller. If we restrict ourselves to a concentration $N_g \geq 4 \times 10^{18}$ cm^{-3} the error due to traps seems to be reasonably small. Note that the trap effect becomes important in lightly doped gates (like those in [16]).

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