

# Electrothermal Analysis of Latch-Up in an IGT

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## Abstract

An IGT combines bipolar conduction with MOS gate control of the current. Due to bipolar conductivity modulation arising from carrier injection, an IGT can be operated at high forward current densities, even when supporting high blocking voltages. Due to its MOS gate, the IGT can be driven with low power.

The concept of the IGT is to use a MOS gate created channel to link the  $n^+$ -emitter region and the  $n^-$ -base [1]. In the on-state, the lower junction towards the collector is forward-biased and the current flow in the IGT occurs via the channel. When latch-up occurs, however, the parasitic thyristor between the collector and emitter terminals in the four-layer IGT structure turns on, and the control of the collector current by the applied gate voltage is lost. In DC circuits, latch-up usually produces catastrophic failure of the device as a result of excessive heat dissipation.

The simulation of the electrothermal nature of latch-up requires a mathematical model of the coupled transport of heat and charge carriers.

$$\text{div grad } \psi = \frac{q}{e} (n - p - C) \quad (1)$$

$$-q \cdot \frac{\partial n}{\partial t} + \text{div } q \cdot \mu_n \cdot n \left( \vec{E} - \frac{kT}{q} \text{grad} (\ln n_{ie}) + \frac{kT}{q} \frac{1}{n} \text{grad } n + P_n^{eff} \text{grad } T \right) = q \cdot R \quad (2)$$

$$q \cdot \frac{\partial p}{\partial t} + \text{div } q \cdot \mu_p \cdot p \left( \vec{E} + \frac{kT}{q} \text{grad} (\ln n_{ie}) - \frac{kT}{q} \frac{1}{p} \text{grad } p - P_p^{eff} \text{grad } T \right) = -q \cdot R \quad (3)$$

$$C \cdot \frac{\partial T}{\partial t} + \text{div} (-\kappa \text{grad } T) = \frac{J_n^2}{\sigma_n} + \frac{J_p^2}{\sigma_p} + q \cdot R \left( 2 \cdot T \cdot \frac{kT}{q} \frac{1}{n_{ie}} \frac{\partial n_{ie}}{\partial T} \right) +$$

$$\vec{J}_n T \text{grad } P_n - \vec{J}_p T \text{grad } P_p + T P_n^{eff} \text{div } \vec{J}_n - T P_p^{eff} \text{div } \vec{J}_p \quad (4)$$

$$\left( \frac{k}{q} \ln \frac{c}{n_{ie}} - \frac{kT}{q} \frac{1}{n_{ie}} \frac{\partial n_{ie}}{\partial T} \right) + P_c \equiv P_c^{eff} \quad (5)$$

$$\frac{\partial n_{ie}}{\partial T} = n_{ie} \left( \frac{E_g}{2kT^2} + \frac{3}{2T} - \frac{q \cdot V_1 \cdot \left( \ln \left( \frac{N_D^+ + N_A^-}{N_0} \right) + \sqrt{\ln^2 \left( \frac{N_D^+ + N_A^-}{N_0} \right) + \frac{1}{2}} \right)}{2kT^2} - \frac{\frac{\partial E_g}{\partial T}}{2kT} + \frac{3 \frac{\partial \left( \frac{m_n^* m_p^*}{m_0^2} \right)}{\partial T}}{4 \left( \frac{m_n^* m_p^*}{m_0^2} \right)^2} \right) \quad (6)$$

The governing equations (1-6) are based on irreversible thermodynamics [2], [3], [4]. They are valid in both the stationary and transient regimes. Four contributions to the heat generation can be distinguished: Joule heat, recombination heat, Thomson heat and carrier source heat. Bandgap-narrowing effects are accounted for, as well as the dependence of the bandgap and the effective masses on temperature. The dependence of the Fermi level on the lattice temperature is made apparent in equation (5). Equations (4)-(6) imply Thomson's laws.

Mixed boundary conditions for the heat flow equation are mandatory in order to be able to model realistic imperfect cooling conditions. This is of special importance for transient electrothermal simulations, as the time constant for self-heating increases with increasing external thermal resistance.

Static latch-up has been investigated in an IGT. It occurs when the forward conduction current density exceeds a critical value, while the collector voltage is low. Geometry and doping data were taken from [1]. The heat sink thermal conductance is  $50 \text{ W/cm}^2 \text{ K}$ .

With  $V_g = 15 \text{ V}$ ,  $V_c = 1.5 \text{ V}$  the IGT is still in the save operating area. Figs. 1, 2 show the carrier concentration in the  $n^+$ -emitter, the channel region and the  $p$ -base.

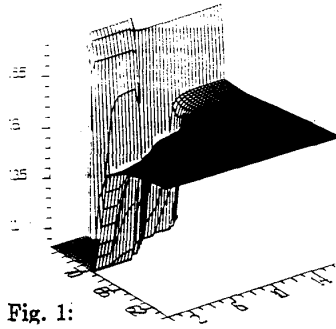


Fig. 1:

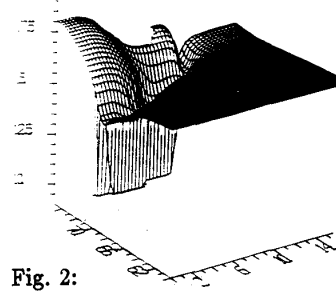


Fig. 2:

The current handling capability of the IGT is limited by the onset of latch-up. In order to find the critical value of the collector current  $I_c$ , the collector voltage  $V_c$  is ramped in a transient electrothermal simulation.

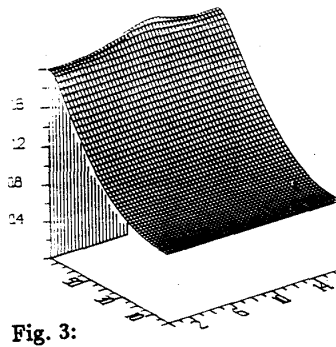


Fig. 3:

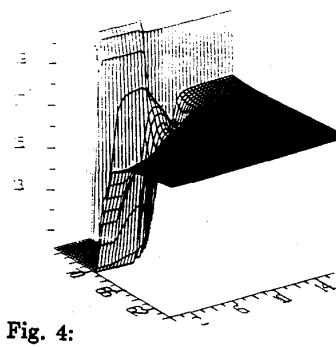


Fig. 4:

Fig. 3 shows the increase of the temperature in the channel region after onset of latch up. The maximum temperature is found to be in the inversion layer. Fig. 4 is a snapshot of the electron concentration after onset of latch-up. It is shown that the emitter injects electrons into the  $p$ -well. In silicon, the critical value is exceeded when the  $n^+$ -emitter- $p$ -base junction becomes forward-biased by more than 0.7 volt, usually because of lateral current flow in the  $p$ -base.

It is found that the latching current is reduced with increasing temperature. The reason is that the gain of the  $pnp$ -transistor as well as the sheet resistance of the  $p$ -base increases with temperature. Thus the latching current reduction is a function of cooling conditions.

## References

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