

**INVESTIGATION OF CHANNELING IN FIELD OXIDE CORNERS BY  
THREE-DIMENSIONAL MONTE CARLO SIMULATION OF  
ION IMPLANTATION**

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**ABSTRACT**

The effects of channeling of source/drain (S/D) implants in field oxide corners are investigated by three-dimensional Monte Carlo simulation of ion implantation. The simulations were carried out for conventional LOCOS and for poly-buffered LOCOS, assuming idealized field oxide geometries. The results of amorphous mode and crystalline mode simulations were compared. For poly-buffered LOCOS we found that due to channeling the bend radius of the isometric surfaces of the dopant concentration is significantly decreased in the field oxide corner even when using a  $7^\circ$  tilt angle for dechanneling. This may result in a reduced breakdown voltage of S/D-to-well diodes.

**INTRODUCTION**

The S/D doping in minimum-size transistor designs is an intrinsically three-dimensional problem. Furthermore, in modern shallow-junction processing channeling may affect the device performance. To verify these effects a rigorous three-dimensional Monte Carlo simulation [1], [2] with advanced physical models for crystalline targets [3] is necessary. To keep the computational effort within acceptable limits we used the new *trajectory split* method [4] for the crystalline mode.

**THREE-DIMENSIONAL MONTE CARLO SIMULATION OF ION IMPLANTATION**

For the simulations we used a phosphorus implant of  $5 \cdot 10^{13} \text{cm}^{-2}$  at 40keV. Fig. 1 and Fig. 2 show the geometries of the conventional and the poly-buffered LOCOS, respectively. In both cases the screening oxide thickness is 10nm and the ion beam was tilted for  $-7^\circ$  in the xy-plane. Fig. 3 and Fig. 5 show the amorphous and crystalline mode simulation results for the conventional LOCOS. From these results follows that in the active region the dopant concentration near the silicon surface is significantly decreased whereas the doping at the periphery (along the bird's beak) remains unaffected due to the dechanneling property of the thicker oxide in that region ( $\approx 60\text{nm}$ ). In contrast, the isometric lines in Fig. 6 show a much sharper bend compared to the results in Fig. 4. This may cause rotation dependent breakdown voltages if the wafer is not properly rotated during implantation.

**CONCLUSION**

Channeling effects in field oxide corners influence the properties of S/D-to-well diodes as well as the dopant concentration near the

interface between silicon and silicondioxide even when the ion beam is tilted for dechanneling. Based on these results further three-dimensional process and device simulations can be carried out for a complete characterization of these phenomena.

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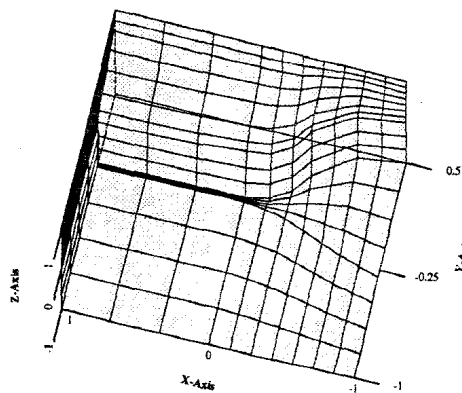


Figure 1: Field oxide corner of a conventional LOCOS

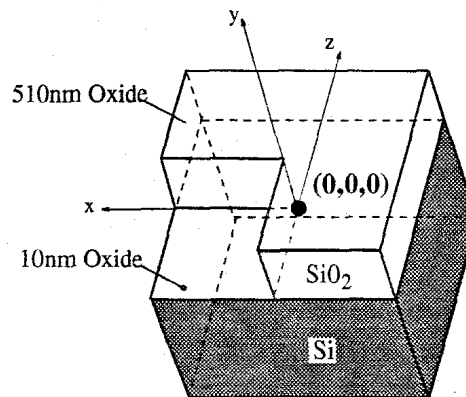


Figure 2: Field oxide corner of a poly-buffered LOCOS

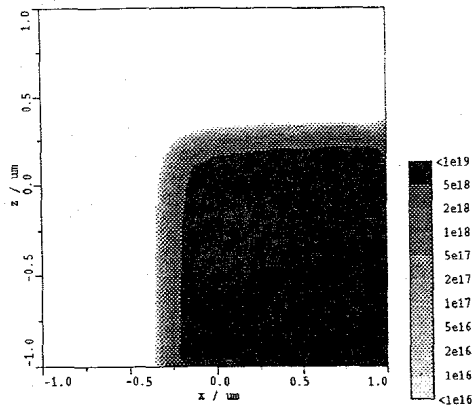


Figure 3: Concentration of phosphorus in  $\text{cm}^{-3}$  10nm below the silicon surface (conventional LOCOS geometry is cut by a horizontal xz-plane, amorphous mode)

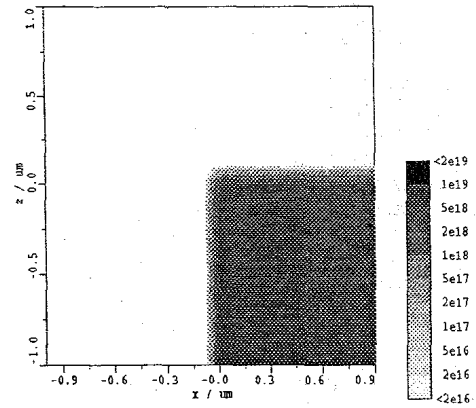


Figure 4: Concentration of phosphorus in  $\text{cm}^{-3}$  40nm below the silicon surface (polybuffered LOCOS geometry is cut by a horizontal xz-plane, amorphous mode)

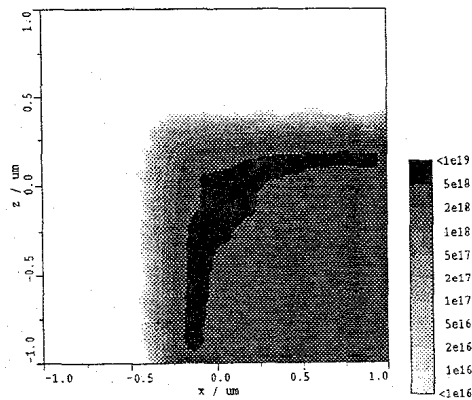


Figure 5: Concentration of phosphorus in  $\text{cm}^{-3}$  10nm below the silicon surface (conventional LOCOS geometry is cut by a horizontal xz-plane, crystalline mode)

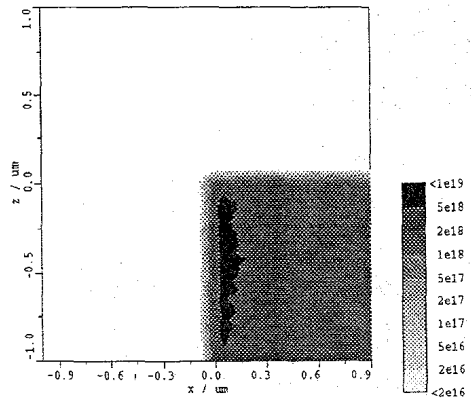


Figure 6: Concentration of phosphorus in  $\text{cm}^{-3}$  40nm below the silicon surface (polybuffered LOCOS geometry is cut by a horizontal xz-plane, crystalline mode)