LAYOUT DATA IN TCAD FRAMEWORKS

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ABSTRACT

Today Technology CAD (TCAD) tools are essential to the development of modern Integrated Circuit (IC) fabrication processes. They are as well, required in the design/optimization of very detailed and critical circuits related to a given IC process, where the usual higher level tools in Electronic Design CAD (ECAD) frameworks do not exhibit the precision or the features required. The boundary between TCAD and ECAD is not well established, and the interfacing between the two must be handled. This paper describes how ECAD and TCAD are linked inside the Viennese Integrated System for Technology CAD Applications (VISTA).

1 INTRODUCTION

Enormous progress has been seen in the design automation of very large integrated circuits, namely at the automatic synthesis and design verification levels. Most of this effort regarded digital integrated circuits, and very efficient tools to check the functional correctness of these designs were developed [Pomeranz and Reddy 1993].

As the last generations of integrated circuits include also analog sections (e.g. analog/digital converters), or very high performance circuits (e.g. ultra high clock speeds) which must be simulated at a detailed level, ECAD frameworks need new capabilities to enable a correct analysis/optimization and verification of designs.

Although TCAD frameworks are not intended to be used in the design of a complete integrated circuit, they include some features and tools that can be very useful, covering some lacks encountered in classical ECAD frameworks. In this paper we report on the concepts how these features are incorporated in VISTA [S. Halama et al.1995] to achieve these objectives, and we give some examples.

2 LAYOUT IN VISTA FRAMEWORK

As the final result of any ECAD framework is layout data, representing the mask artwork of the structures to be fabricated (or simulated), it is obvious that this information must be supplied to the TCAD framework. But in generality of such frameworks the tools used to display, print and interactively manipulate geometrical data, are a-priori not suitable to handle layout data. They were developed mainly to edit device geometries (vertical design) where there are no polygons overlapping. In addition instead of layer names, material types are defined.

In VISTA data is stored in the Profile Interchange Format (PIF) [F. Fasching et al.1994]. To the PIF EDitor [Rieger 1995] tool, that suffered from the above drawbacks, we added some functionality creating a special mode for layout editing. However, in most of the cases the better way is to use converters from CIF or GDS-II [Rubin 1987] layout representations to PIF. The PIF EDitor is used only for the visualization and manipulation

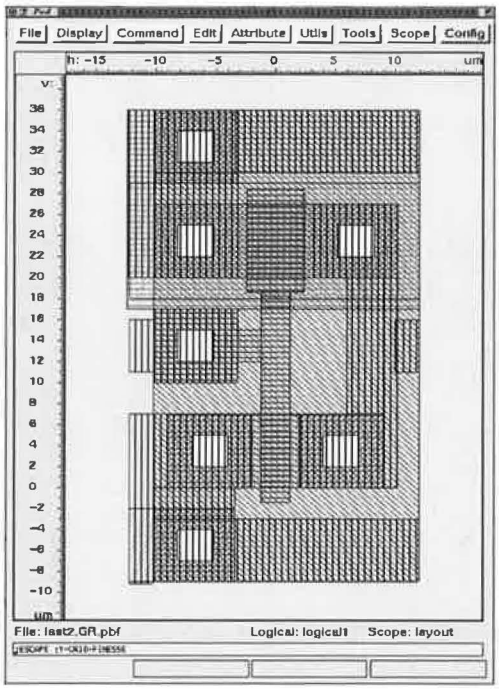

Figure 1: Displaying an imported piece of layout: A CMOS inverter.

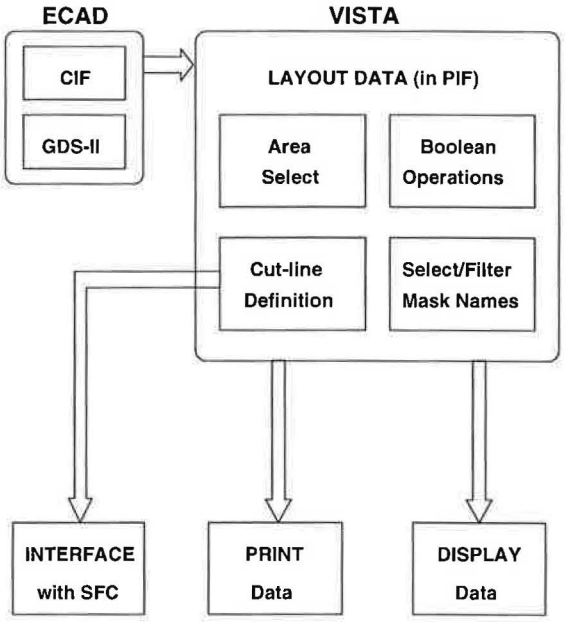

Figure 2: Layout data in VISTA - Block diagram.

of this data. As the cited formats are extensively used, the interface with any ECAD framework is assured. In Figure 1. we present an inverter layout imported from the CADENCE DWF-II framework.

In general, the simulators inside TCAD frameworks can not handle large pieces of layout. Therefore a tool to interactively select areas of interest from large layouts was created. In addition tools to perform boolean operations with masks and to filter/select given mask names were developed. An overview diagram is shown in Figure 2.

Since most process and device simulators are designed for two-dimensional applications, there is the need to interactively specify the locations where in the layout, a cut is to be performed. That means the end points of the cut-line, as shown in Figure 3. have to be given. The tool designed for this task can also warn the user of some problems associated with this operation.

An interesting feature is that the result of the cut-line tool is understood by the VISTA Simulation Flow Controller(SFC) [Pichler 1993] so the process simulation (and consequent device simulation) can be carried without the user have to explicitly define etches using the absolute coordinates. The interface relies in a LISP-like syntax format, to make it easily compatible with the SFC code, that it is implemented in LISP. In this way it is also very flexible and easy to extend with new features, as required by the integration of the various process and device simulators. Anyhow, in PIF the layout data is stored in such a way, that these simulators can use it as stand-alone applications directly without having to perform any further operations.

Another feature is the capability to understand mask names. The mask names in the CIF file, or in the technology file accompanying the GDS-II files change between different technologies (eg. the metal1 layer can be "METAL1" or sometimes "METAL_1"). So some intelligence was added in such a way that the user can select the desired layer without knowing exactly its name, which of course works only with the usual layers in IC technologies.

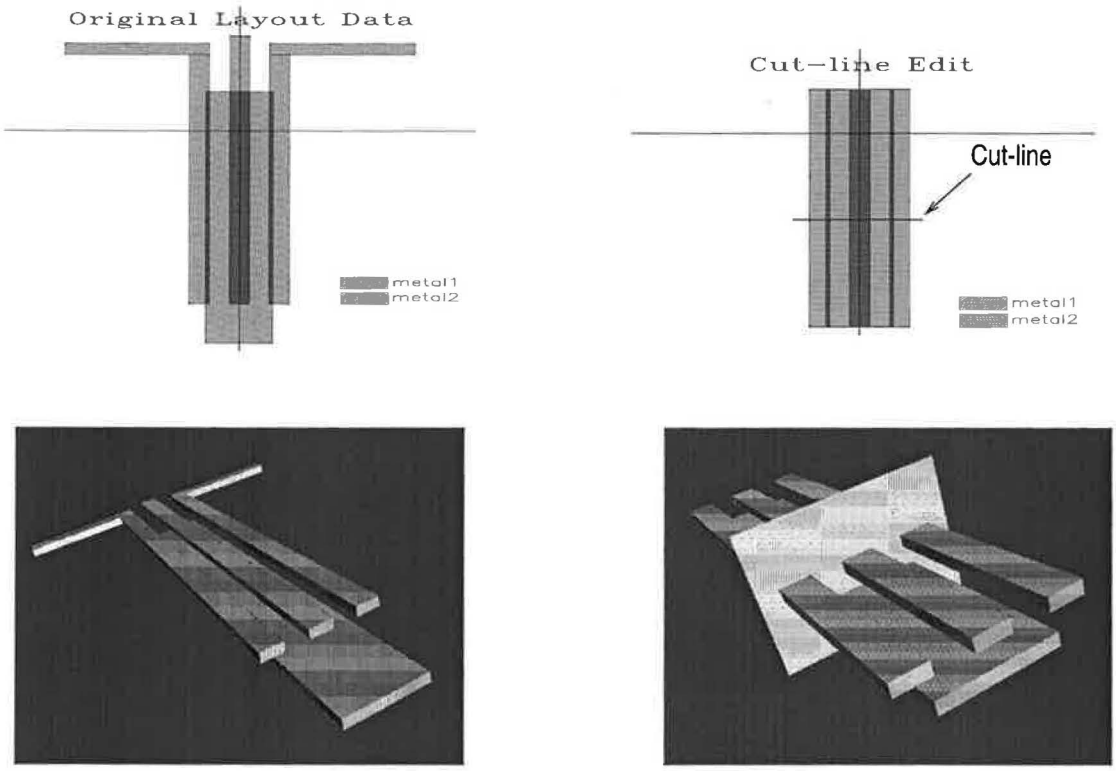

Figure 3: Handling layout to perform a capacitance extraction.

3 EXAMPLES

In this section we present some examples how the layout data can be used in TCAD. These are representative examples of typical simulation cases found in critical integrated circuit design.

Figure 3. shows an example of how VISTA can be used to extract accurate interconnect wire capacitances. The layout was imported from a commercial IC design framework that could not calculate the capacitances between the conductors in METAL2. First, a piece of layout (where one dimension is not changing) was selected and then, a cut performed. The result is then fed to the capacitance extractor simulator SCAP [M. Mukai 1995]. Although SCAP has three-dimensional capabilities, in this example they are not used.

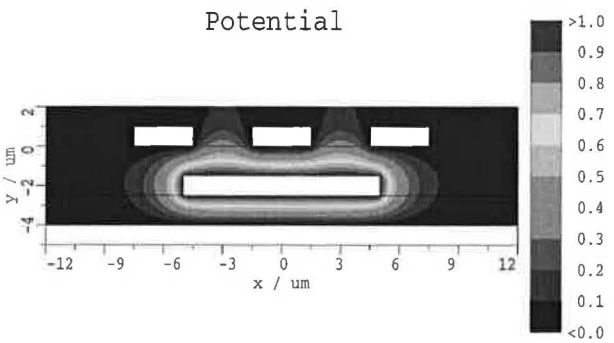

Figure 4: Cut showing potential distribution in wires.

The result of the cut and the potential distribution in the wires are displayed in Figure 4. It is to remark that a ground plane (the substrate) is always assumed to exist and the material surrounding the wires is SiO_2. In the simulation, the METAL1 conductor is at 1V potential and all the other conductors (substrate included) at a null potential. In this situation the calculated capacitances are as in Table 1.

CAPACITOR	VALUE (F/m)		CAPACITOR	VALUE (F/m)
$C_{1,2}$	1.814e-11		$C_{1,3}$	7.189e-15
$C_{1,4}$	6.138e-11		$C_{1,5}$	3.361e-11
$C_{2,3}$	1.814e-11		$C_{2,4}$	1.181e-10
$C_{2,5}$	8.892e-14		$C_{3,4}$	6.137e-11
$C_{3,5}$	3.361e-11		$C_{4,5}$	2.845e-10

1 ¨3 - METAL2 4 - METAL1 5 - SUBSTRATE

Table 1: The simulated capacitance values.

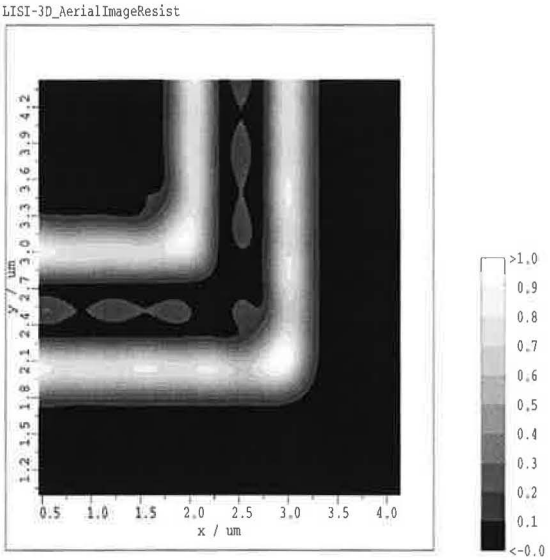

Figure 6: Lithography simulations.

In Figure 5. and Figure 6. the results obtained from a three-dimensional simulator are shown. In this example the aerial image has been generated from a module of a lithography simulator, where the masks are used directly as input. In the first image, the problems of the elbows are due to mask deficiencies and in the second, they result from a large defocus. The parameters used in the simulations are in Table 2.

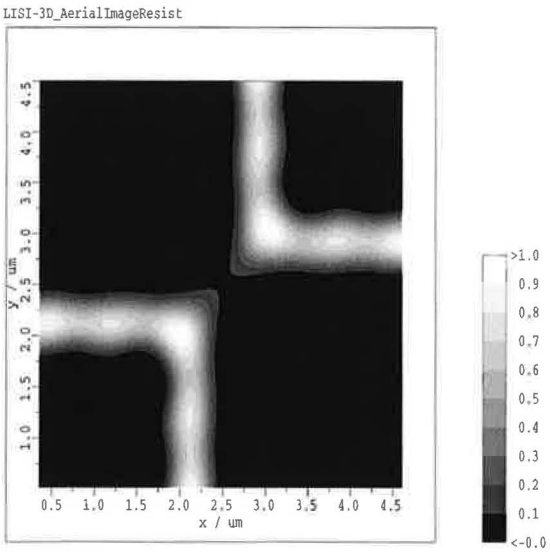

Figure 5: Lithography simulations.

	Figure 5.	Figure 6.
Wavelength - λ	365nm	248nm
defocus	0	700nm
Num. Aperture - NA	0.48	0.38

Table 2: simulation parameters

For very special technologies and modes of device operation (e.g. moderate inversion operation of a MOSFET transistor) the SPICE like models included in ECAD frameworks are not enough precise, or sometimes inexistent. In this case a device simulator like MINIMOS [S. Selberherr 1987] may be necessary. Figure 7. shows the transient response of an inverter (see Figure 1.) designed in an ultra low voltage technology (0.5V). The result was obtained using first the SFC (as explained before) which integrates MINIMOS to get a device model (for each transistor) and then MINISIM [Stach 1995], a charge based circuit simulator.

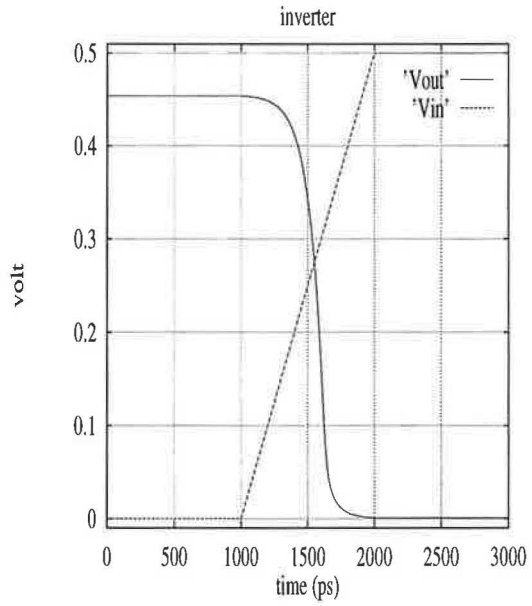

Figure 7: Simulation of the transient response of an inverter.

4 CONCLUSION

The TCAD frameworks can be extended with features, that allows them to understand and manipulate layout data. In this way, they can be used in the design and optimization of integrated circuits, providing an excellent help to cover some missing, or not so sophisticated tools in ECAD environments.

ACKNOWLEDGMENT

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BIOGRAPHY

R. Martins was born in Porto, Portugal, in 1968. He studied electronic and telecommunications engineering at the University of Aveiro - Portugal, where he received the degree of 'Licenciado' in 1991 and M.Sc. in 1994. In 1993 he joined INESC (Institute for Systems and Computers) where he worked on biomedical instrumentation. He joined the 'Institut für Mikroelektronik' in October 1994. He is currently working towards his doctoral degree. His scientific interests include very low power analog and digital integrated circuit design, digital signal processing and TCAD framework aspects.