

Analysis of Leakage Currents in Smart Power Devices

M. Knaipp^a, T. Simlinger^a, W. Kanert^b, S. Selberherr^a

^aInstitute for Microelectronics, TU Vienna,
Gusshausstrasse 27-29, A-1040 Vienna, Austria

^bSiemens AG, Semiconductor Group,
Otto-Hahn-Ring 6, 81730 Munich, Germany

Abstract

The Smart Power Device under consideration is a buried layer device which is widely used in industry. An n-doped epitaxy layer is grown on a highly n-doped buried layer. This layer is placed on the p-substrate. The epitaxy- and buried layers are surrounded by a double diffused p-isolation. The leakage currents between the epitaxy layer and the isolation are simulated and measured in a temperature range from 300 K to 500 K.

1. Introduction

In recent years, the smart power technology (SPT) has become an important part in semiconductor manufacturing. Self-heating effects and high environment temperatures play a significant role in the design of power devices. Technical specifications guarantee safe operation areas far exceeding 400 K. At high temperatures leakage currents can often lead to unexpected device behavior. On the other hand SPT devices are frequently used in the automotive industry, where strict safety requirements are given. At these high temperatures accurate leakage simulations are rare. We have investigated leakage currents of SPT devices in a temperature range from 300 K to 500 K by two-dimensional simulations using MINIMOS-NT [2].

2. Description of the simulated structure

Integrated Smart Power Technologies have a highly doped buried layer as a common drain for the DMOS transistors. The technology under consideration has a double diffused p-isolation. The lower part of this isolation is implanted before deposition of the epitaxy layer. The structure used for simulation is schematically shown in Fig. 1.

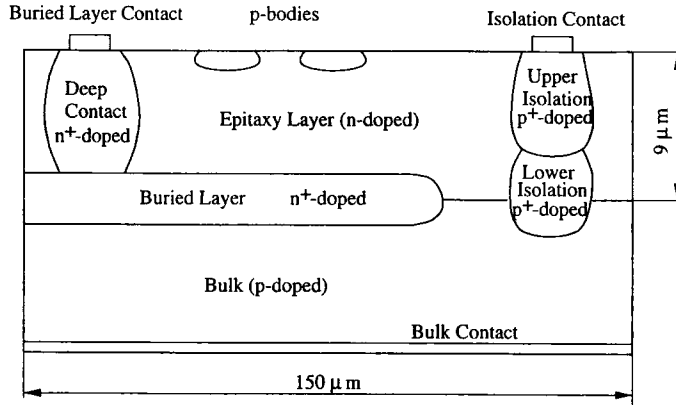


Figure 1: Simulated SPT Structure

The simulation domain was restricted to the fringe of the buried layer and was chosen to be $150\mu\text{m}$ wide. As the lateral distance between the buried layer and the lower isolation implantation is only $20\mu\text{m}$, which is small compared to the width of the buried layer, edge effects can be neglected. The p-bodies were not connected during the measurement. Their location in the epitaxy layer lies outside the p-n junction and so they can be ignored. The simulation conditions were chosen in accordance with those of the measurement, i.e. the voltage applied to the buried layer covered a range of $0 - 90\text{ V}$. Isolation- and bulk contact were on ground level.

3. Generation of the device simulator input file

The doping profile has been obtained by two-dimensional process simulation. SIMS profiles have been used to tune the various model parameters in order to obtain agreement between the simulated and measured doping profile. The maximum n- and p-doped regions lie near the aluminum contact of the buried layer and the isolation contact, respectively. The contact n-doping decreases towards the buried layer. In the buried layer region the doping increases again until it reaches a maximum value at $N_D^+ = 1.35 \cdot 10^{19}\text{ cm}^{-3}$. The maximum acceptor doping in the upper- and lower isolation is in a range of $N_A^- = 3.5 \cdot 10^{17}\text{ cm}^{-3}$ and $N_A^- = 1.5 \cdot 10^{17}\text{ cm}^{-3}$.

4. Description of the used temperature models

All material specific parameters have been modeled according to the required lattice temperature range of $300\text{ K} - 500\text{ K}$. This concerns the band edge energies, the effective densities of states and the carrier effective masses of electrons and holes. Standard MINIMOS mobility models have been used

to describe the device characteristics at high temperatures. The level of the leakage current is mostly influenced by the generation of carriers in the space charge region between the buried layer and the isolation. This generation has been described using a temperature dependent SHOCKLEY-READ-HALL model. The generation rate reads:

$$R = \frac{np - n_i^2}{\tau_p(n + n_1) + \tau_n(p + p_1)}.$$

The auxiliary values n_1 and p_1 are defined as:

$$n_1 = N_c(T) \cdot e^{-\frac{E_c + E_t}{kT}}; \quad p_1 = N_v(T) \cdot e^{-\frac{E_t + E_v}{kT}}.$$

The effective densities of states for electrons $N_c(T)$ and holes $N_v(T)$ have been calculated using the standard power law. We have assumed that the trap energy level is at the middle of the gap. The temperature dependence of the lifetimes is modeled after [1]. The lifetimes τ_n^o and τ_p^o were calculated with:

$$\tau_{n,p}^o = \frac{1}{c_{n,p}^o \cdot N_t}; \quad \tau_{n,p}(T) = \tau_{n,p}^o \cdot \left(\frac{300}{T}\right)^{1.5}$$

The concentration of deep traps N_t was used as a fitting parameter to obtain good agreement between measurement and simulation. With the mean lifetimes of $\tau_{n,p}^o = 2.5 \cdot 10^{-5}$ s and the capture rates $c_{n,p}^o = 6 \cdot 10^{-9}$ cm³/s, the concentration of recombination centers has been calculated. Best agreement with measured currents is obtained with a recombination trap density of $N_t = 6 \cdot 10^{12}$ cm⁻³. Fig.2 shows the simulated currents compared to the measured data. In Fig.3 the temperature dependence of the simulated currents is given. The voltage dependence on the currents decreases with higher temperatures. The maximum electric field appears near the upper isolation-epitaxy layer junction. Its value is about $\vec{E}_{max} = 2.5 \cdot 10^5$ V/cm at 300 K. The field decreases slightly with higher temperatures. In the high depletion area the maximum generation rate is about $G_{n,p} = 2.1 \cdot 10^{15}$ s⁻¹cm⁻³ at 300 K. The rate increases up to $G_{n,p} = 1.32 \cdot 10^{20}$ s⁻¹cm⁻³ for temperatures of 500 K.

ACKNOWLEDGMENT:

The authors would like to thank Dr. Soppa (Fachhochschule Osnabrück) for providing the measured data. This work was supported by SIEMENS, EZM Villach, Austria.

References

- [1] A. Schenk. A model for the field and temperature dependence of SHOCKLEY-READ-HALL lifetimes in silicon. *Solid-State Electron.*, 35(11):1585–1596, 1992.
- [2] T. Simlinger, H. Kosina, M. Rottinger, and S. Selberherr. MINIMOS-NT: A generic simulator for complex semiconductor devices. In H.C. de Graaff and H. van Kranenburg, editors, *ESSDERC'95 - 25th European Solid State Device Research Conference*, pages 83–86, Gif-sur-Yvette Cedex, France, 1995. Editions Frontieres.

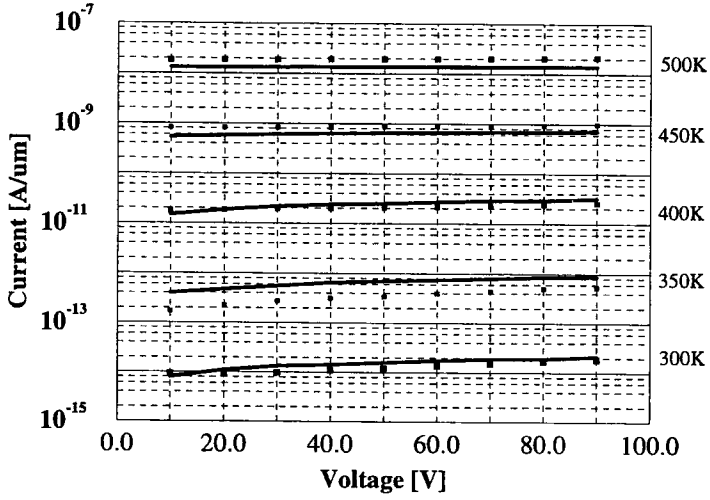


Figure 2: Simulated (full lines) and measured leakage currents (squares)

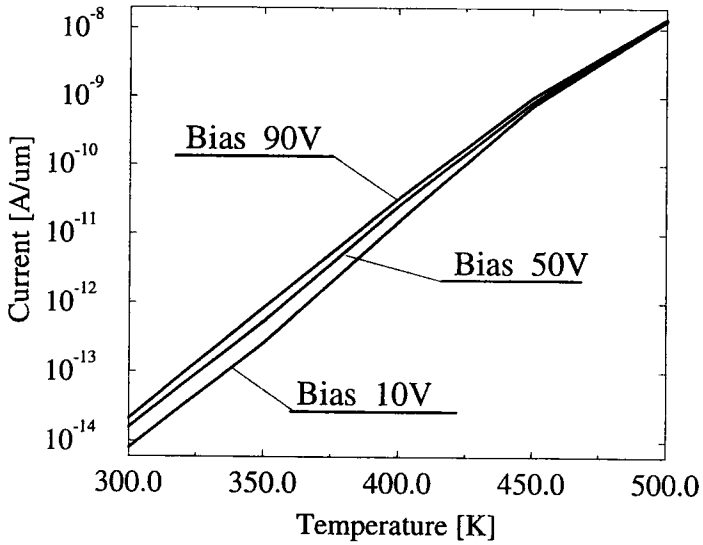


Figure 3: Simulated currents versus temperature