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A Physically Based Substrate Current Simulation

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***Abstract*—The substrate currents of submicron n-channel MOSFETs resulting from Drift-Diffusion (DD) and Hydrodynamic (HD) simulations are compared. The investigated devices are submicron LDD n-channel MOSFETs with pocket implants and gate lengths of 0.4, 1.0 μm. The current density distribution in the area of maximal generation is investigated. The influence of a surface reduced impact generation rate model is discussed. Finally, a generation rate which is proportional to the carrier concentration is calculated. This is in contrast to most used models were the generation rate is proportional to the particle flux density. To include nonlocal effects the carrier temperatures are used to calculate the generation rates instead of the local electric field.**

Introduction

In recent years MOSFET feature sizes have been continuously scaled down into the submicron range. This size reduction causes an increase of the maximum field strength inside the device and thus, an increase of the substrate current. The amount of substrate current is an important indicator for the aging behavior of the device [4]. Small substrate currents can be attained by a careful design of the device doping. To calculate the substrate current it is necessary to use an accurate, physical motivated impact ionization model. The standard Drift-Diffusion model (DD) can only use a field-dependent impact ionization model since no carrier temperatures are available [5]. However, the electric field dependence is inaccurate especially in small devices. Nonlocal effects must be taken into account when the typical thickness of space charge regions becomes comparable with the carrier energy relaxation lengths. To include nonlocality the impact generation rate must be calculated using the local carrier temperatures instead of the local electric field. The local carrier temperatures are obtained from Monte Carlo or Hydrodynamic (HD) simulations.

With the carrier temperature an equivalent electric field can be computed using results from Monte Carlo calculations for the homogeneous electric field versus temperature characteristic [7]. Finally, the equivalent electric field is used instead of the local electric field to calculate the carrier generation rates. This is often done in combination with a conventional DD model to achieve a better convergence compared to a fully HD simulation [6].

The Investigated Devices

The investigated devices are LDD-Pocket N-channel MOSFET test structures ($L_g = 0.4\,\mu\mathrm{m}, 1.0\,\mu\mathrm{m}$) for which detailed substrate current measurements were performed. During the measurements the substrate and source contacts were grounded. The doping profiles were generated by two-dimensional process simulation and have been verified by comparison of the measured and simulated device characteristics. A channel adjust implant is used to fix the threshold voltage. To prevent punch through a pocket implant is used near the source and drain doping. The maximum of the LDD doping is about 0.024μm below the semiconductor-spacer interface. The spacer width is 0.06μm for both channel lengths.

Results and Discussion

At low gate voltages the substrate current increase until a maximum value is reached. In this region the drain current increases faster than the electron temperature decreases which leads to a rise of the substrate current. When the gate voltage is near the drain voltage the carrier temperature decreases faster compared to the rise in drain current which finally leads to a reduction in the substrate current.

An additional effect takes place when an impact ionization model is used which accounts for a reduction of the surface generation rate [2][6]. At low gate voltages the pinch-off point is located closer to the source side. After the pinch off point the current is pushed towards the LDD-doping region which leads to a maximum current density near this LDD-doping rather than beneath the surface.

In [2] and [6] the surface generation rate is smaller compared to the bulk generation rate. In these publications a surface distance-dependent function determines the final generation rate for electrons and holes near the surface. Using this model an additional decrease of substrate current for higher gate voltage can be seen which can be attributed to a shift of the current density away from the region where the ionization coefficients have their maximum value.

The influence of a surface impact ionization model can be estimated when we look at the current density of vertical section through the maximum generation point. Fig. 1 and Fig. 2 show that there is a sharp local maximum of the current density in the DD model. In the HD model the current density is much smoother. At low gate biases (Fig. 1) the maximum current density is in the LDD-doping region rather than beneath the surface. Using high gate biases (Fig. 2) the maximum current density moves towards the surface. When we compare the two figures, it can be seen that the shift of the relative current density is much higher in the DD model than in the HD model. The broadening of the current density in the HD model is caused by the high diffusion of the carriers after reaching the pinch-off point. This effect can be explained when the partial driving forces of the DD model (Eq. 1) are compared with the partial driving forces of the HD model (Eq. 2). The driving force for electrons with a concentration n reads in the DD model (analogous for holes):

$$\vec{F}_{DD} = -\mathrm{grad}\ \psi + \frac{k_B \cdot T_0}{q} \cdot \frac{1}{n} \mathrm{grad}\ n \tag{1}$$

Note, that the prefactor to the concentration gradient depends on the lattice temperature T_0 which is usually set constant. In homogeneous materials the HD model uses a driving force which depends on an additional carrier temperature gradient.

$$\vec{F}_{HD} = -\mathrm{grad}\ \psi + \frac{k_B \cdot T_n}{q} \cdot \frac{1}{n} \mathrm{grad} n + \frac{k_B}{q} \cdot \mathrm{grad}\ T_n \tag{2}$$

The prefactor to the concentration gradient in the HD model now depends on the electron temperature T_n. Comparing the two prefactors of the concentration gradients, it can be seen that the factor in the HD model can be much larger especially in the high temperature range. The influence of the grad T_n term in the HD model is small compared with the grad n term. The reason for this is the small vertical gradient of the electron temperature in the region of interest.

Therefore, when the generation rate is calculated, the influence of the surface reduction in the HD model is much smaller compared to the conventional DD model.

A recent publication [1] also shows that the reduction of the surface generation rate is much smaller than published in earlier works. This agrees well with the shown HD simulations (Fig. 1, Fig. 2).

Because of the above mentioned reasons we have calculated the substrate current using a Hydrodynamic bulk ionization model even in the channel region. The model is based on the work of [3]. The advantage of this model is that the calculated generation rate is proportional to the carrier concentration and not to the particle flux density. This is physically motivated because the saturation velocity is much smaller compared to the thermal velocity. The model is implemented in a self-consistent manner, i.e., the energy flux equations account for carrier cooling.

The used equation for the electron generation rate depending on the concentration n reads:

$$G_n(n, T_n) = n\, A\, \exp(B\, u) \times$$
$$\left[\left(1 + \frac{1}{2}u\right) \mathrm{erfc}\left(\frac{1}{\sqrt{u}}\right) - \frac{1}{2}\sqrt{u}\exp\left(\frac{-1}{u}\right)\right] \tag{3}$$

$$u = u(T_n) = \frac{k_B T_n}{E_{th}} \qquad B = \frac{C\, k_B T_0}{E_{th}} \tag{4}$$

The electron temperature strongly depends on the used energy relaxation time which is assumed to be $\tau_n = 0.4$ps. The parameters A and C have to be calibrated to give best agreement with the measurements. The best correspondence with the measurement is found with $\mathrm{A} = 4.53 \cdot 10^9\,\mathrm{s}^{-1}$ and $\mathrm{C} = 0.416$.

For the threshold energy E_{th} the value 1.12eV is used.

The simulation results are shown in Fig. 3 and Fig. 4. The electron temperature in the maximum generation point increases from 2690 K (0.4μm device $V_D = 2\mathrm{V}, \mathrm{V_G} = 3\mathrm{V}$) up to 7750 K (0.4$\mu$m device $V_D = 3.3\mathrm{V}, \mathrm{V_G} = 0.6\mathrm{V}$). The highest generation rate is about $2.33 \cdot 10^{28}\mathrm{s}^{-1}\mathrm{cm}^{-3}$ (0.4μm device $V_D = 3.3\mathrm{V}, \mathrm{V_G} = 1.4\mathrm{V}$) and the smallest generation rate in the maximum generation point is about $5.62 \cdot 10^{24}\mathrm{s}^{-1}\mathrm{cm}^{-3}$ (0.4μm device $V_D = 2.0\mathrm{V}, \mathrm{V_G} = 0.6\mathrm{V}$)

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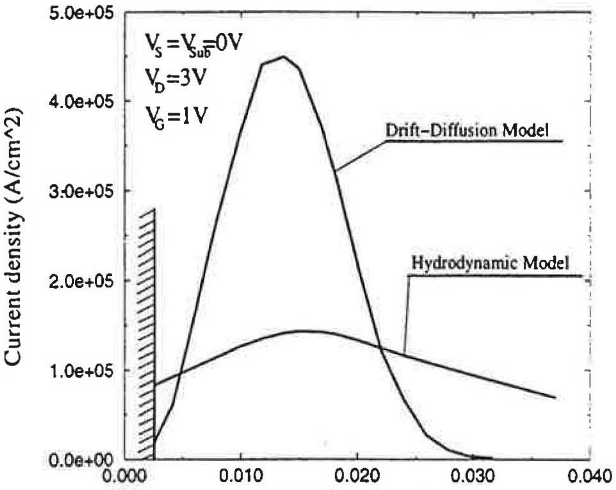

Fig. 1. Current distribution in the maximum generation point at low gate bias

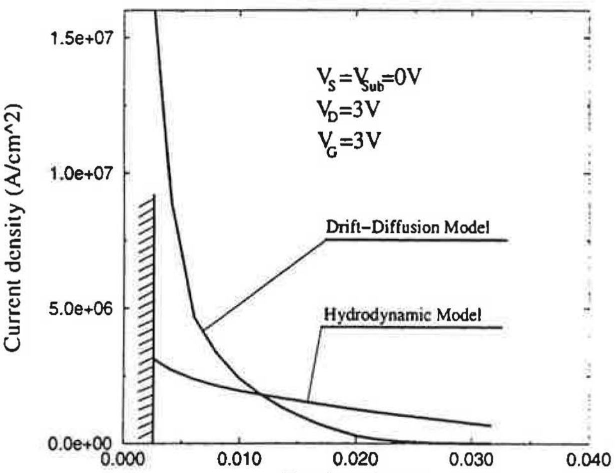

Fig. 2. Current distribution in the maximum generation point at high gate bias

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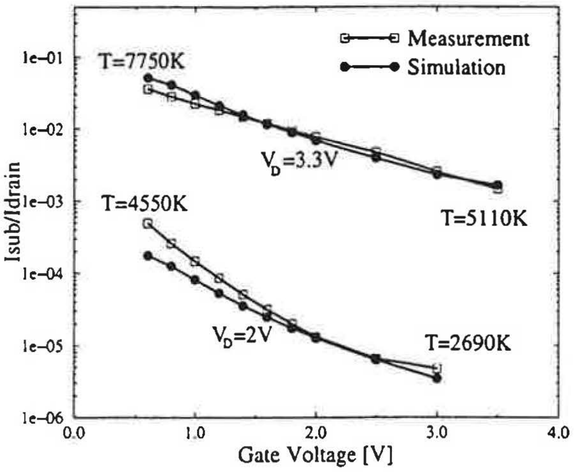

Fig. 3. Multiplication factors for the $0.4\mu m$ device ($V_S = V_{Sub} = 0\text{V}$). Electron temperatures are values in the points of maximum generation.

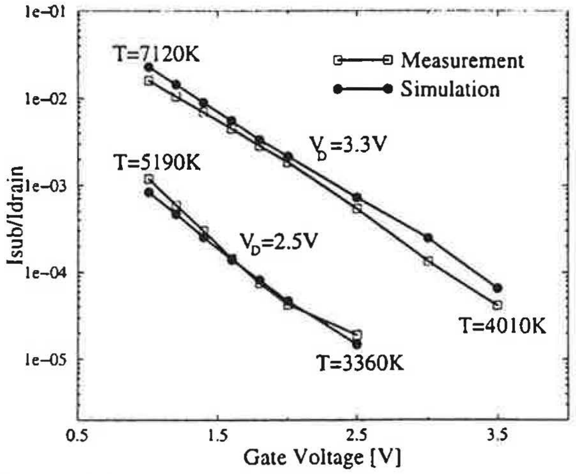

Fig. 4. Multiplication factors for the $1.0\mu m$ device ($V_S = V_{Sub} = 0\text{V}$). Electron temperatures are values in the points of maximum generation.

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