OPTIMIZATION TASKS IN TECHNOLOGY CAD

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Computer Aided Design (CAD), VLSI & simulation, Optimization, Computer-aided analysis, Intelligent simulation environments.

ABSTRACT

This paper presents new features implemented in the simulation environment VISTA which has been developed in our institute. The basic functionality dealing with the simulation of the manufacturing process and electrical characterization of semiconductor devices was extended by automatic experiment generation, parameter fit and optimization features. An example demonstrates the optimization of the electrical characteristics of vertical double-diffused metal-oxide-semiconductor field-effect transistors using these framework capabilities.

INTRODUCTION

The design and fabrication of smaller and faster semiconductor devices relies on the proper numerical simulation of fabrication processes and electrical characteristics. This field of technology engineering is known as Technology Computer Aided Design (TCAD).

For a complete simulation and characterization of a modern Very Large Scale Integration (VLSI) technology several hundred simulation steps have to be computed. Furthermore the process steps have different aspects, like geometry manipulations in etching and deposition steps or changes in the doping profiles during implantation and diffusion steps. Also grid manipulations can be necessary between the simulation steps. For these complex manipulations the Vienna Integrated System for TCAD Applications (VISTA) (Halama et al. 1993) (Pichler et al. 1997) has been developed.

To improve the manufacturability of deep sub-micron devices different variations of process parameters have to be analyzed. For this purpose highlevel analysis functionality has to be supported by a state-of-the art TCAD framework.

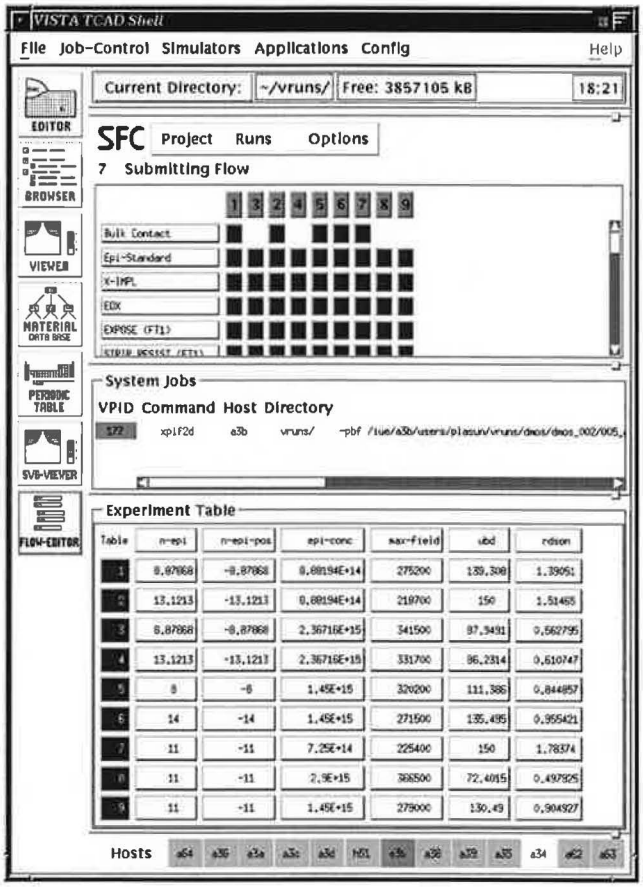

Figure 1: Main components of the VISTA TCAD framework.

THE VISTA FRAMEWORK

The VISTA framework and its modules form a programmable simulation environment for VLSI technology analysis, focusing on process flow simulation and heterogeneous tool integration. Based on process and device simulation capabilities with a variety of simulation tools, split-lot experiments can be defined for fabrication process flows and simulation sequences.

All operating-system dependent services are encapsulated by the operating-system layer which ensures portability over a wide variety of operating systems and platforms.

The VLISP interpreter (VISTA 1996) provides inter-

faces to all internal modules like the operating system layer or the graphical user interface. This makes it possible to run calculation intensive tasks in batch mode.

The *run controller* takes care of the detection of splits, of scheduling multiple runs in parallel operation on a heterogeneous workstation cluster. A persistent *run data base* keeps all simulation results and prevents unnecessary re-computations.

Figure 1 shows the graphical user interface of the VISTA simulation environment.

The topmost window contains the interface of the *run data base* and *run controller* modules. The process steps of the selected process flow are listed on the left side, the split tree of simulation runs in the current project provides direct access to all data of all computed steps and gives a quick summary of the activity states of all simulations.

The *System Jobs* window gives an overview of all active and queued system jobs started on behalf of the *run controller.*

The *Hosts* window displays the busy-state of all network hosts used for submitting system jobs. Dynamic load balancing ensures to use the computation resources efficiently.

The *Experiment Table* window contains a spreadsheet representation of all simulation runs and control and response variables defined for the process flow. Task-level tools like Design of Experiments and Response Surface Methodology generation are directly accessible.

The *flow editor* (Figure 2) offers an intuitive and convenient graphical interface for writing process flows.

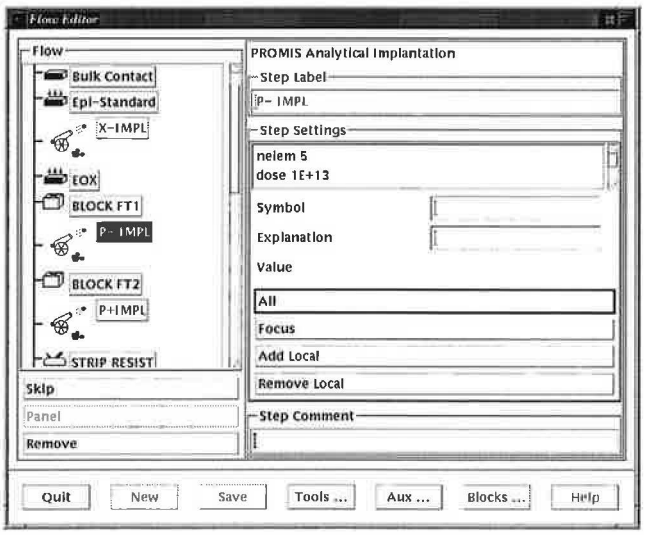

Figure 2: In the VISTA *simulation flow editor* the steps can be specified and modified.

HIGHLEVEL ANALYSIS TOOLS

For full-automatic TCAD analysis highlevel modules with complex features are included.

One of the most important tasks is the optimization of extracted physical parameters for a given input parameter space. Direct optimization methods are not very well suited for this problem, because in order to calculate one set of input and output values, a whole process flow and usually several device tests have to be simulated. To save CPU-time, methods like Design of Experiments (DoE) (Lorenzen and Anderson 1991) and Response Surface Methodology (RSM) (Box and Draper 1987) have to be used.

For automatic generation of experiments, the DoE module can be used. The type of the experimental design can be chosen out of a large number of available types (tab. 1). The result of the DoE is the *design matrix* which is processed by the *run controller* module.

NOM	Nominal Design
SA	Screening Analysis
FUL	Full Factorial Design
CCF	Central Composite Face-centered Design
CCC	Central Composite Circumscribed Design
CCI	Central Composite Inscribed Design
RAN	Random Design
DIA	Diagonal Design
GRI	2D - Grid Design
LAT	Latin Hypercube Design
FRA	Fractional Factorial Design
PLA	Plackett-Burman Design
OME	Orthogonal Main Effect Design
SUP	Supplementary Design

Table 1: Available experimental designs.

After simulating these runs the control and the response values are extracted and written in the *experiment table.*

The RSM module fits polynomial functions to the data in the *experiment table.* As in the DoE module, additional transformations for the controls and the responses can be added.

To accurately model the system behavior, both the DoE and RSM modules make use of transformations of the parameter space to linearize the dependence of the output variables on the transformed input parameters. Subdivision of the parameter space as well as fitting of the response surfaces takes place in transformed space.

For each input parameter, a transformation function can be selected from a set of well-known transformations. If the transformation function requires parameters (*transformation parameters*), these parameters may either be specified explicitly - e.g., in the case when a physical formula has been established, or they

may be determined automatically from a set of sample points. Additionally, it is also possible to automatically select the best out of a given set of transformation functions for a given set of sample points. Thus the user does not need to specify the transformation to use.

For optimizing device performance parameters over a given input variable space, a constrained optimizer with sequential quadratic approximations has been integrated. It minimizes the target function which can be assembled out of input and output values. The gradient is calculated by evaluating finite differences, and the Hessian is built by a BFGS update (Gill et al. 1995). For calibration tasks an optimizer based on the Levenberg Marquardt algorithm (Khalil 1995) is available.

APPLICATION

In this section it will be shown how the electrical parameters of a VDMOS (vertical double-diffused metal-oxide-semiconductor field-effect transistor) can be improved by the highlevel analysis functionality.

The structure of the VDMOS transistor (Figure 3) has the advantage of a low on resistance and a smaller lateral size as lateral DMOS transistors. Due to the high breakdown voltage of up to 100V, they are commonly used as power devices, e.g., in automotive electronics.

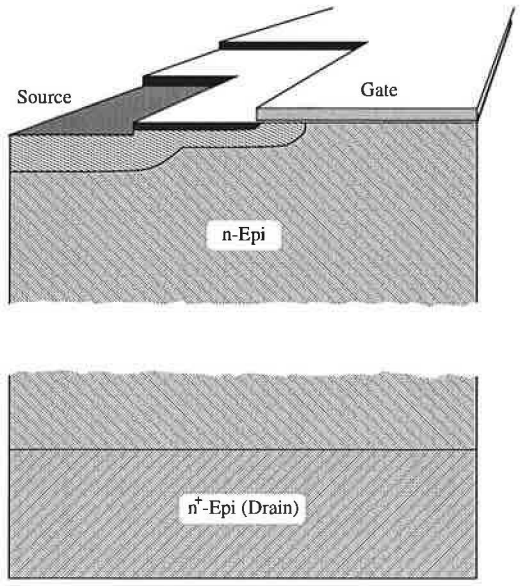

Figure 3: Structure of the vertical DMOS transistor (source metalization and gate oxide are not shown).

The two control variables are the epitaxial doping and the thickness of the epi layer. The extracted responses are the on-resistance `rds-on` and the breakdown voltage `ubd`. The goal of this optimization is to minimize the on-resistance, but to hold the breakdown voltage above 105V.

For the simulation of the process fabrication the simulators SKETCH, ETCH, PROMIS-Implant,

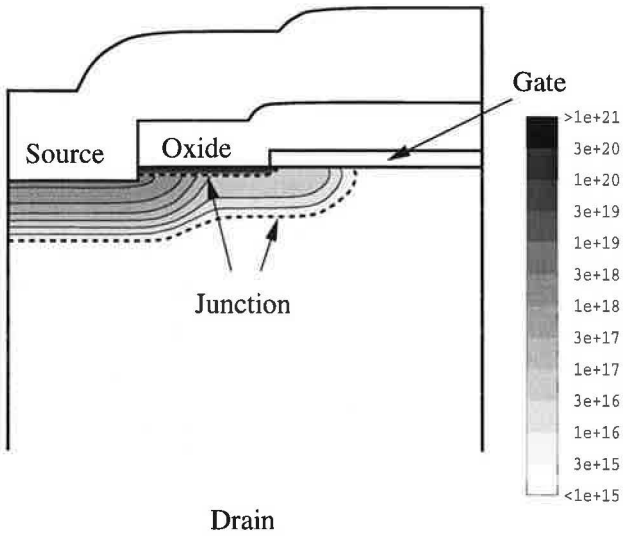

Figure 4: Netdoping concentration (cm^{-3}) of the final VDMOS transistor.

the commercial tool TSUPREM (TMA 1995) and, for the electrical characterization, MINIMOS-NT (Simlinger et al. 1995) were used. The process flow of the device is shown in Figure 2.

The optimization problem is defined by a small VLISP program (Figure 5). The function `Eve-Define-Control` defines an internal name of a control variable (first argument) from a process step and from a parameter of this step (second and third argument). The key `:eval-expr` can be used to calculate this internal variable out of others, like `n-epi-pos` – the button position of the epi-layer – which is the negative value of `n-epi` the epi thickness. `Eve-Set-Control` assigns default values, ranges and transformations to the internal control variables. `Eve-Define-Response` defines a control variable and has the same arguments as `Eve-Define-Control`.

The functions `calc-breakdown` and `calc-rdson` are used to calculate the specified values out of the `iv-data` structure.

Figure 6 shows the structure of the optimization task defined in the last part of the program. The Design of Experiments module generates a Central Composite Inscribed experimental design out of the defined control ranges. These 9 runs where simulated on the workstation cluster, scheduled by the *run controller*. After all steps are finished and the responses are extracted, the RSM-evaluator module calculates results, queried by the constrained nonlinear optimizer.

The minimum value of the on-resistance is found on the constraint where the breakdown voltage is the lower limit of 105V. Figure 7 shows the target function (on-resistance) versus the parameter space of the control variables (epi-doping concentration and epi layer thickness). Thus the optimum process parameters are found with `n-epi` = 10.37μm, `epi-conc` = $1.9e15\text{cm}^{-3}$, and $R_{DS(on)} = 0.614\Omega$ (Figure 4).

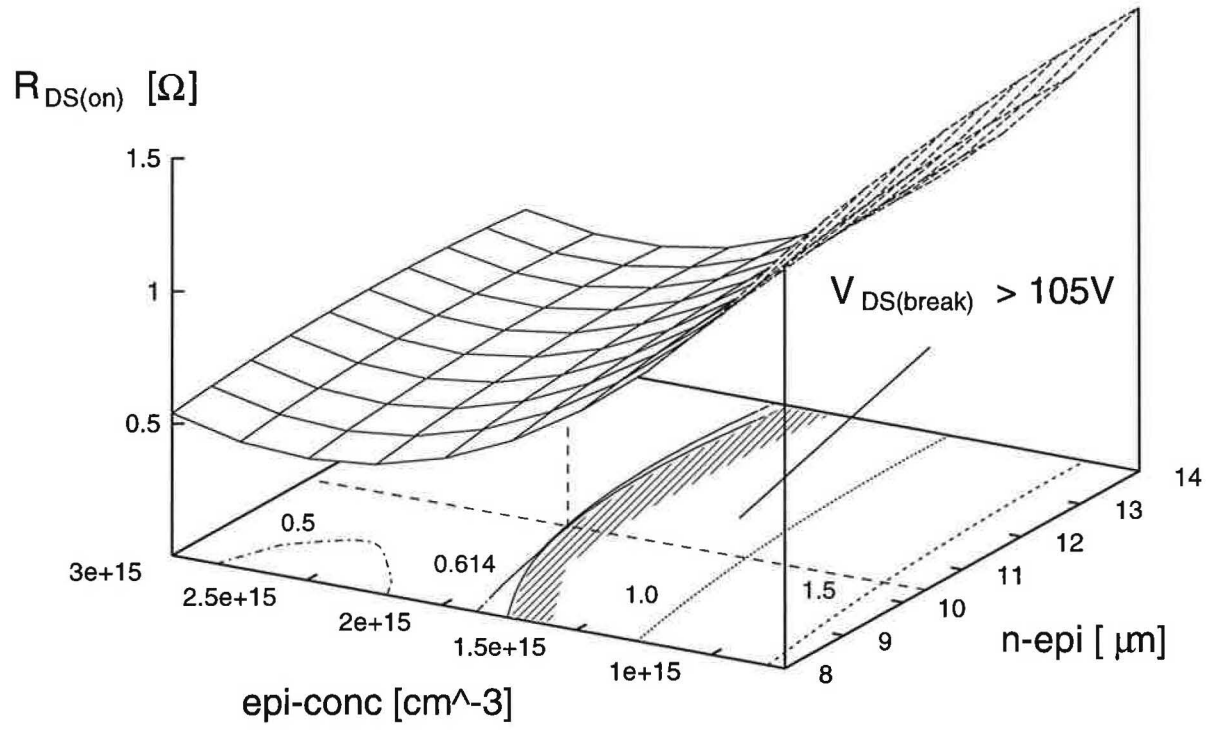

Figure 7: Response surface of the target function.

CONCLUSION

In the example of the vertical DMOS transistor we have shown that the VISTA framework is well suitable for the complex task of optimizing the device parameters. The capabilities of split-lot experiments, Response Surface Methodology, Design of Experiments, and optimization make VISTA a powerful instrument not only for microelectronics but also for smart power technology.

FURTHER RESEARCH

For an interactive use of these highlevel analysis modules a graphical user interface with drag and drop features will be implemented. Further new concepts of tool binding and database management have to be developed to handle three-dimensional simulators and their data in the near future.

ACKNOWLEDGMENT

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```
;; process flow
(Project :flow-file #"~/vwork/flows/dmos.sfe")

;; creates an evaluation object
(Flow-Eve)

;; definition of the control variables
(Eve-Define-Control "n-epi"      "Epi-Standard"
                    "thickness")

(Eve-Define-Control "n-epi-pos"  "Bulk Contact"
                    "y-offset"
                    :eval-expr '(* -1 n-epi))

(Eve-Define-Control "epi-conc"   "Epi-Standard"
                    "dope-conc")

;; assign values to the control variables
(Eve-Set-Control "n-epi"    10.5
                 :min        8
                 :max       14)

(Eve-Set-Control "epi-conc" 1.45e15
                 :min 0.725e15
                 :max 2.9e15
                 :trans 'log)

;; definition of the response variables
(Eve-Define-Response "max-field"
                     "MMNT-breakdown"
                     "max-filed"
            :eval-expr '(apply 'max max-field))

(Eve-Define-Response "ubd"
                     "MMNT-breakdown"
                     "iv-data"
            :eval-expr '(when ubd
                          (calc-breakdown ubd)))

(Eve-Define-Response "rdson"
                     "MMNT-rdson"
                     "iv-data"
            :eval-expr '(when rdson
                          (calc-rdson rdson)))

;; optimization tasks
(sequence
 '(Eve-Doe 'CCI)
 '(Rsm-Eve "rsm-eve" :skip '("n-epi-pos"))
 '(Eve-Optimize "target"
   :eve "rsm-eve"
   :range-eve sfc::current-eve
   :eval-exp '(+ rdson
                 (* 100 (if (plusp (- 110 ubd))
                            (- 110 ubd) 0)))))
```

Figure 5: Listing for solving the optimization problem for the VDMOS transistor example.

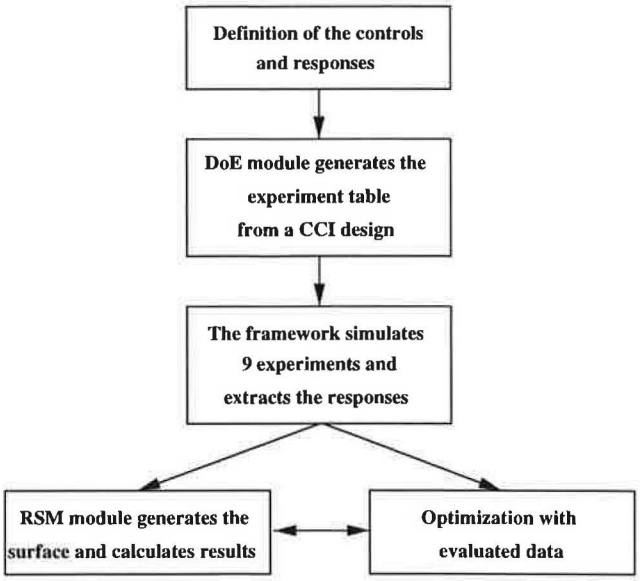

Figure 6: Structure of the optimization task.

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BIOGRAPHY

Richard Plasun was born in Vienna, Austria, in 1969. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in March 1995. He is currently working towards his doctoral degree. From October to December 1996, he was with the National Semiconductor Cooperation in Santa Clara, where he concentrated on tool binding and process optimization aspects. His scientific interests include linear and nonlinear optimization, technology CAD framework aspects and software development.