STAP — A FINITE ELEMENT SIMULATOR FOR THREE-DIMENSIONAL THERMAL ANALYSIS OF INTERCONNECT STRUCTURES

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ABSTRACT

We have developed a two- and three-dimensional simulation tool for a coupled electro-thermal analysis of VLSI interconnect lines, which uses the finite element method to solve Laplace's equation and the heat conduction equation. Thereby, triangular and tetrahedral grid elements with linear and quadratic shape functions are used. Two preprocessors allow a layer-based input of the simulation geometry and specification of boundary conditions for voltage, current and temperature. They are also responsible for the generation of the simulation grid. The main program calculates the potential and temperature distributions and extracts the resistance between two contacts. Two application examples are presented.

INTRODUCTION

In deep submicron designs the interconnect structures significantly determine the overall circuit behavior (Bohr 1995). Beside the general known limitation of circuit speed by the interconnect resistance and capacitance the influence of thermal effects gains in significance. As a consequence of the increasing packaging density the design comes closer to the physical limits for temperature and current density. Careful investigations during the design phase become necessary regarding circuit reliability. Since experimental measurements of these physical effects are often expensive, inaccurate, or impossible, there is an increasing need for numerical calculation.

Conventional ECAD tools supply analytical models for resistance extraction, which allows to calculate generated heat and estimate the temperature. Since this approach often proves as too inaccurate, a full three-dimensional simulation becomes necessary. General purpose FEM packages do a good service for this task, but the specification of the models, geometry and boundary conditions may be a difficult time consuming job. For this reason the simulator STAP (Smart Thermal Analysis Program) was developed. It has been designed specially for interconnect applications, thus enabling a high level of optimization.

MATHEMATICAL BACKGROUND

For the numerical calculation of Joule self-heating effects two partial differential equations have to be solved. The first one describes the electric sub-problem,

$$\operatorname{div}(\gamma_E \operatorname{grad}\varphi) = 0. \tag{1}$$

The electric potential φ needs to be solved for only inside domains composed of electrically conducting material (γ_E represents the electrical conductivity). The next step is to calculate the power loss density p,

$$p = \gamma_E(\operatorname{grad}\varphi)^2. \tag{2}$$

Then, the static heat conduction equation has to be solved to obtain the distribution of the temperature T,

$$\operatorname{div}(\gamma_T \operatorname{grad} T) = -p. \tag{3}$$

γ_T represents the thermal conductivity.

MODELING OF INTERCONNECT STRUCTURES FOR THERMAL SIMULATIONS

For the dependence of the electrical resistivity of the conductors on the temperature we use a linear model:

$$\gamma_E = \gamma_0 \frac{1}{1+\alpha(T-T_0)}. \tag{4}$$

γ_0 is the electrical conductivity at the temperature T_0 of 300K, and α is a constant temperature coefficient.

The temperature dependence of the thermal conductivity is very low for commonly used interconnect materials and can be neglected in most applications.

For accurate simulation results it is important to specify a sufficiently large simulation domain. We found that the lateral width of the simulation area should be chosen at least 1.2...1.5 times the thickness of the thickest layer (i.e. the Si substrate) but it is possible to omit small geometric features in areas where accuracy is not critical. A reduction of the simulation domain first causes an error in the calculated temperature while current densities and temperature gradients are still accurate.

Areas of the chip surface exposed to air are difficult to model with the heat flow equation since the heat transport mechanism in gases is dominated by convection, not conduction. The total thermal resistance for the boundary to air is nonlinear and depends on some poorly known factors (e.g. airspeed). Fortunately the thermal conductivity of air is very low compared to other materials. However, in most cases the air-boundary cannot be totally neglected because it covers a major part of the chip and a considerable amount of the generated heat is dissipated thereby. We tackle this problem with a very simple model, namely a 1μm thick layer of "air" with a thermal conductivity of $0.015 \ldots 0.03 \frac{\mathrm{W}}{\mathrm{mK}}$ and constant temperature (ambient temperature) on the top. This model has been found to be sufficient for most applications since the obtained results compare well to measurements.

THE PROGRAM STAP

The simulator STAP uses the finite element method to solve Laplace's equation (1) to calculate the potential φ inside the conductors. The power loss density is determined according to (2). Then the heat diffusion equation (3) is solved over the whole simulation domain to obtain the temperature distribution, again using the finite element method. Because of the temperature dependence of the electrical conductivity (4), the whole simulation has to be repeated in a loop until an equilibrium is established. Triangular and tetrahedral grid elements can be used for two- and three-dimensional simulations. The calculations can be performed with linear and quadratic shape functions. For efficient utilization of computer memory the sparsely occupied stiffness matrix is stored in a compressed format (MCSR). A preconditioned conjugate gradient solver is used to solve the large linear systems. For highly accurate results a global grid refinement algorithm is implemented.

Two preprocessors (LAYGRID and CUTGRID (Bauer et al. 1993)) are used for specification of the simulation geometry and contacts (both electrical and thermal) in terms of polygonal layers. The preprocessors are also responsible for the generation of the simulation grid. In two dimensions the mesher called Triangle (Shewchuck 1996) is used, for the three-dimensional case we utilize a layer-based grid generation method (Fleischmann et al. 1996).

APPLICATIONS

Two application examples will be presented, namely a single Aluminum line, where thermal simulations allowed to extract some poorly known material parameters, and a via-chain test-structure which is commonly considered for reliability experiments.

Al-Line Structure

The structure of the first simulation example is shown in Fig. 1. The total length of the aluminum line is 500μm and its width is 0.5μm, 0.95μm, 2μm, or 3μm. There are two dummy lines with a width of 1.5μm on each side of the center line (Fig. 1 shows only one of them) spaced at 0.5μm.

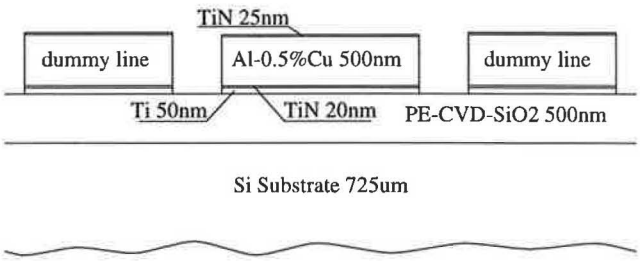

Figure 1: Cross sectional view of the Al-line test structure.

This structure has been simulated with no passivation and 700nm SiO_2 passivation. Table 1 shows the material properties used for all simulations.

Material	ρ [$\mu\Omega$cm]	α [1]	γ_T [$\frac{\mathrm{W}}{\mathrm{mK}}$]
Al-0.5%Cu	3	0.0042	238.00
Ti	60	0.0041	15.00
TiN	600	0.0041	10.00
W	10	0.0038	140.00
Si			84.00
PE-CVD-SiO_2			1.30
thermal SiO_2			1.35
SiN			7.30
Air			0.023

Table 1: Material properties.

The middle line is loaded by a current of 5–150mA. The dummy lines carry no current. The bottom of the Si substrate is mounted on a metal plate which is kept at room temperature. The top of the structure is exposed to air, which is also at room temperature.

The simulation results have been fitted to the experimental data by variation of some poorly known material parameters. Best results were achieved with a thermal conductivity of

- $1.3\frac{W}{mK}$ for the PE-CVD SiO_2 layer and
- $1.2\frac{W}{mK}$ for the SiO_2 passivation layer.

Figures 2 and 3 show the dependence of the calculated temperatures on the applied current (solid lines). The measured data are represented by symbols.

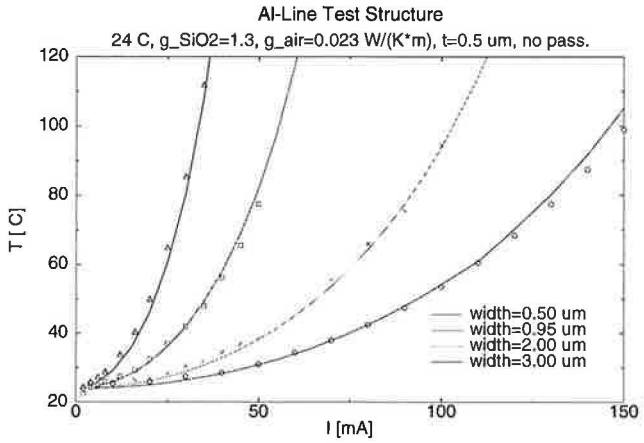

Figure 2: Simulated and measured data for the structure without passivation.

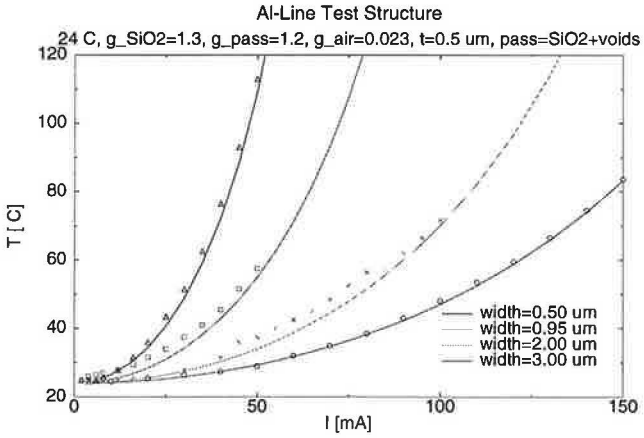

Figure 3: Simulated and measured data for the structure with SiO_2 passivation.

Via-Chain Structure

The second test structure is a chain of Tungsten vias (see Fig. 4). Thicknesses of the layers are 600nm for SiO_2, 580nm for Metal 1+2 (40nm/60nm Ti/TiN barrier, 440nm AlCu(0.5%), 40nm TiN ARC), and 700nm for the passivation. Table 1 shows the material properties used for the simulation.

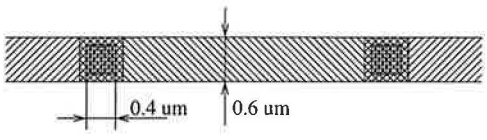

Figure 4: Layout of Tungsten-via test structure.

A current of 34mA is applied to the ends of the line, which is equivalent to a current density of approximately $13MA/cm^2$ in the AlCu line and approximately $21MA/cm^2$ in the Tungsten plug. The bottom of the Si-Substrate is kept at constant temperature of 24°C.

Since the geometric structure repeats periodically it is only necessary to simulate one single via. Figure 5 shows the calculated potential distribution inside the AlCu lines and the via. The high resistivity of TiN causes a large voltage drop at the bottom of the W-plug resulting in a high heat generation rate.

Figures 6 and 7 show the temperature profile cross-section and on the surface of the conductors in an enlarged scale. The maximum temperature of 99°C is reached on the bottom of the Tungsten plug and coincides well with the heat generation rate.

MEMORY AND CPU TIME CONSUMPTION

The dynamically allocated memory and CPU time consumption of the simulator STAP has been measured on a Silicon Graphics Workstation with a MIPS R8000 CPU at 90 MHz running IRIX64. Figure 8 shows the dependence on the total number of grid nodes.

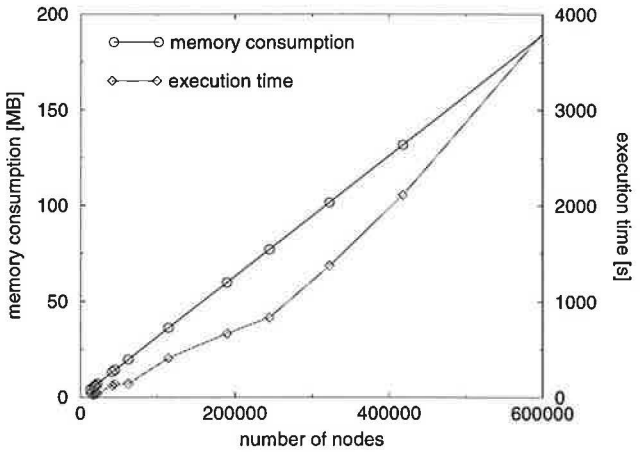

Figure 8: Memory and CPU time consumption on a Silicon Graphics workstation.

CONCLUSION

We have developed a Finite Element based simulation package for coupled electro-thermal interconnect analysis and formulated models suitable for most applications. The program is freely available and has been tested with a large number of applications. The simulator has been used for the extraction of thermal resistances from measured data and to locate hot spots in interconnect vias. The obtained results compare well to experimental measurements. Future plans include the implementation of a transient simulation mode and a fully unstructured mesh generation method.

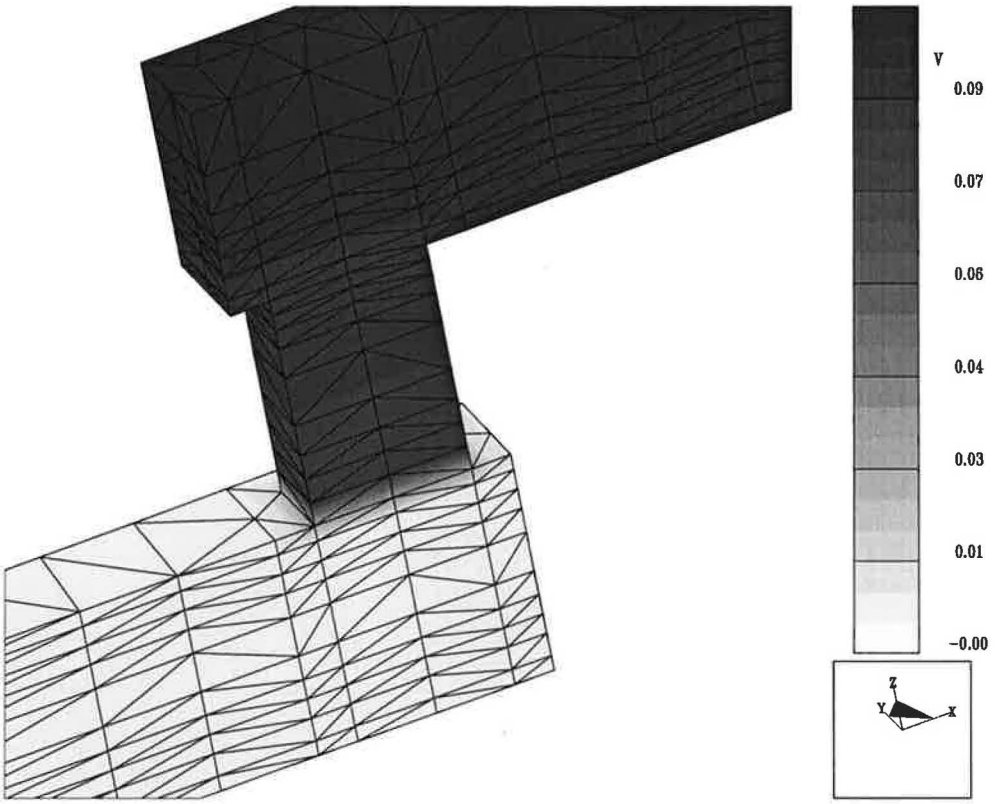

Figure 5: Electric potential profile on one half of the test structure.

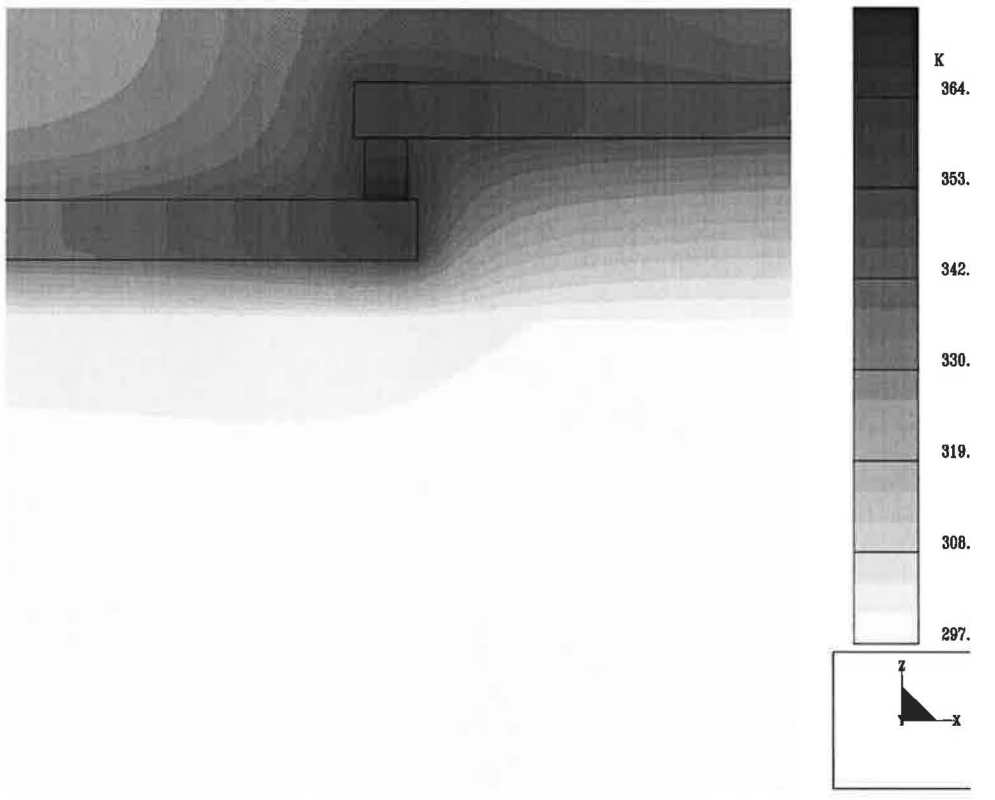

Figure 6: Temperature profile on the cross-sectional view of the test structure.

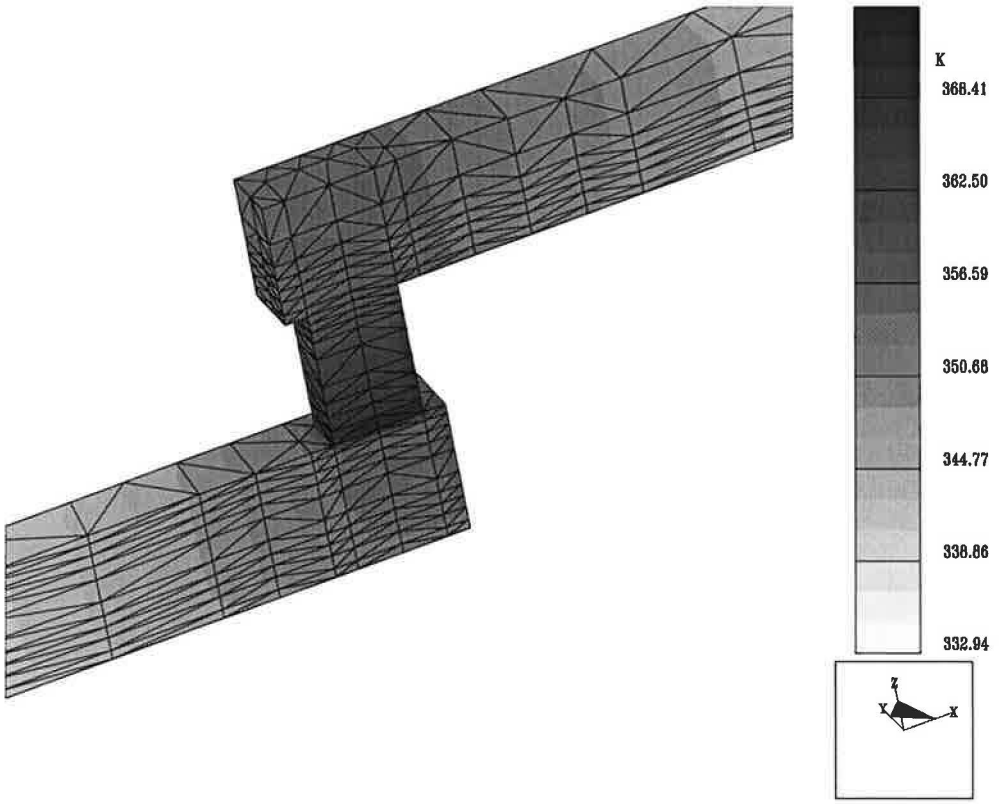

Figure 7: Temperature profile of one half of the conductor structure.

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BIOGRAPHY

Rainer Sabelka was born in Vienna, Austria, in 1969. He studied electrical engineering at the Technical University of Vienna, where he received the degree of 'Diplomingenieur' in 1994. He joined the 'Institut für Mikroelektronik' in January 1995. He is currently working for his doctoral degree. He held visiting research positions at Digital Equipment Corporation, Hudson, in 1996 and at Sony, Atsugi, Japan in 1997. His scientific interests include three-dimensional interconnect simulation of multilevel wired VLSI circuits, visualization and software technology.