Single-Electron Memories

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One of the most promising applications of single-electronics is a single-electron memory chip. Such a chip would have orders of magnitude lower power consumption compared to state-of-the-art dynamic memories, and would allow integration densities beyond the tera bit chip. In order to reach this goal certain questions have to be solved: Is room temperature operation possible? How can single-electron memories be made random background charge independent? Is it possible to mass fabricate such single-electron devices?

Thus we studied various single-electron memory designs by simulation. Our main focus was on comparing operation temperature and random background charge independence. We examined already proposed memory designs, such as single-electron flip-flop [1], single-electron trap [2], Q_0-independent memory [3], and new variations which try to improve random background charge independence and manufacturability with todays process techniques.

Very often a single-electron transistor is used to read out the charge stored in a single-electron memory cell. Unfortunately, the single-electron transistor is strongly background charge dependent, and difficult to fabricate for room temperature operation. We show that the substitution of a single-electron transistor which consists of two tunnel junctions with a granular film batch which consists of many tunnel junctions solves many problems. Firstly, a granular film batch exhibits a similar Coulomb blockade and similar Coulomb oscillations as a single-electron transistor and thus can be substituted without change in functionality. Secondly, the individual grains of granular films which can have diameters in the nano-meter range provide with their minuteness a Coulomb blockade of up to 1eV and thus allow room temperature operation. Thirdly, the behavior of a batch which consists of hundreds and thousands of grains does not depend on individual grains, but on the ensemble characteristics. These are much easier to control in an industrial mass production and show much better independence to random background charges than the single-island single-electron transistor. Finally, the lateral dimensions of the granular film batch can be in the range achievable with todays e-beam lithography ($\sim$30 nm). Hence the necessity for highly advanced lithography is absent.

The conclusion of our simulations is, that a combination of granular film processes with state-of-the-art lithography allows the production of random background charge independent memory chips operating at room temperature.

[1] A. N. Korotkov, R. H. Chen, and K. K. Likharev. Possible performance of capacitively coupled single-electron transistors in digital circuits. *Journal of Applied Physics*, 78(4):2520–2530, August 1995.

[2] K. Nakazato and H. Ahmed. The multiple-tunnel junction and its application to single-electron memory and logic circuits. *Japanese Journal of Applied Physics*, 34(Part1, 2B):700–706, February 1995.

[3] K. K. Likharev and A. N. Korotkov. Analysis of Q_0-independent single-electron systems. In *Int. Workshop on Computational Electronics*, page 42, 1995.