VLSI Performance Metric Based on Minimum TCAD Simulations

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***Abstract*— A new approach to performance metrology and qualification of digital VLSI processes with TCAD simulations is proposed. The method yields performance data on the system level directly from raw electrical device data obtained with a minimum set of device simulations. The key performance and qualification parameters are identified, pointing out the differences between these and traditional device performance metrics, and the methods to determine these parameters from the device data are described.**

I. Introduction

Traditional device performance and qualification criteria are primarily drive current, leakage, and threshold control. However, these parameters are very indirectly linked to the actual system performance. Previous work on systems analysis was usually based on analytical IV and CV equations with parameters analytically derived from nominal process parameters [2], [3]. However, such analytical models are ever less adequate to capture the non-ideal behavior of advanced deep-sub-micron devices. On the other hand, complete device characterization and circuit simulation to determine the system performance is often not affordable and, as in the case of deep-sub-micron devices, not a straight-forward task. Therefore, a new method was developed by carefully selecting the relevant parameters and device data sets that can be combined with a suitable system model.

II. System Model

In this work we use a simple model of a homogeneous digital system, which is described by the parameters a, ld, F_{io}, L_M, and c_M which are activity ratio, logic depth, average fan-in/fan-out, average interconnect length, and interconnect capacitance per length. Primary operating parameters are $V_{DD,nom}$, L_{nom}, $T_{j,nom}$, and $f_{c,nom}$ which are the nominal supply voltage, gate length, junction temperature, and clock frequency. Furthermore, to enable investigations based on just one device type (e.g., the NMOS transistor), all analyses can be carried out assuming symmetric (but statistically independent) transistors. For clarity, most equations are only given for the single-device-type case.

III. Device Simulation

In order to obtain the necessary data a minimum set of device simulations is carried out for a given structure at the nominal junction temperature T_j (cf. Table I). The data sets 1–3b yield the main performance parameters, and they are functions of the supply voltage, so they cover also V_{DD} variations. The simulations 3a/3b render the terminal charges for the on-state and the off-state respectively (cf. [4]). The sets 4a/4b determine the noise margins and are valid for a fixed V_{DD}. The sets 5a/5b are independent of V_{DD} and render only informational parameters, so they are optional.

TABLE I
Device simulations

	simulation	device data
1	dc step V_G and V_D	$I_{on}(V_{DD})$
2	dc step V_D, $V_G = 0$V	$I_{off}(V_{DD})$
3a	transient ramp V_G, $V_D = 0$V	$Q_{G,on}(V_{DD}), Q_{D,on}(V_{DD})$
3b	transient ramp V_D, $V_G = 0$V	$Q_{G,off}(V_{DD}), Q_{D,off}(V_{DD})$
4a	dc step V_G, $V_D = V_{DD}/2$	$I_D(V_G, V_D = V_{DD}/2)$
4b	dc step V_D, $V_G = V_{DD}/2$	$I_D(V_D, V_G = V_{DD}/2)$
5a	dc step V_G, $V_D = 50$mV	$I_{Dlin}(V_G)$
5b	dc step V_D (≤ 1V), $V_G = V_{T,lin}$	$I_D(V_D, V_G = V_{T,lin})$

IV. Key Parameters and Informational Parameters

The primary performance parameters and the qualification parameters used for pass/fail decisions are listed in Table II. The numbers in the 'source' column refer to the required device simulations (cf. Table I). It is important to note, that the threshold voltage does not appear in this list, nor is it needed in any other way. However, as the threshold voltage is a very vivid and popular parameter $V_{T,lin}$ has been added to a list of so-called informational parameters, i.e., quantities that are only indirectly linked to performance and sensitivity (cf. Table III). For

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all parameter definitions that require arbitrary threshold currents (such as for $V_{T,sat}$, V_{punch} [5]) one unique characteristic current I_T is extracted from data set 5b by extrapolating $\log(I_D)$ to $V_D = 0\text{V}$.

TABLE II
System performance and qualification parameters

	parameter	source
t_d	inverter delay	1, 3
E_s	switching energy	1, 2, 3
$f_{c,max}$	maximum clock frequency	1, 3
$f_{c,min}$	minimum clock frequency	2, 3
NM	normalized noise margins	4
OS	normalized output voltage swing	2, 5a
A_{inv}	inverter gain	4

TABLE III
Informational parameters

	parameter	source
I_{on}	turn-on current	1
I_{off}	turn-off current	2
$V_{T,lin}$	linear threshold voltage	5
$V_{T,sat}$	saturation threshold voltage	4a
I_T	threshold current	5
R_{dibl}	surface DIBL rate	2
R_{punch}	sub-surface DIBL rate	2
V_{punch}	punch-through voltage	2, 5b

V. Dynamic Inverter Model

The inverter delay t_d is determined by the drive current I_{on}, V_{DD}, and the nonlinear capacitances of the intrinsic transistors. The influence of the latter can also be formulated as follows: For switching one transistor a total switching charge of

$$\begin{aligned} Q_{sw}(V_{DD}) &= Q_{G,on}(V_{DD}) - Q_{G,off}(V_{DD}) + \\ &\quad + Q_{D,off}(V_{DD}) - Q_{D,on}(V_{DD}) \end{aligned} \tag{1}$$

is transferred. The charges can be obtained as a function of V_{DD} from two transient simulations (4a, 4b) [4]. An effective load capacitance C_L including interconnects is then determined as

$$C_L = \frac{Q_{sw}}{V_{DD}} + c_M L_M \tag{2}$$

and the loaded-inverter delay is estimated as $t_d = V_{DD}C_L/I_{on} - I_{off}$. The maximum clock frequency is then $f_{c,max} = 1/(ldt_d)$ (inverter chain model). Although these two expressions are generally not very accurate, they reflect the various tendencies very closely and are therefore well-suited for optimization purposes.

VI. Power Consumption

Sum total of dynamic and static power consumption, and the switching energy per transistor are modeled as [3]

$$P = P_{dyn} + P_{stat} = af_c {V_{DD}}^2 C_L + V_{DD} I_{off} \tag{3}$$

and

$$E_s = \frac{P}{af_c} = {V_{DD}}^2 C_L + V_{DD} I_{off} \frac{1}{af_c} \tag{4}$$

neglecting the crow-bar current during the switching transient, which is usually applicable. According to the system model the power delay product is related to the switching energy as $Pt_d = E_s \cdot af_c t_d$.

VII. Noise Margins, Inverter Gain, and Output Swing

The determination of the static noise margins NM_H, NM_L would require circuit simulation of an inverter. A close estimate of the noise margins can be determined from just two DC simulations (4a, 4b). Exploiting the fact that the input voltages V_{IH}, V_{IL} will be around $V_{DD}/2$ and that one of the output transistors is in saturation, the following algorithm can be used to determine the noise margins: The currents and conductances at the critical voltages (i.e., where the inverter gain is $|A_{inv}| = 1$) are estimated by scaling two IV curves according to Fig. 2. With $I_1(V) = I_D(V_G = V, V_D = V_{DD}/2)$, $I_2(V) = I_D(V_D = V, V_G = V_{DD}/2)$, and $I_{sc} = I_1(V_{DD}/2) = I_2(V_{DD}/2)$ the critical voltages V_{IL}, V_{OH} can be obtained by solving:

$$\begin{aligned} I_1(V_{IL}) \tfrac{I_2(V_{OH})}{I_{sc}} &= I_2(V_{DD} - V_{OH}) \tfrac{I_1(V_{DD} - V_{IL})}{I_{sc}} \\ \tfrac{\partial I_1(V_{IL})}{\partial V_{IL}} \cdot \tfrac{I_2(V_{OH})}{I_{sc}} &= -\tfrac{\partial I_2(V_{DD} - V_{OH})}{\partial V_{OH}} \cdot \tfrac{I_1(V_{DD} - V_{IL})}{I_{sc}} \end{aligned} \tag{5}$$

The input-low noise margin NM_L is then

$$NM_L = \frac{V_{IL} - (V_{DD} - V_{OH})}{V_{DD}} \tag{6}$$

and the input-high noise margin is determined accordingly. In the case of a single-device analysis the inverter transfer curves are symmetrical and the noise margins are $NM_L = NM_H = NM$. The noise margins of gates can be estimated also by scaling the currents I_1, I_2 according to the fan-in and the logic style (e.g., for a static-logic NAND gate with a fan-in of F_{in} we obtain $\tilde{I}_1 = I_1/F_{in}$, $\tilde{I}_2 = I_2 \cdot F_{in}$). Inverter gain and output voltage swing are determined as $A_{inv} = g_m/g_o|_{V_G = V_D = V_{DD}/2}$ and $OS = (V_{DD} - 2I_{off}R_{on})/V_{DD}$ from 4a/4b and 2/5a respectively.

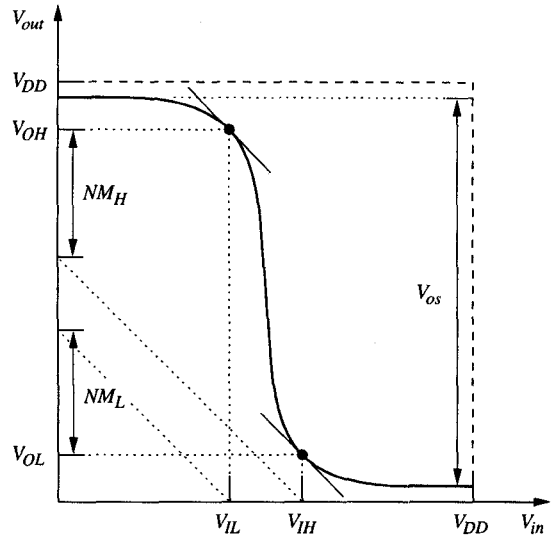

Fig. 1. Definition of static noise margins and output swing

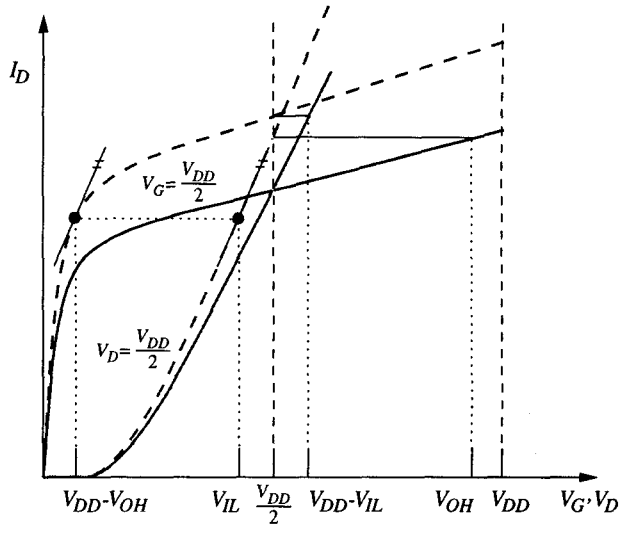

Fig. 2. Extraction of static noise margins

VIII. Application

To obtain the raw device data, MINIMOS [1] is used as device simulator and the device structures can be generated either by coupled process simulation, or, with an additional program, from analytical profile descriptions.

Table IV shows results from a pocket-implanted LDD NMOS device with $L_{nom} = 0.18\mu$m, $t_{ox} = 5$nm, and $X_j = 0.09\mu$m designed for operation at $V_{DD} = 1.5$V. The system parameters used for analysis were $ld = 7$ and $a = 0.1$ (interconnect capacitances were not considered). The evaluation was carried out for the nominal case ('nominal') and two worst-case corners ('a': $T = T_{max} = 125°$C, channel and pocket implant doses, and L reduced by 20%; and 'b': $T = T_{min} = 0°$C, channel and pocket implant doses increased by 50%, and L increased by 20%). The data 'c' are the same as 'a' except that t_{ox} was reduced instead of the channel and pocket implants (to obtain the same shift in $V_{T,lin}$). Each of these evaluations takes a CPU time of about 5 minutes on an HP735 workstation.

TABLE IV
Performance of a pocket-implanted LDD NMOST
($L = 0.18\mu$m, $V_{DD} = 1.5$V)

case (see text)	$V_{T,lin}$ [V]	t_d [ps]	E_s [fJ]	$f_{c,max}$ [GHz]	$\frac{f_{c,max}}{f_{c,min}}$	NM [Vdd]	A_{inv}
nominal	0.44	47.6	18.1	3.0	$8.5 \cdot 10^4$	0.36	9.7
a: $N\downarrow T\uparrow L\downarrow$	0.21	34.2	27.2	4.2	$7.3 \cdot 10^0$	0.29	6.1
b: $N\uparrow T\downarrow L\uparrow$	0.67	92.6	19.3	1.5	$2.6 \cdot 10^9$	0.44	34.2
c: $t_{ox}\downarrow T\uparrow L\downarrow$	0.23	35.9	19.8	4.0	$7.1 \cdot 10^1$	0.32	9.9

The curves in Figs. 3–6 are the inverter delay, switching energy, maximum clock frequency, and clock frequency margin $f_{c,max}/f_{c,min}$ for the three cases. From Fig. 6 and Table IV it can be seen that the device fails at corner 'a' because $f_{c,max}/f_{c,min}$ is too small for dynamic logic. The noise margins, however, are still $30\%V_{DD}$, which would allow static-logic operation.

The impact of supply and threshold voltage on maximum clock frequency and switching energy is shown in Figs. 7 and 8. For the simulations t_{ox} was varied from 1nm to 18nm, and $f_{c,max}$ and E_s were plotted over V_{DD} and the extracted $V_{T,lin}$.

IX. Conclusion

Our new approach combines the immediate relevance of system models with the accuracy of device simulation at minimum computing effort. Yielding system information directly for arbitrary operating points, like worst-case process corners, makes this method an ideal tool for fast device evaluation without the need of full compact-model characterization during the optimization process.

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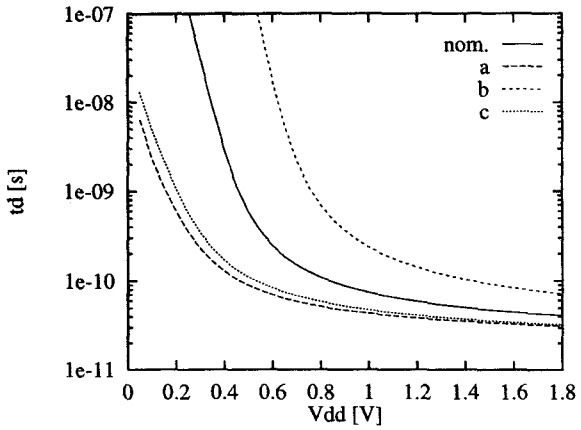

Fig. 3. Inverter delay t_d vs. V_{DD}

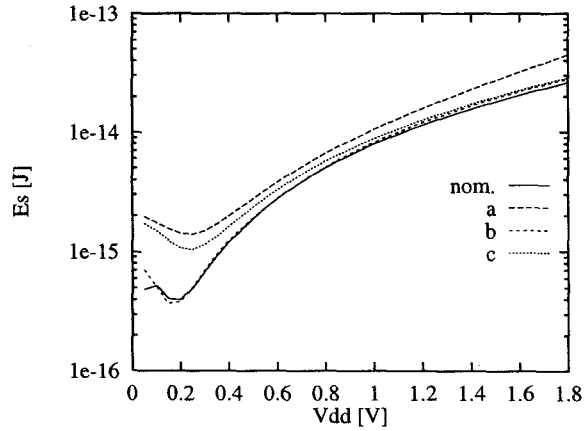

Fig. 4. Switching energy E_s vs. V_{DD}

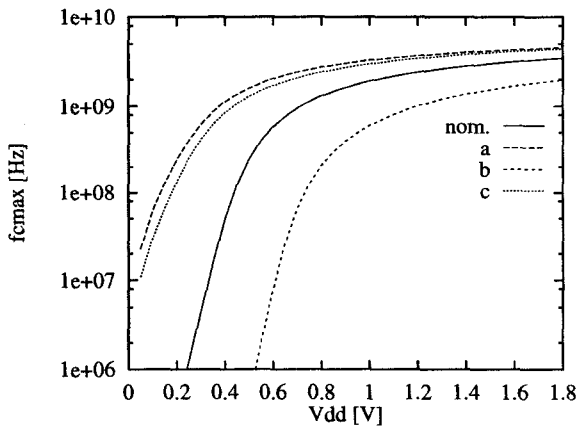

Fig. 5. Maximum clock frequency $f_{c,max}$ vs. V_{DD}

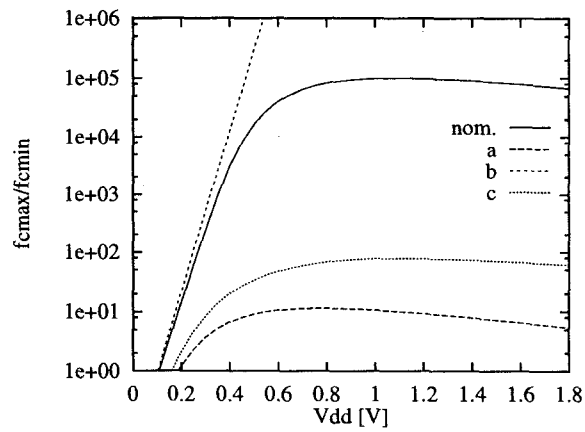

Fig. 6. Clock frequency margin $f_{c,max}/f_{c,min}$ vs. V_{DD}

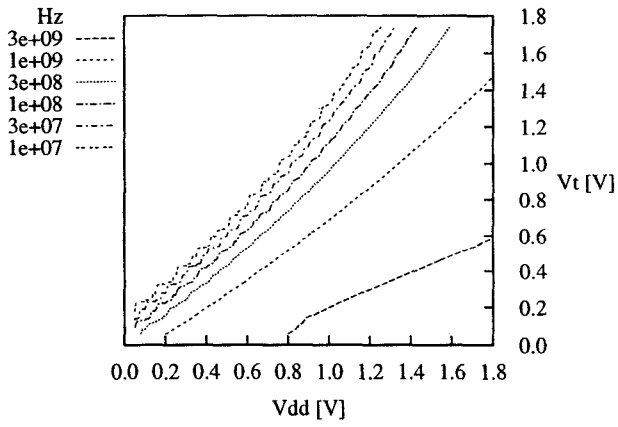

Fig. 7. Maximum clock frequency $f_{c,max}$ vs. V_{DD} and $V_{T,lin}$

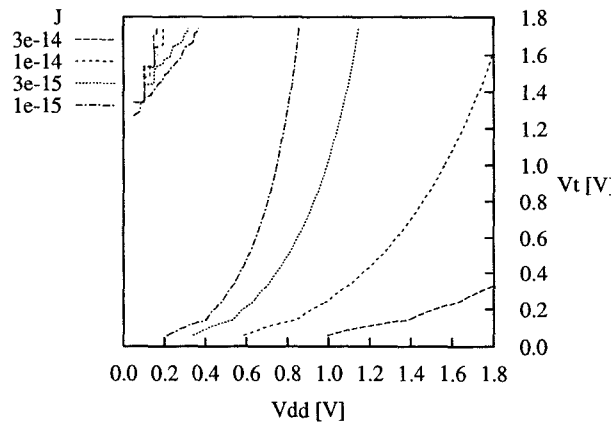

Fig. 8. Switching energy E_s vs. V_{DD} and $V_{T,lin}$