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A CMOS IC for Portable EEG Acquisition Systems

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Abstract *- This paper presents a monolithic low-power, low-noise analog front-end electroencephalogram (EEG) acquisition system. It draws only 500 μA from a standard 9 V battery, making it suitable for use in portable systems. Although fabricated in a standard CMOS technology, using current feedback techniques it achieves a CMRR of 100 dB while the total input noise referred to input is kept as low as 1.5 μV (RMS).*

I. INTRODUCTION.

The use of VLSI techniques in biomedical instrumentation opened the doors towards the miniaturization and portability of such systems. The portability gives among other benefits, more freedom of movements to the patient (of particular importance in long duration exams) and allows the of very small leads between the electrodes and the input amplifiers [1]. This last point is of great importance as this systems are usually used in noisy environments, while the signals to acquire have very low levels (down to few μV). But portability requires very low-power consumption to guaranty long life to the battery, what in turn creates constraints in circuits performance difficult to overcome.

In this paper a monolithic implementation of an analog front-end of a portable EEG acquisition system is presented. Besides low-power, the key design points are high Common Mode Rejection Ratio (CMRR) and very low noise. Minimum component count is also important to reduce systems weight and volume.

The system includes 16 instrumentation amplifiers, one 16:1 analog multiplexer, one programmable gain amplifier, auto-calibration circuitry for nulling mismatches among the 16 channels (including a test signal oscillator), a microprocessor compatible digital interface and an internal current/voltage reference source as shown in the block diagram of Fig. 1. It was implemented in the low-cost MIETEC 2.4 μV double-poly/double-metal CMOS technology opening good perspectives for a complete system integration, if an ADC and telemetry circuitry is added.

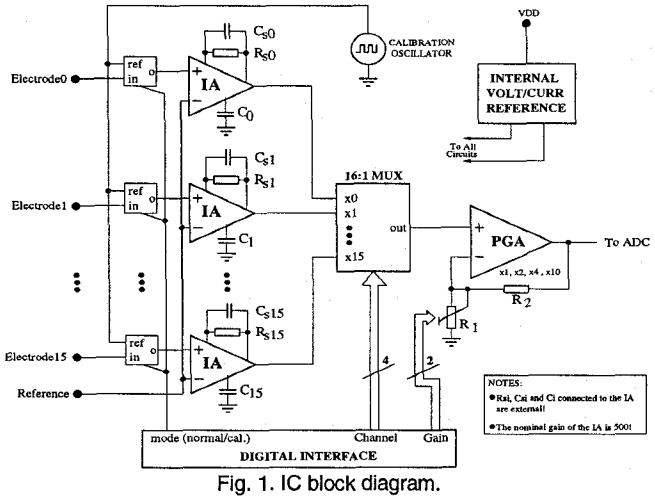

Fig. 1. IC block diagram.

II. INSTRUMENTATION AMPLIFIERS

In an acquisition system the overall performance is strongly dependent on the quality of its input IAs. They are the most critical elements in the integrated circuit described here and therefore the component to which more attention was given.

CMOS is unquestionably the best technology for micropower circuits [2]. However, among other problems associated with it, the CMRR behavior is worse than their bipolar and JFET counterparts. As EEG signals exhibit low frequencies (0.3 - 150 Hz) [3], the flicker noise becomes another potential problem as this technology exhibits higher flicker noise levels. Since we are not interested in circuits using sampling techniques [4], only a careful full-custom design can overcome such difficulties.

A. Current Feedback Instrumentation Amplifiers

Conventional resistive feedback differential amplifiers (where the classical three opamp structure is included) are not suitable when low-power, low-cost and high CMRR are simultaneously required. They need opamps with low output impedance to drive the feedback resistors, which implies high currents and large power

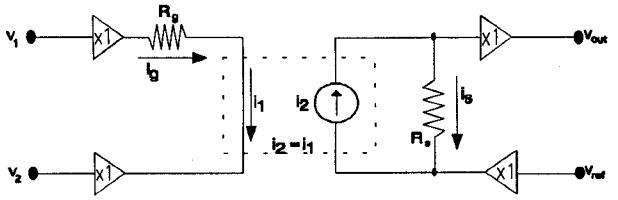

Fig. 2. Block diagram of an AI with current feedback.

drain. They need also precisely matched resistors to achieve high CMRR. This matching usually requires laser trimmed resistors, an expensive technique not available in a standard CMOS technology. One way to overcome these problems is the use of current feedback amplifiers [5]-[9], whose basic functional block diagram is presented in Fig. 2. Analyzing the input branch of this figure, we conclude that a high input impedance is guaranteed by two unit gain buffers and the current in resistor R_G is

$$i_g = \frac{1}{R_s} \cdot (v_1 - v_2) \tag{1}$$

whereas the output voltage equals

$$v_{out} = R_s \cdot i_s + v_{ref} \tag{2}$$

The input and output circuits behave, respectively, as transconductance amplifier and a transresistance amplifier. If the current in the input branch is mirrored into the output one ($i_1 = i_g = i_2 = i_s$) we obtain

$$v_{out} = \frac{R_s}{R_g} \cdot (v_1 - v_2) + v_{ref} \tag{3}$$

the usual relation for an instrumentation amplifier. But it is important to refer, that contrary to the classical 3 opamps configuration, there is no global feedback (from the output to the input) and that there is only one high impedance node, which simplifies the frequency compensation. Another advantage is that the CMRR (and the gain as well) do not depend on any matching of resistor values. The resistor count is also reduced saving chip area.

B. Implementation Issues

There are different possibilities to design a current feedback IA. Most of the reported ones are in bipolar technology [5]-[7] and [8] used CMOS. We implemented a CMOS variation of [6], as with this configuration only a reduced number of stacked transistors is necessary (improving dc behavior at low voltage power supplies) and solely 2 transistors at input are needed (optimal for noise reasons). Also, as PMOS transistors exhibit low flicker noise for the same area, we chose them to the input as shown in Fig. 3.

The circuit with no signal applied is fully balanced, so all

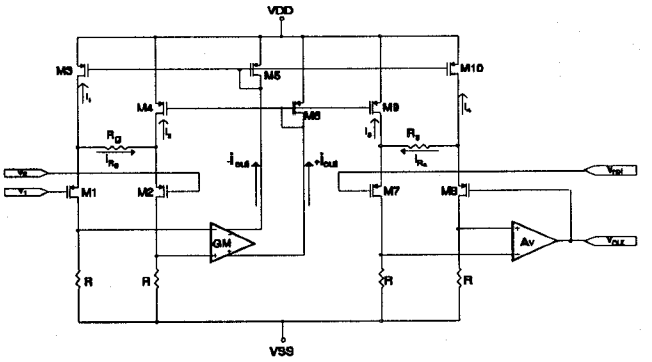

Fig. 3. Simplified IA circuit.

currents are equal and $v_{out} = 0$. When a differential signal is applied, the output currents of the transconductance amplifier GM become unbalanced in order to maintain the drain currents of M1 and M2 equal. In this situation, if both transistors are well matched their gate-source voltages are approximately equal and

$$i_{Rg} = \frac{v_1 - v_2}{R_g}$$

We can say that M1 and M2 linearized by GM replace the input buffers —▷— of Fig. 2. The transistors M7 and M8 linearized by the voltage amplifier Av working in a complementary (but similar) way, convert an input current into a voltage according to

$$i_{Rs} = \frac{(v_{out} - v_{ref})}{R_s}$$

Since the output current of the input circuit is mirrored by M6-M9 and M5-M10 the output/input relation becomes exactly equal to (3).

With the aim to reduce noise to the minimum, the IA also incorporates circuitry to make it a bandpass filter (0.3-150 Hz). For the low-pass filter, a capacitor C_S is connected in parallel with R_S, which causes a pole at

$$f_H = \frac{1}{2\pi \cdot R_s \cdot C_s}$$

The hi-pass filter action is more difficult to implement. The use of a passive RC filter is not a good solution for such a low cut-off frequency (0.3 Hz), so it was implemented using another feedback loop around the output circuit, as shown in Fig. 4. GM_{filter} acts as a resistor, but offers two advantages over a real one: First, as it is possible to make its transcondutance low, a high equivalent resistor can be obtained (>1MΩ). Second, there is no resistive loading of the output. The zero is at frequency

$$f_L = GM_{filter} / (2\pi \cdot C_{filter})$$

To improve the CMRR and also for low-power consumption the input transistors were made to work almost in moderate inversion [2]. For a good matching of

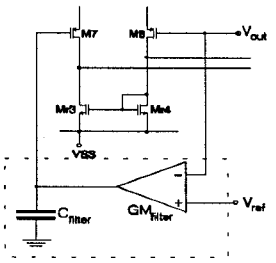

Fig. 4. Feedback loop realizing the hi-pass filter function.

these devices both W and L are quite bigger than the minimum feature dimension of the technology used. Furthermore, the layout was done carefully - the input transistors have common centroid structures, and all interconnections were made symmetric.

Load transistors Mr1 - Mr4 are usually designed according to the rule of thumb which states its transcondutance should be three times lower than the one of the input transistors so that these dominate the noise and offset performance. For thermal noise it is correct, but unfortunately this transcondutance ratio is insufficient when considering flicker noise and in case the input transistors are PMOS (note the load transistors are NMOS). For flicker noise, the parameter Y_F - *noise excess factor* [10] - that normalizes the total equivalent input noise density to the equivalent input noise density of only one of the input transistors is:

$$Y_F = \left.\frac{v_{n_i}^2}{v_{n_{M1}}^2}\right|_{FLICKER} = 2\left[1+\frac{Kf_N}{Kf_P}\cdot\left(\frac{g_{m_{Mr1}}}{g_{m_{M1}}}\right)^2\cdot\frac{(W\cdot L)_{M1}}{(W\cdot L)_{Mr1}}\right]$$

where Kf[11] is the flicker noise coefficient. An equivalent rule must then be:

$$\frac{g_{m_{M1}}}{g_{m_{Mr1}}} > 3\sqrt{\frac{Kf_N}{Kf_P}\cdot\frac{(W\cdot L)_{M1}}{(W\cdot L)_{Mr1}}} \qquad (4)$$

The condition (4), however is difficult to be verified if we do not want to waste a lot of area in Mr1. Our option was to make Y_F=4 (the input and load transistors generate the same noise). To obtain an integrated noise in the referred bandwidth less than 1.2 μV (RMS), we end up with relatively large transistors: $(W/L)_{M1}$= (600/25) and $(W/L)_{Mr1}$= (24/200) - all dimensions are in μm.

One reason why current feedback IA are frequently implemented in bipolar technology is the low transcondutance gain of these devices. It is important to guarantee sufficient loop gain in the input and output circuits to make a good linearization of M1, M2 and M7, M8. For the input circuit the relative error in the gain (the ideal transcondutance gain is $1/R_g$) as function of the transcondutance of the block GM is shown in Fig. 5 (simulation).

For the output circuit we present the relative error as

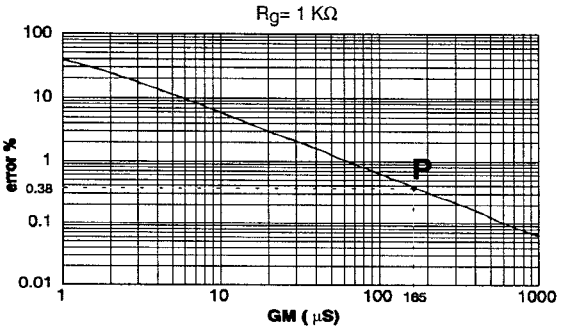

Fig.5 Transcondutance error (ideal gain is $1/R_g$).

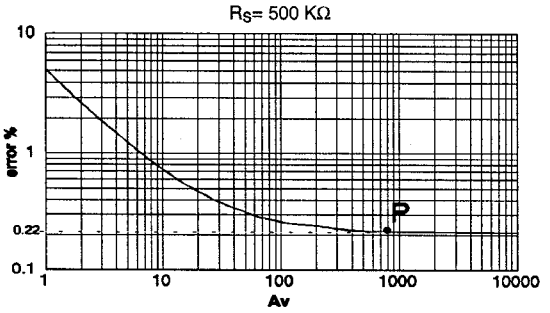

Fig.6 Transresistance error (ideal gain is R_f).

function of the voltage gain in Av (with the ideal transresistence gain being equal to R_S) in Fig. 6. In this, as well as in Fig. 5, the point P represents the chosen value, which corresponds to a total error of 0.6%.

As we have to deal with two separate amplifiers the stability problems are somewhat relaxed. In the input circuit no special circuitry is necessary. At the output circuit a compensation capacitor C_C, must be added to assure stability, because the loop gain is relatively high. This is done inside the block Av of Fig. 3. The complete circuit of the instrumentation amplifier is shown in Fig. 7.

III. OTHER COMPONENTS

A. Programmable Gain Amplifier

The IA has a fixed gain of 500. Then we have an amplifier with a programmable gain of 1, 2, 4 or 10. This amplifier is also used as buffer with low output impedance. As the signal level at its input is already high, there are no problems related to noise and precision as in the AI. We decided to use a simple configuration in which the most important design criteria was the low power consumption. Therefore, we designed a classical two stage opamp with a Miller compensation scheme and a class AB output stage as presented in Fig. 7. The AB class output stage allows to source/sink high currents while the biasing current is low. It is in a non-inverting configuration and the gain is modified switching the resistor R1 (see Fig. 1).

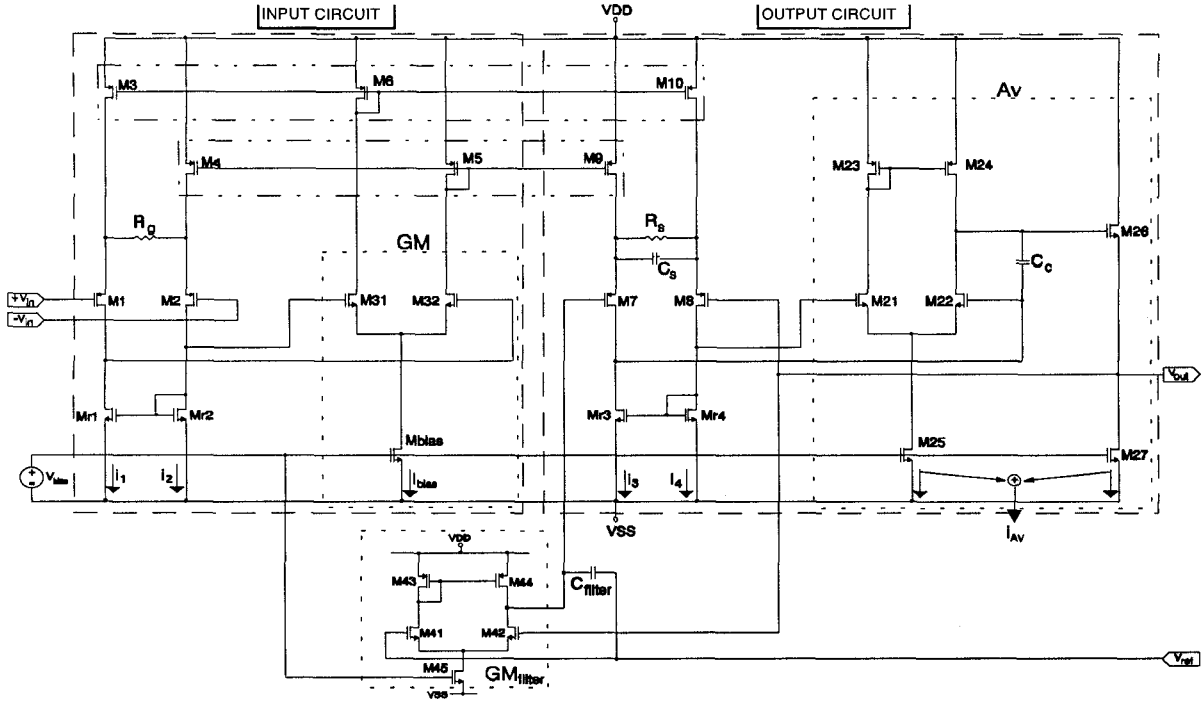

Fig. 7. Instrumentation amplifier (complete schematic).

B. Auto-Calibration Signal Oscillator

There are always some gain mismatches among the 16 channels. This effect is easily corrected by software if a common signal is injected in all channels and used as reference to determine all gains relative to one given channel. In EEG systems the usual test signal is a square-wave with 10 Hz and amplitude of 50 μV.

We designed a relaxation oscillator with output levels not dependent on the power supply, whose schematic is presented in Fig. 14. Transistors M1-M10 form a comparator with histeresis [12] and the integration is performed by the capacitor C_{ext} over a current independent of the power supply value. Hence, if *S= W/L,* the frequency is also stabilized and is given by

$$f_{osc} = \frac{I_{bias}}{4 \cdot C \cdot \sqrt{\frac{2 \cdot I_{bias}}{K \cdot S_1 \cdot (S_3 + S_5)}} \cdot \left(\sqrt{S_5} - \sqrt{S_3}\right)}$$

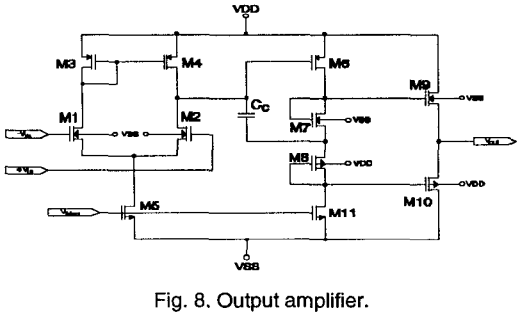

Fig. 8. Output amplifier.

To obtain a stable level for the test signal we switch a reference current (with M20 and M21) into the resistor.

C. Voltage/Current Internal References

As the voltage of a battery changes widely from a full-charge condition to the empty level, we integrated a stabilized current and voltage sources, We use a bootstrap type [12] with a start circuit as in Fig. 10 which always forces the stable operating point N.

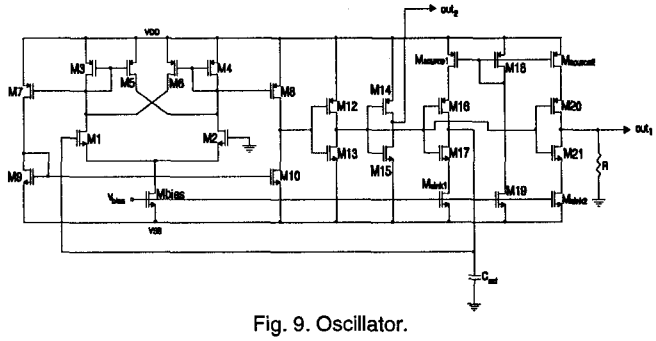

Fig. 9. Oscillator.

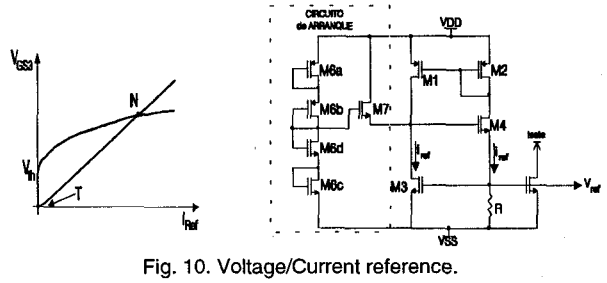

Fig. 10. Voltage/Current reference.

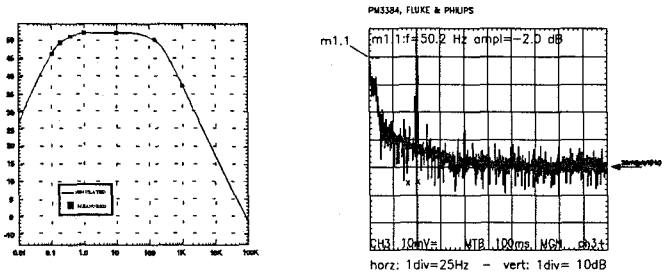

Fig. 11. Inst. Amplifier: Left - Frequency response; Right - Noise

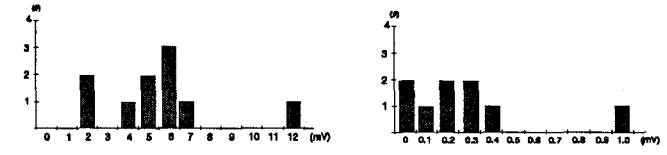

Fig. 12. Inst. Amplifier: Left - Inp. voltage offset (hi-pass filter disabled) Right - Voltage offset at output (with hi-pass filter).

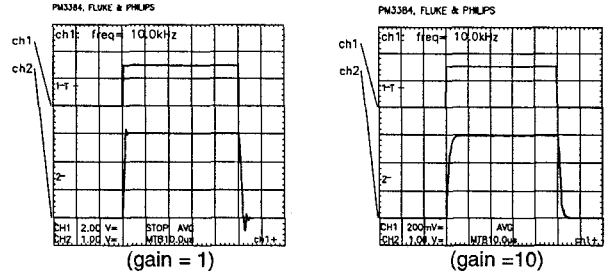

Fig. 13. Output amp: Transient Resp. (C_L=4.7pF) Ch1: V_{in} ; Ch2: V_{out}.

IV. MEASURED DATA

From Fig. 11 to Fig. 15 we show the measured data on prototype samples. All circuits functioned properly and inside the target values. Other important parameters are presented in Table I.

TABLE I

MEASURED RESULTS

PARAMETER	value	Note
Active area	24 mm^2	
Power supply	±4.5 V	
Total current	520 µA	typical
Maximal error in gain	0.9 %	Any gain
Total noise (inp. Ref.)	1.4 µV (RS)	0.3 < BW< 150 Hz
CMRR	99 dB	typical (50 Hz)
Offset (input)	0.29 mV	typical (hi-filter disabled)
Offset (output)	5.7 mV	typical (hi-filter enabled)
PSRR	40 dB	typical (low-freq)

V. CONCLUSION

We presented a monolithic analog front-end in a standard CMOS technology drawing 0.5 mA from a standard 9 V battery. So as to obtain high CMRR and low noise we designed an instrumentation amplifier based in current feedback techniques with specifications suitable for EEG acquisition systems, namely a CMRR of 100 dB and a total input equivalent noise of only 1.4 µV.

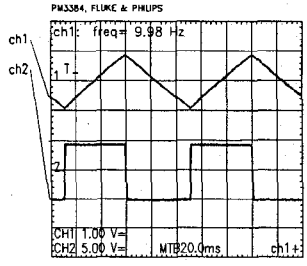

Fig. 14. Oscillator - Ch1: Signal at capacitor ; Ch2: Output signal V_{out2}

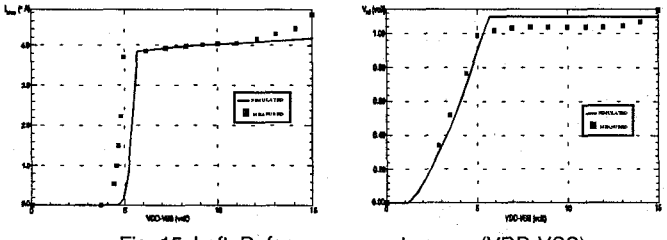

Fig. 15. Left: Reference current versus (VDD-VSS). Right: Reference voltage versus (VDD-VSS).

ACKNOWLEDGMENT

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