Influence of T-Gate Shape and Footprint Length on PHEMT High Frequency Performance

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Abstract - Combined hydrodynamic/drift-diffusion simulations of GaAs-based pseudomorphic high electron mobility transistors (PHEMTs) are presented. They do not only take into account the structure of the intrinsic transistor but also model the complex geometries of contacts and dielectric passivation in a realistic manner. Special care was taken to implement a general scheme for the T-gate cross section that allows to model gate profiles realized with electron beam lithography as well as with spacer processes based on optical lithography. Measured dc and RF data of two different PHEMTs (gate lengths 220 and 500 nm, respectively) manufactured on the same wafer with spacer technology are calculated very exactly. The simulator is then used to predict the effects of gate length reduction, modification of the T-gate profile and thinning of the passivation on device RF performance quantitatively. The specific problems of gate spacer processes applied to high frequency devices are identified, and the most effective process improvements are indicated.

I. INTRODUCTION

Pseudomorphic HEMTs are now becoming widely used in MMICs operating up to 100 GHz. In this frequency range, gate lengths L_G far below a quarter micron are necessary. Simultaneously, a small gate resistance must be realized. This is commonly achieved by the introduction of mushroom or T-gates. Their fabrication can be either based on electron beam lithography (EBL) with multiple resist layers or on optical waver stepper lithography combined with sidewall spacers [1]. For large volume production, optical lithography is preferred over EBL for cost reasons [2]. In both cases, the gate cross section depends in a sensitive way on the details of the process. The shape of the T-gate, the footprint length L_G as well as the thickness of the passivation all have a major impact on the gate capacitance C_G which is a key parameter for the RF performance of the device. If the influence of changes in the surface topology on C_G is known quantitatively, the effort of technological development is minimized. Up to now, most of the attempts to identify different contributions to C_G have been carried out for MESFETs. Basically, the results also apply for PHEMTs. The contributions that originate in the material layers below the device surface have been analyzed quite in detail [3] whereas few investigations of the parts of C_G originating from outside the semiconductor exist. These are either only valid for a specific contact geometry [4, 5] or restricted to qualitative discussion [6]. In this paper, we present device simulations carried out with the simulator MINIMOS-NT [7]. Power PHEMTs are realistically modeled including the geometry of double recess, T-gate, ohmic contacts and passivation layers. The implemented gate geometry is such that the gate profiles typically realized with EBL or spacer technology can both be modeled realistically. The results can be directly applied to identify which process improvements are expected to have the largest impact on device performance.

II. SIMULATIONS AND MEASUREMENTS

The PHEMT cross section used in the simulations is shown schematically in Fig. 1. It includes the complete epitaxial structure, the T-gate, double recess, and passivation layers with two different dielectric constants ε_{r1} and ε_{r2}. In order to quantify the geometrical shape of the gate, it is described by

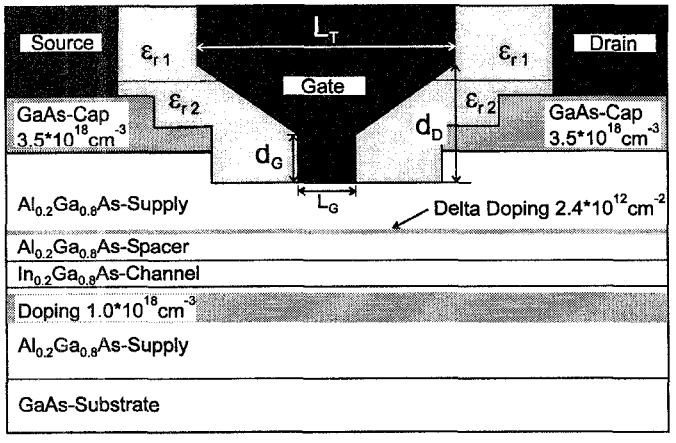

Fig. 1. Schematic cross section of the simulated PHEMTs.

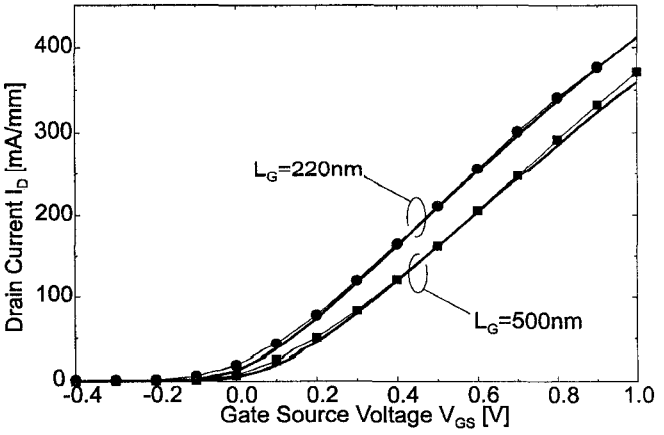

Fig. 2. Simulated (bold line without symbols) and measured (line with symbols) transfer characteristic for V_{DS} = 2.0 V.

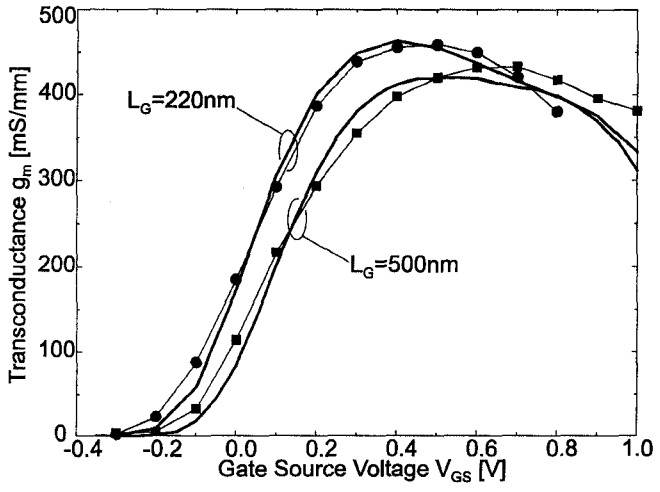

Fig. 3. Simulated (bold line) and measured (line with symbols) transconductance g_m at V_{DS} = 2.0V.

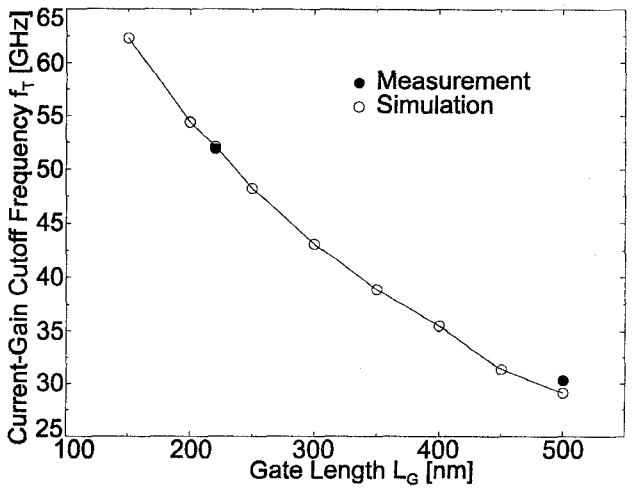

Fig. 4. Simulated and measured current-gain cutoff frequency f_T at V_{DS} = 2.0 V, I_D = 160 mA/mm.

the two characteristic dimensions d_G (at the footprint) and d_D (at the drain side of the structure), both shown in Fig. 1.

GaAs-based AlGaAs/InGaAs/AlGaAs power PHEMTs were manufactured on the same wafer with two different gate lengths L_G of 220 nm and 500 nm, respectively. Measurements and simulations of the transfer characteristics and the extrinsic transconductance g_m of these two PHEMTs are compared in Figs. 2 and 3. The simulations of the two PHEMTs were performed with one consistent set of physical and geometrical parameters with the exception of the different lateral dimensions. In both cases, d_G = 0, d_D = 200 nm, and $L_T = L_G$ + 600 nm. This means that a T-gate stem is practically non-existent, and the gate has a rather V-shaped profile. As depicted in Figs. 2 and 3, simulations and measurements agree very well.

The results discussed so far are dc properties and, thus sensitive to the gate footprint length L_G but not particularly to the shape of the T-gate. However, this shape influences the total gate capacitance C_G and the RF performance. In the simulations, C_G is determined by the quasi static expression

$$C_G(V_{GS},V_{DS}) = \left.\frac{\partial Q_G(V_{GS},V_{DS})}{\partial V_{GS}}\right|_{V_{DS}} \quad (1)$$

where Q_G is the total charge on the gate contact. The current-gain cutoff frequency f_T is then calculated by the approximation $f_T = g_m/(2\pi C_G)$.

When RF measurements are performed, contact to the PHEMT is made by means of microstrip lines and contact pads. These represent parasitic elements which are not included in the simulations. To make comparison of measured and simulated f_T's possible, the method described in [8] was adopted. The contribution of microstrips and pads to the total capacitance was determined by measurements of PHEMTs with different gate widths of 80, 180, and 360 µm. The measured f_T's were corrected by the result of the deembedding procedure. A comparison of the simulated f_T's with the measurements for the two experimentally examined values of L_G is shown in Fig. 4. The excellent agreement of both dc and RF simulations with the experiment gives confidence that the simulator cannot only reproduce the properties of existing devices but also will be able to make reliable predictions for process variations not yet realized.

III. CONTRIBUTIONS TO THE GATE CAPACITANCE

A. *Dependence of C_G on gate length*

In order to identify the different contributions to C_G, we minimize the capacitive coupling of the gate metal to the ohmic contacts and to the semiconductor material by setting $\varepsilon_{r1} = \varepsilon_{r2} = \varepsilon_r = 1$ (no passivation at all). The opposite extreme is represented by the case $\varepsilon_r = 7$ (space between contacts completely filled with dielectrics). Fig. 5 shows the simulated C_G as a function of L_G for both cases. As expected, C_G depends linearly on L_G (as well as on ε_r; not demonstrated in the figure). Thus, C_G can be described by the expression

$$C_G = A_1 + \varepsilon_r \cdot A_2 + L_G \cdot A_3 . \quad (2)$$

By extrapolation of the straight line for $\varepsilon_r = 1$ to $L_G = 0$, the fringe capacitance $C_F = A_1 + A_2$ is obtained. In Fig. 5, $C_F \approx 200$ fF/mm. Because the two-dimensional gate cross section is fully taken into account, this value is higher than the one given by Wasserstrom and McKenna [9] who use infinitely thin contacts in their model. From the separation of the two straight lines in Fig. 5, A_2 can be deduced. This contribution is determined by the device cross section above the semiconductor surface. In our case, $A_2 \approx 85$ fF/mm. Finally, A_3 is given by the slope of the two lines. Apart from some influences of minor importance (like lateral spacing of the three contacts), this quantity is dominated by the sheet charge under the gate. In our example, A_3 = 3.2 nF/mm^2 (for a gate with L_G = 100 nm, this is equivalent to 320 fF/mm). This last term in (2) is the only one necessary for the function of the transistor, the other two only diminish its performance.

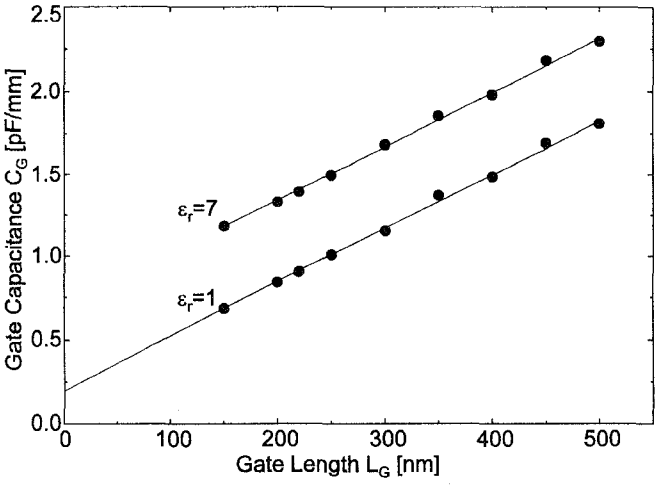

Fig. 5. Simulated gate capacitance C_G vs. gate length L_G for two different ε_r at V_{DS} = 2.0 V, I_D = 160 mA/mm.

B. Dependence of C_G on passivation

As already mentioned, the second term in (2) depends linearly on ε_r. Unfortunately, there exist no suitable passivation materials with ε_r significantly smaller than 7. A way to reduce the average ε_r in the space between semiconductor surface and contacts is to decrease the thickness of the dielectric coating such that this space is partially filled with air. This was done experimentally in [10] by selectively etching away part of the passivation. The change in C_G strongly depends on the electric field E in the space where the passivation is removed, (i. e., ε_r is changed from 7 to 1). Fig. 6 shows the spatial distribution of E in case of the PHEMT with L_G = 220 nm at a bias V_{DS} = 2.0 V, V_{GS} = 0.4 V. The highest field is at the drain-sided end of the gate footprint and decreases strongly towards the top of the gate contact. Therefore, only a moderate decrease of C_G is expected when only the top part of the passivation is removed.

This is quantitatively shown in Fig. 7. Simulations were performed for partially removed passivation, i. e. ε_{r2} = 7 and ε_{r1} = 1, where the interface between both regions is horizontal as indicated in Fig. 1. The capacitance C_G is reduced by about 120 fF/mm when the passivation is thinned to a residual thickness of 100 nm (passivation surface on a level with cap surface). The same decrease of C_G would be obtained by a reduction of L_G of about 40 nm, as can be deduced from Fig. 5. An even larger reduction of about 500 fF/mm is calculated for complete omission of the dielectric layer (case ε_r = 1 in Fig. 5). For comparison, the term $L_G A_3$ in (2) has a magnitude of about 700 fF/mm for the PHEMT with L_G = 220 nm.

Among the various capacitances that characterize a transistor, we have up to now only considered C_G and its influence on f_T. However, as a figure of merit for RF performance, the maximum frequency of oscillation f_{max} is of even more significance than f_T. Prerequisite for high f_{max} is a large ratio C_{GS}/C_{GD} where C_{GS} and C_{GD} are the gate-source

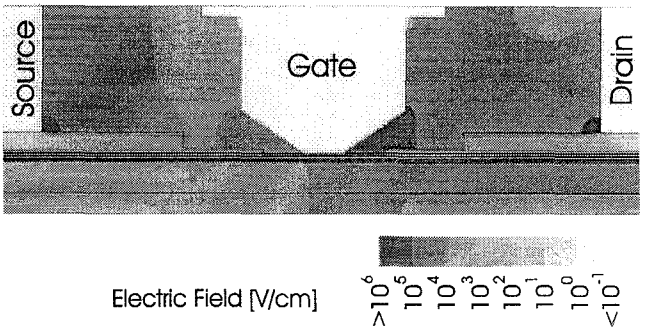

Fig. 6. Electric field of the simulated PHEMT in true scale at V_{DS} = 2.0 V, V_{GS} = 0.4 V.

and gate-drain capacitances, respectively. Analogous to (1), C_{GD} is obtained by

$$C_{GD}(V_{GS},V_{DS}) = \left.\frac{\partial Q_G(V_{GS},V_{DS})}{\partial V_{DS}}\right|_{V_{GS}} . \quad (3)$$

The gate-source capacitance is assumed to be given by $C_{GS} = C_G - C_{GD}$. In Fig. 7, the calculated quantities C_{GS}, C_{GD} and C_{GS}/C_{GD} are shown as a function of passivation thickness. With decreasing thickness, C_{GD} decreases proportionally more rapidly than C_{GS}, in our particular case especially for thicknesses below 200 nm. The ratio C_{GS}/C_{GD} accordingly rises dramatically. This result leads to two important conclusions: First, for high f_{max}, a thin passivation is very favorable, but, secondly, in this regime of small parasitic capacitances, C_{GS}/C_{GD} is subject to very rapid changes caused by very small process variations. Consequently, it is extremely difficult to achieve tight control over f_{max}, and hence the gain.

C. Dependence on T-gate cross section

To investigate the influence of the gate cross section, different gate geometries were simulated by varying the two characteristic dimensions d_G and d_D. All calculations were performed for L_G = 220 nm and L_T = 820 nm. One limiting case for the gate geometry is d_G = 0 (as shown in Fig. 6 and used for all simulations discussed up to here) whereas the other extreme is given by $d_G = d_D$ ("ideal" T-gate cross section). Fig. 8 presents simulations of C_G and f_T as a function of d_G for a completely passivated device with d_D as a parameter. The closed circle in Fig. 8 designates measurement and simulation of the particular PHEMT shown in Fig. 6. Here, a distinct T-gate stem is not existent (d_G = 0). According to Fig. 8, the f_T of this device could be increased from 53 GHz to a value close to 60 GHz if the gate cross section could be improved in a way that d_G changes from zero to 200 nm ($d_G = d_D$, ideal T-gate). Further increase of d_G and d_D would further improve f_T. Values about 65 GHz are expected for $d_G = d_D$ = 400 nm, without decreasing the gate length. In the case that still d_G = 0 and only d_D = 400 nm (gate stem sidewalls and device surface enclose an angle of 53°), again $f_T \approx$ 60 GHz is expected, comparable to the case $d_G = d_D$ = 200 nm.

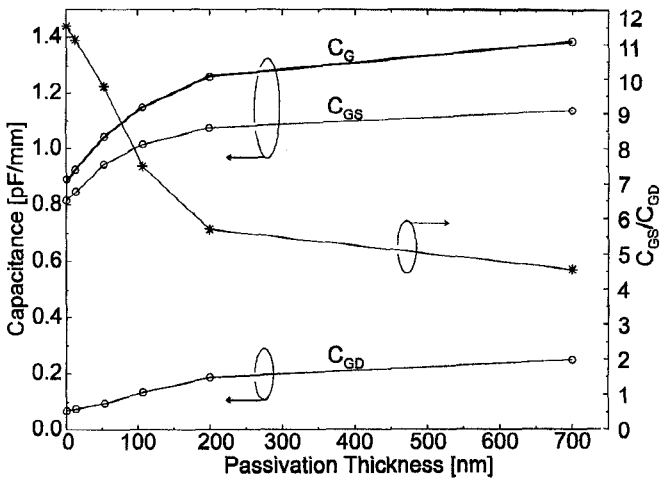

Fig. 7 Capacitances C_G, C_{GS}, C_{GD}, and the ratio C_{GS}/C_{GD} as a function of passivation thickness.

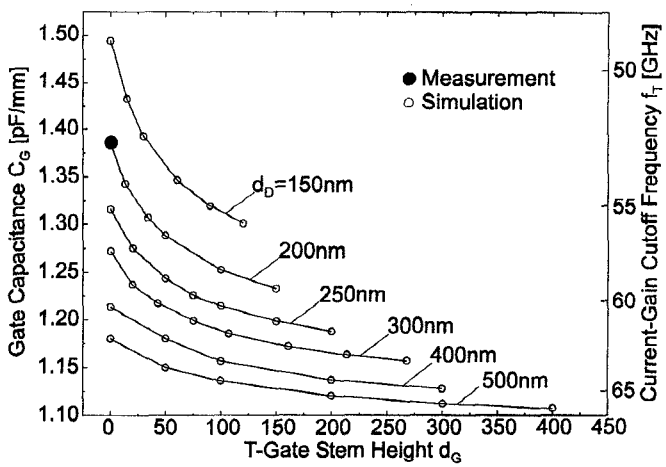

Fig. 8 Simulated gate capacitance C_G and current-gain cutoff frequency f_T for $L_G = 220$ nm and different gate cross sections ($V_{DS} = 2.0$ V, $V_{GS} = 0.4$ V). All calculations for $L_T = 800$ nm.

Thus, it is of immense importance that the process technology is able to realize a gate cross section where the gate stem sidewalls are really perpendicular to the semiconductor surface (ideal T-gate). If the enclosed angle is significantly smaller than 90° (V-shaped gate stem), d_D has to be substantially greater compared to the perpendicular case if the same f_T has to be realized. The multi-resist level approach of most EBL processes facilitates the fabrication of such vertical T-gate stems. Gate technologies that use optical lithography are usually based on narrowing the comparatively large resist openings by spacers. They often have the property not to result in really vertical sidewalls. If such a technology is used for the fabrication of devices for high-frequency application, it is important that at least the part of the gate immediately adjacent to the semiconductor surface has perpendicular sidewalls.

IV. CONCLUSION

We have discussed two-dimensional simulations which take fully account of the complex structure of a PHEMT, including all geometrical details of recess, T-gate, ohmic contacts and dielectric layers. We have quantitatively analyzed the different mechanisms that contribute to the gate capacitances. Therefore, we can make reliable predictions on the consequences of technological development, particularly for transistor RF performance. We are able to identify the process improvements which promise the comparatively largest progress. For instance, a decrease of the gate length might have significantly less impact on the cutoff frequencies f_T and f_{max} of a PHEMT than a careful optimization of the gate cross section in the region close to the semiconductor surface. This last issue is particularly important if optical lithography and spacer technology are used for the fabrication of short gates below a quarter micron, because this approach does not offer the easy modification of the gate cross section that can be achieved with EBL-based multi-level resist techniques. However, recent progress in spacer technology control has allowed to take full advantage of the insight provided by the simulations. This has resulted in the successful fabrication of state-of-the-art W-band MMICs with optical lithography, based on GaAs PHEMTs with $L_G = 120$ nm and $f_T = 120$ GHz [2].

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