Closed-Loop CMOS Gate Delay Time Optimization

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Abstract

We present a closed-loop CMOS gate delay time optimization procedure for low- power applications which emulates the behavior of an infinite inverter chain. This optimization procedure is applied to doping profile optimization of a 0.25 μm CMOS technology. The average gate delay time was improved by more than 50% compared to transistors with a uniformly doped channel region.

1. Introduction

Increasing speed and reducing standby power are the key challenges of the ever growing portable electronics market. Reducing the average gate delay of a CMOS inverter chain, as shown in Fig. 1, while keeping the leakage current low means increasing the speed of the whole technology without changing the standby power.

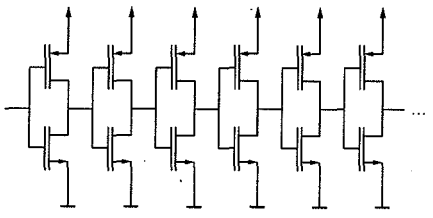

Figure 1. Infinite CMOS inverter chain

Usually, the device geometry and the supply voltage are fixed for a given technology, therefore the key challenge lies in an optimized doping profile which will be the scope of this work.

2. Optimization Procedure

In order to evaluate the average gate delay time of an infinite inverter chain, an adequate model for one single stage has to be found (Fig. 2). It consists of a CMOS inverter and a capacitive load C_L connected to the output which accounts for the gate capacitance of the following stage. Since this capacitance changes during transition, it is assumed to be voltage dependent. It can be calculated using the input current information of the succeeding stage.

$$C_L(V) = \left.\frac{I_{in}(t)}{dV_{in}(t)/dt}\right|_{V_{in}(t)=V} \quad (1)$$

An optimizer drives the closed-loop optimization procedure [1]. The optimization target which will be minimized during optimization, is defined as the average inverter delay time for the on- and off-transitions:

$$\text{target} = \frac{(t_{d,on} + t_{d,off})}{2} \quad (2)$$

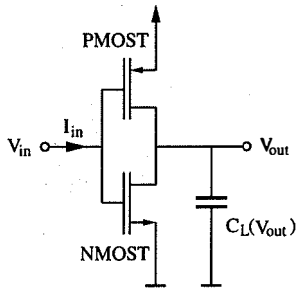

Figure 2. Single stage inverter model

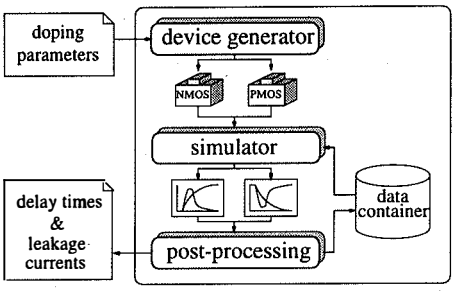

Figure 3. Delay and leakage model

The optimization constraint which is kept above zero, guarantees that the average leakage current stays below 1 pA:

$$\text{constr.} = -\log\left(\frac{(I_{\text{l,on}} + I_{\text{l,off}})/2}{1\ \text{pA}}\right) \quad (3)$$

The model for the inverter delay times and the static leakage currents is shown in Fig. 3. After reading a given set of doping parameters, the device description of the NMOS and PMOS transistors are produced. Then the inverter model depicted in Fig. 2 is evaluated by transient simulations for both the on- and off-transitions. Additional input data for the simulator, besides the device descriptions, are the input V(t) curves and the C(V) curves of the capacitive load C_L which are taken from a data container. Using the resulting output V(t) and input I(t) curves of the inverter, the delay times and leakage currents are calculated. The processed input V(t) and C(V) curves for following model evaluations are stored in the data container.

Fig. 4 shows the optimization sequence of this procedure. Any time a temporary minimum is found after a number of evaluation steps, a gradients calculation is launched to find the Jacobian matrix for the optimization parameters, and then the next temporary minimum is searched. After each temporary minimum step, the output curves are stored in a wait-state and will be transferred into the data container after the gradients calculation is finished. This permanent update of the data container provides a self-contained emulation of an infinite inverter chain, since output voltage curves and input currents will be used for input curves and load capacitance evaluations for the next steps, repeatedly.

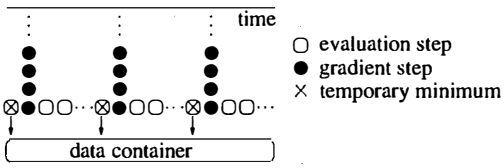

Figure 4. Optimization sequence

3. Doping Profile Optimization

The optimization procedure was performed on MOSFETs with 0.25 μm gate length, 1 μm gate width, and 5 nm gate oxide thickness for 1.5 V supply voltage. The source/drain doping profiles stayed fixed during optimization with a maximum doping of 10^{20} cm^{-3} and about 50 nm junction depth.

Two different methods were used to obtain a set of optimization parameters which define the doping profiles in the active regions of the two transistors: A general two-dimensional approach using an optimization grid, and an approach with implanta-

tion models. The simulator MINIMOS-NT [2] was used for all simulation tasks since it supports the coupling between circuit simulation with compact models and numerical device simulations consistently.

3.1. Two-Dimensional

An optimization grid was chosen with the shape of an inverted "T" to cover all regions which might influence the device behavior. Fig. 5 shows the optimization grid and the source/drain wells. The doping at each grid point is defined by one optimization parameter, therefore 124 parameters, 62 for each device, are required. Between the grid points, an interpolation method was used to provide a smooth two-dimensional doping profile. Outside the optimization region the substrate doping was kept at 10^{15} cm^{-3}.

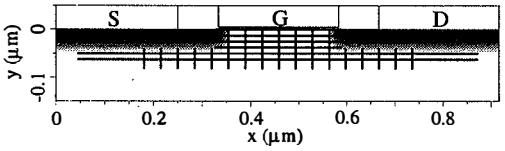

Figure 5. Optimization grid and S/D wells

Fig. 6 shows the resulting doping profiles. The average gate delay time was reduced by 58%, from 82.1 ps to 34.8 ps compared to the initial device with a uniformly doped "inverted-T" region.

3.2. Implantation Models

The use of Gaussian implantation models allows for a considerable reduction of the number of doping parameters and, therefore, for a faster optimization procedure. Additionally, the results from the two-dimensional approach, which look quite complex due to the numeric origin of the optimization procedure, can be tailored to more realistic profiles.

Three implantations were used for the channel region. The first one is located in

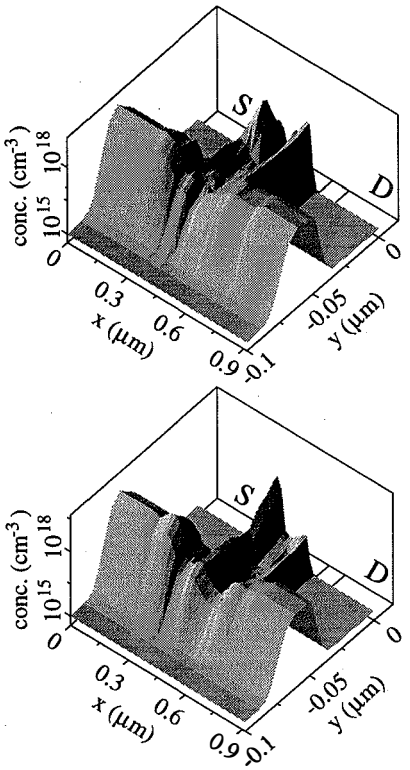

Figure 6. Two-dimensional optimization results, top: NMOST, bottom: PMOST

the channel close to the source well. It sets the threshold voltage of the device and reduces the effective gate length. The second and third implants are located deeper, under the source and drain wells, respectively. They improve the short channel effects and work as a shield against deep punchthrough. Fig. 7 shows the resulting doping profiles. The delay-time reduction with this method is still 55%.

4. Discussion

The optimized doping profiles are similar to the results obtained by previous work where only the drive current of a single NMOS transistor was optimized [3].

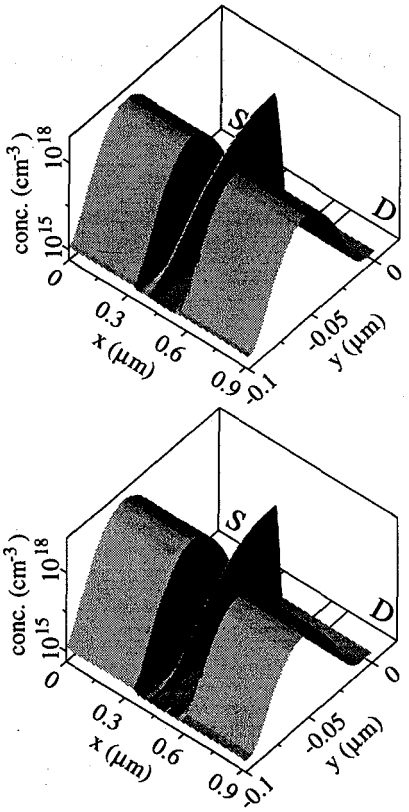

Figure 7. Implantation models optimization results, top: NMOST, bottom: PMOST

Now the regions under source/drain are of increased importance because of the source/drain well capacitances.

Fig. 8 shows the inverter input/output curves before and after optimization for both transition cases. For optimization, or rather simulation, reasons, the transition time point of the input curves, defined at 50% of the supply voltage, was kept constant. The delay time for the output-on transition is higher than for the output-off transition because the optimizer kept both leakage currents at about the same value of 1 pA. Therefore, the PMOS transistor delivers a lower drive current due to the lower majority carrier mobility.

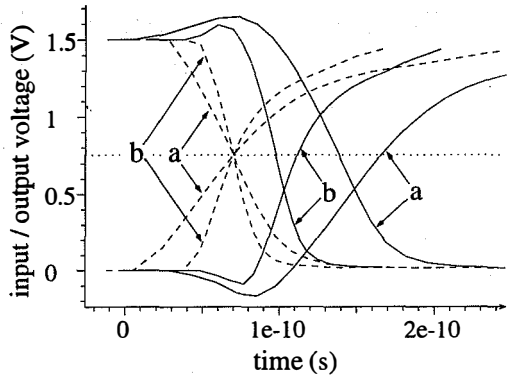

Figure 8. Input (dashed) and output (solid) curves before (a) and after (b) optimization

5. Conclusion

We presented a CMOS gate delay time optimization procedure which was applied to doping profile optimization of a 0.25 μm CMOS technology using two different approaches. The average gate delay time was improved by more than 50% compared to transistors with a uniformly doped channel region.

[1] R. Plasun, M. Stockinger, and S. Selberherr, "Integrated Optimization Capabilities in the VISTA Technology CAD Framework," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 17, no. 12, pp. 1244–1251, 1998.

[2] T. Grasser, V. Palankovski, G. Schrom, and S. Selberherr, "Hydrodynamic Mixed-Mode Simulation," in K. D. Meyer and S. Biesemans, eds., *Simulation of Semiconductor Processes and Devices*, pp. 247–250, Wien, New York: Springer, 1998.

[3] M. Stockinger, A. Wild, and S. Selberherr, "Closed-Loop MOSFET Doping Profile Optimization for Portable Systems," in *Proc. MSM Int. Conf. on Modeling and Simulation of Microsystems*, (San Juan, Puerto Rico, USA), Apr. 1999.