Closed-Loop MOSFET Doping Profile Optimization for Portable Systems

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ABSTRACT

We present a new closed-loop simulation-based optimization process for a 100 nm MOSFET for portable systems such as subscriber units for wireless communications, yielding an almost double drive performance at equivalent stand-by power when compared to conventional uniformly-doped structures. A discretization of the acceptor doping profile is performed to obtain a set of optimization parameters and a global optimization target is defined which, when minimized, maximizes the drive current while keeping the drain-source leakage current in the vicinity of 1 pA/μm. The optimized doping profile exhibits two regions which dominate the device performance. To obtain a simpler doping profile characterization a second optimization process is performed with two Gaussian implantation models. General device design guidelines are given featuring high drive- and low leakage current, building on the advantages of the asymmetric device structures.

Keywords: optimization, simulation, MOSFET, low-power, asymmetric channel doping

INTRODUCTION

In the past low-power applications became more and more important because of the increasing portable electronics market. A subscriber unit, for example, spends typically most of its time in stand-by, so that its leakage current must be kept below a specified value to maximize the battery lifetime. When a communication takes place, the unit must perform high speed computations, for example, it will de-compress the incoming signal and compress the outgoing signal. These system requirements are best satisfied by a MOSFET featuring a restricted drain-source leakage current when turned off and highest possible drive current when turned on.

For a given technology generation, the minimum feature size and the gate oxide thickness are implicitly defined. Various MOSFET structures have been recently reported with channel lengths down to the nanometer regime [1], but no general evaluation addressed the optimum doping profiles for a given application. This paper demonstrates that considerable performance improvements can be achieved by optimizing the doping profile.

OPTIMIZATION PROCESS

The optimization starts with a two-dimensional discretization of the acceptor doping of an n-MOSFET with 100 nm geometry gate length, 1 μm gate width, and 2.5 nm gate-oxide thickness as shown in Fig. 1.

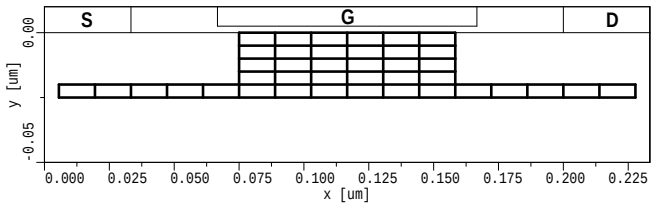

Figure 1: The "inverted T" acceptor-doping discretization

The length of the source and drain spacers is one third of the gate length, the source and drain junction depth is about 20 nm. The source and drain donor doping at the surface is 10^{20} cm^{-3}, the constant substrate acceptor doping is 10^{15} cm^{-3}. Fig. 2 shows the donor doping of the device which is kept invariable during the optimization.

In contrast to previous optimization experiments, in which only the channel region of a 0.25 μm MOSFET was considered [2], now the optimization region is extended under the source and drain, taking the form of an "inverted T" which allows for improved control over the short channel effects.

The acceptor doping concentration values in each of the 62 discretization points are treated as free optimization parameters ("doping parameters"). The effective acceptor doping in the "inverted T" region is obtained by superposition of 62 raised-cosine shaped doping fragments in the logarithmic domain. The background doping is kept at a constant, low value.

An optimizer drives the closed-loop optimization process [3] finding the doping parameters that maximize the drive current I_{on} ("goal") while keeping the leakage current I_{off} in the vicinity of 1 pA/μm ("constraint"). For optimization purposes the constraint is combined with the goal to receive a global optimization target which will be minimized during the optimization:

$$\mathrm{target}(I_{\mathrm{on}}, I_{\mathrm{off}}) = \mathrm{P}(I_{\mathrm{off}}) - I_{\mathrm{on}} \quad (1)$$

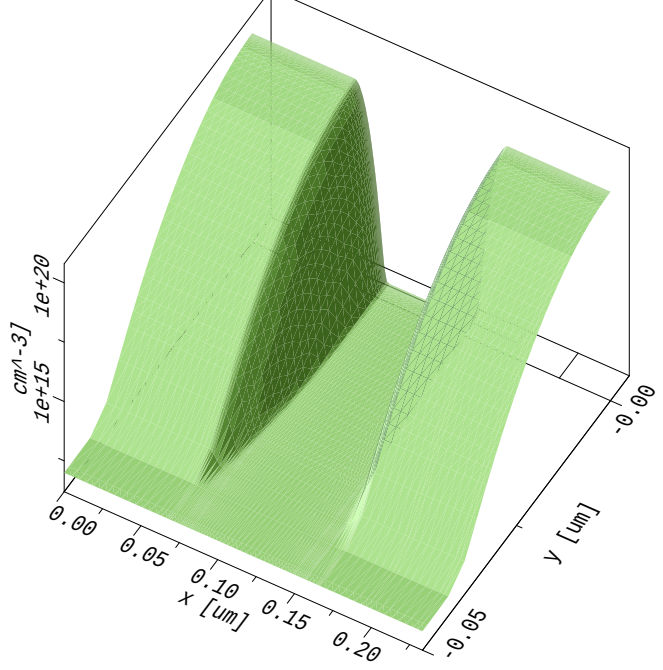

Figure 2: The invariable donor doping

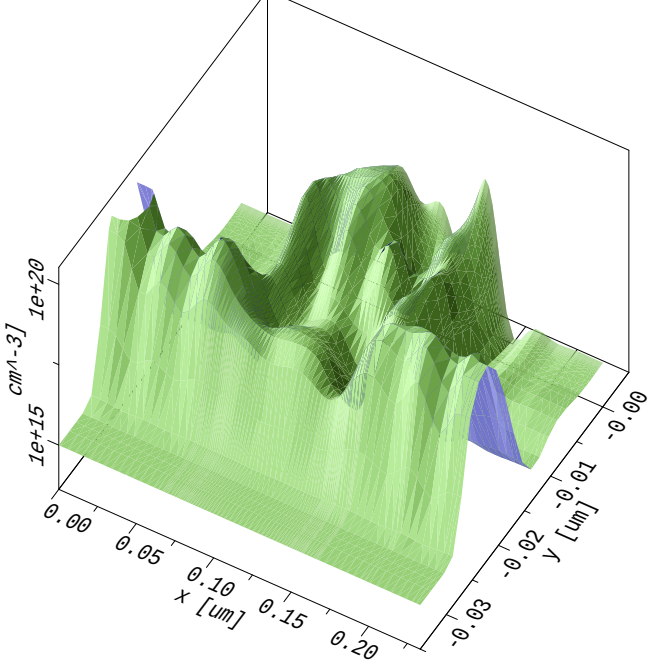

Figure 3: The optimized acceptor doping after optimization of the "inverted T" structure

where we make use of a half-parabolic penalty function:

$$\mathrm{P}(I_{\mathrm{off}}) = \begin{cases} 10^{19}\mathrm{A}^{-1} \cdot (I_{\mathrm{off}} - 1\mathrm{pA})^2 & : \; I_{\mathrm{off}} > 1\mathrm{pA} \\ 0 & : \; I_{\mathrm{off}} <= 1\mathrm{pA} \end{cases} \quad (2)$$

In each optimization step the numerical device simulator MINIMOS-NT [4] is launched with the refined device structure to determine the drive- and leakage current. The optimizer is fed with the results, and decides whether to continue the refinement of the structure or to stop the process since the optimum has been reached.

One optimization step is as follows:

- the optimizer requests an evaluation with a set of doping parameters
- the device description (geometry and doping) is produced by an analytical device generator using this parameter set
- device simulations to find I_{on} and I_{off} are carried out by the simulator
- the global optimization target is calculated and returned to the optimizer

The result of such an optimization run is presented in Fig. 3, about 7000 steps were necessary to find the optimum. For the initial device, all doping parameters were set to $5 \cdot 10^{18}$ cm^{-3}. The overall optimization time was reduced drastically by exploiting parallel simulation strategies with sophisticated load-balancing algorithms [5] and clever initialization of the device simulator using previous simulation results.

SENSITIVITY ANALYSIS

In order to find out which doping regions have a real impact on the result, a sensitivity analysis is carried out: The doping parameters are increased slightly, one at a time, and for each variation the drive and leakage current are determined. The relative variations with respect to the target are shown in Fig. 4. Two regions dominate the result: region 1, located in the channel, close to the surface, near the source, which sets the threshold voltage of the device, and region 2, located deeper, in front of the source curvature, which prevents the deep punchthrough. The remaining region has less influence on the device performance, therefore the doping in this region can be chosen more or less arbitrarily, provided that its value is low enough not to gain influence on the threshold voltage.

GAUSSIAN IMPLANTATION MODELS

The discrete doping parameters are replaced with a continuous model, using two adjustable Gaussian implantation models and the optimization is performed again. The new optimization parameters are the acceptor substrate doping, as well as the lateral and vertical position, the peak doping, and the lateral and vertical sigma values for both of the implantation models. As they are much less numerous than the discrete doping parameters, the overall runtime is drastically reduced.

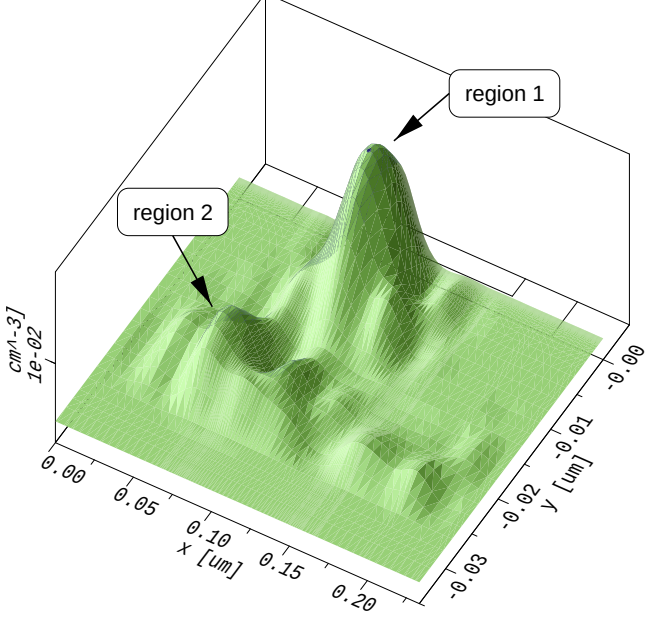

Figure 4: The relative sensitivity of the optimization target

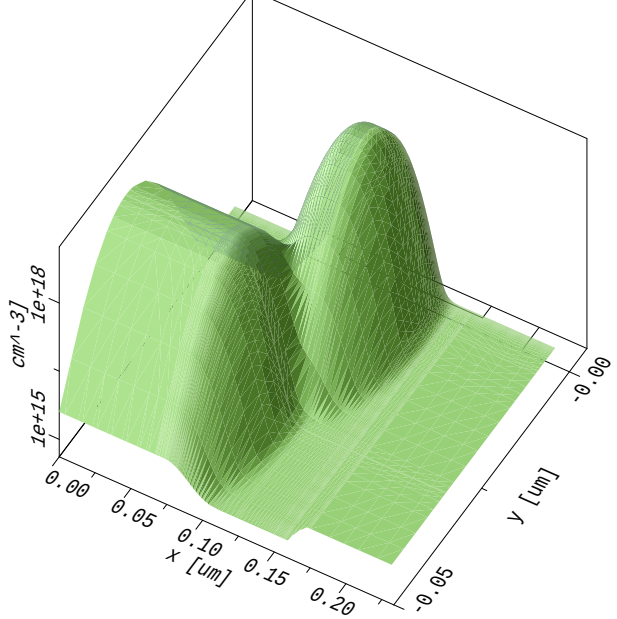

Figure 5: The optimized acceptor doping after optimization with two Gaussian implantation models

It is important to note that the resulting device structure (Fig. 5) features a clearly asymmetric channel doping. For the same leakage current, the optimization yields a drive current 82% higher than that of a uniformly-doped device. This performance improvement results from the reduction of the effective gate length as shown for a 0.25 μm device in [6]. Table 1 gives a comparison of the device performances, where a uniformly-doped device with an acceptor doping concentration of $2.388 \cdot 10^{18}$ cm^{-3} delivering the same I_{off} is used as the reference device.

Table 1: Comparison of the device performances

device	I_{off} (pA)	I_{on} (μA)	$I_{\text{on}}-$ improvement
uniformly doped	1.75	124.3	—
two-dimensional	1.70	231.5	86%
implantation model	1.76	226.7	82%

DISCUSSION

As a result of this optimization study, a few general device design guidelines can be given for MOSFETs featuring high drive- and low leakage current, building on the advantages of the asymmetric device structures. These guidelines can be formulated as follows:

- an asymmetrical channel doping should be employed with its maximum at the source side
- precautions have to be taken to prevent the device from deep punchthrough, this can be done using an implantation under the source
- the constant substrate doping should be low to achieve a steep subthreshold slope

Devices with a symmetric channel profile show an inferior performance, though pure vertical channel optimization can, in some cases, offer satisfying results (see, for example, [7], [8]).

Devices with a sub-surface doping layer for punchthrough shielding (delta doping, steep retrograde profile) suffer from a bad subthreshold slope due to the bulk-charge effect, but they offer superior short-channel effects [1], [9] which can be of major interest, in some cases.

Fig. 6 shows the transfer curves of the optimized device depicted in Fig. 5. Two different drain voltages were applied, 50 mV and 0.9 V, to show the device behavior in the linear and saturation region, respectively. The device has a steep subthreshold slope of 70 mV/decade due to the small constant substrate doping. The threshold voltage, though of no special concern in our work, is 0.34 V for the linear and 0.4 V for the saturated case, and is defined as the gate voltage for a drain-source current of 100 nA. The calculated DIBL (Drain Induced Barrier Lowering), defined as the decrease in threshold voltage for a drain-voltage increase of 1 V, is 70 mV

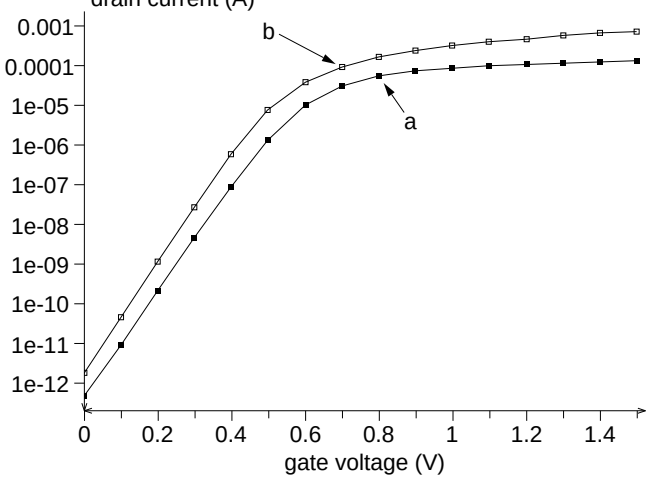

Figure 6: The transfer curves for (a) V_D=50 mV and (b) V_D=0.9 V

which is acceptable. One has to make a tradeoff between drive current and short-channel effects [1]. For this work the drive current has been the matter of interest.

CONCLUSION

We presented a new closed-loop simulation-based optimization process for the optimization of arbitrary device parameters and carried out a two-dimensional doping profile optimization for a low-power 100 nm n-MOSFET. The optimization result was investigated by performing a sensitivity analysis for the doping parameters. Two important regions showed up, one located in the channel, close to the surface, near the source, and the second located deeper, in front of the source curvature.

A second optimization was performed using two simple implantation models with Gaussian shape. The drive current was improved by more than 80% compared to a uniformly-doped device. General design guidelines for high drive currents and low leakage currents were presented, building on the advantages of the asymmetric device structures, evidencing the tradeoff between drive current and short-channel effects.

The presented optimization process is usable for a large variety of device types and optimization goals, as required by different systems and applications. A theoretical approach to the question "Which doping profile suits best for a desired performance goal?" was taken.

Additional performance metrics can be straightforwardly considered for optimization like junction capacitances, gate delay, or ring-oscillator time constant of an inverter stage. The implementation of such new goals into the optimization process means no effort in general, but much longer computation times have to be expected due to the required AC and/or transient simulations.

ACKNOWLEDGMENT

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