High-Precision Interconnect Analysis

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***Abstract*— Integrated circuits have evolved to a stage where interconnections significantly limit their performance and functional complexity. We introduce a set of tools to perform highly accurate three-dimensional capacitance and resistance/thermal calculations of interconnect structures. We automatically generate these structures from layout information and a given process description. The main enhancement of our work is that we extract the interconnect characteristics after a complete and accurate topography simulation with previous optional lithography analysis, instead of elementary geometric blocks derived from simple analytical models. The capacitance and resistance/thermal extractor simulators are based on optimized finite-element methods, and the topography simulators use a cellular data-based approach.**

***Index Terms*—Capacitance, resistance, three-dimensional simulation, topography.**

I. Introduction

THROUGHOUT the evolution of integrated circuits, the minimum feature sizes have been continuously reduced to increase their functional complexity and improve performance. This is accomplished mainly by improving the switching speed of digital circuits and extending the bandwidth of their analog counterparts. The scaling down of active devices played a major role in the achievement of these goals in the past, but the constraints in circuit speed and complexity are becoming increasingly governed by the interconnections between them. In addition, recent generations of application-specific integrated circuits include both digital and analog parts, which are very sensitive to cross talk, noise coupling, and other factors strongly dependent on routing. Thus, more attention toward modeling interconnections is required as we enter the deep-submicrometer regime.

Several software packages were reported to simulate capacitances and resistances in three dimensions. While the lateral dimensions of interconnect lines are being scaled down along with the devices, their thickness remains relatively constant, causing the fringing effects to be more severe. This makes fast procedures for estimating capacitances based on analytic models [1], [2] too inaccurate, as they cannot handle the fringe capacitances of complex structures in an appropriate manner and are difficult to generalize to every technology. Therefore, only numerical approaches can be used to fully and accurately characterize interconnect structures. Methods based on finite differences [3], [4], boundary elements [5], finite elements, [6]–[8], multipole algorithms [9], [10], and stochastic techniques [11] have been reported in literature to perform these quite complex tasks.

The applicability of three-dimensional interconnect simulators is, however, conditioned by the data needed as input to this software packages. The data formats change widely, and the input processes are usually extremely time consuming and error prone (e.g., geometry-based input formats entered manually), which restricts their use to simple problems (even if their solvers are powerful and in theory able to handle much larger problems). A better solution requires a general approach, one that provides an interface between mask layout and the fabrication process [12], [13]. The result should be a circuit-level electrical model, compatible with standard circuit simulators such as SPICE. In such a solution, the structures to be investigated are generated automatically, allowing electronic CAD (ECAD) designers to predict the interconnect behavior before any silicon is produced. This way, the conservative design rules of a conventional very-large-scale-integration circuit design, where the design and fabrication phases are uncorrelated, can be relaxed, resulting in more compact circuits with improved performance and functionality while keeping good yield capabilities. This raises the problem of linking ECAD and technology CAD (TCAD), the field of engineering that simulates the fabrication processes of integrated circuits, where we can find very accurate etching/deposition simulators to model interconnect structures. The techniques presented in [12] and [13] become inadequate, as they use too simple models to perform these process steps properly. This matter is becoming more acute, as the new processes use multilevel metallization steps, trench etching, and other methods that cause highly nonplanar topographies. Another drawback of those solutions is that they assume that the final structures follow the layout closely. However, as we enter in deep-submicrometer technologies, this is no longer true, and one must consider lithographic phenomena.

We present a set of layout-driven CAD tools that perform interconnect analysis, where the automatically created three-dimensional structures are derived from accurate topography simulation. The data flow is shown in Fig. 1.

Our tools present, in relation to the commercial ones that follow the same approach [14]–[16], models for reactive ion etching and sputter deposition, the possibility of a transient mode simulation (especially suitable for clock-delay problems), and a flexible solid modeler where it is easy to combine

Manuscript received March 2, 1998; revised June 20, 1998. This work was supported by FCT under program PRAXIS XXI, Portugal, by Austria Mikro Systeme International AG, Unterpremstätten, Austria, and by Christian Doppler Forschungsgesellschaft, Vienna, Austria. This paper was recommended by Associate Editor Z. Yu.

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Publisher Item Identifier S 0278-0070(98)08584-4.

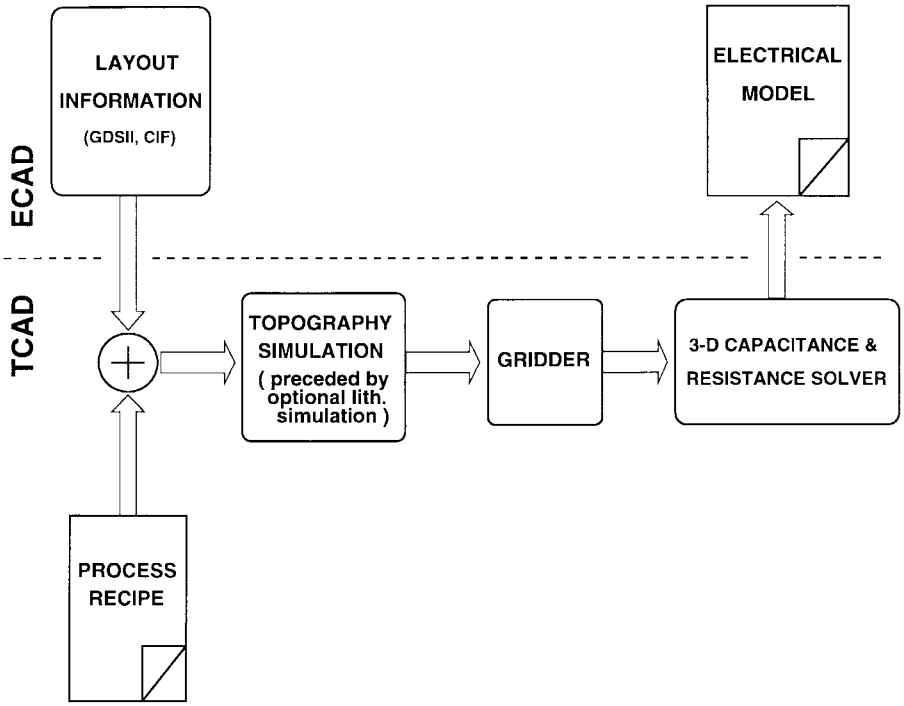


Fig. 1. Data flow and block diagram of proposed tools.

simple models for noncritical steps (e.g., a wire in Metal1 where the surface is sufficiently planar) with the results of a three-dimensional topography simulator. This reduces calculation time and computer resources while maintaining a high accuracy.

In the next section, we discuss issues concerning the layout data and the interface between ECAD and TCAD. We also refer to how lithography-related effects are incorporated in our simulation flow. In Section III, we present the topography simulators and enlighten the grid generation required by the next module. In Section IV, the capacitance and resistance/thermal simulators are described. In Section V, some representative examples are given.

II. Layout Specification

The layout of an integrated circuit or part of it specifies where in the wafer the action of one given process step is going to be made effective or masked out. As a consequence, it describes the locations on the wafer where the devices and their interconnections are going to be built. Layout is the final product of an ECAD framework and links the circuit designer to the fabrication facilities. It is also the natural linkage to TCAD, as this tries to substitute the fabrication process by simulation.

A. Layout Edition

In the TCAD framework VISTA [17], the tool PED is used to handle layout data [18]. It can edit small pieces of layout from scratch and accepts files in CIF or GDSII stream formats created elsewhere (by far the most popular ones among ECAD frameworks), converting them to the VISTA internal data representation. Besides data conversions, it provides a direct interface between layout data and the process simulators of VISTA. It allows one to perform Boolean operations with the masks of the layout and, as the final result must be a circuit-level model, to interactively specify net names (or generate them automatically). These net names are consistently kept along all the simulation phases in order to be included in the final netlist, as is done in conventional extraction programs found in ECAD frameworks. In the case of resistance/thermal simulation, contacts where a voltage/current density (or temperature) is forced have to be specified. Once more, the extracted resistors are annotated according to the names in the layout. An example of layout is shown in Fig. 2.

B. Parameterized Layout

In a new process development, different variations of parameters (e.g., the physical dimensions) have to be analyzed. To assist the generation of these sets of data, we include facilities to create parameterized layouts. The result can be then linked with optimization procedures or response surface methodology to investigate in detail the coupling between the layout and device/circuit performance.

In our approach, the generation of parameterized layout sets can be separated into four steps:

1) edition of a template layout;
2) specification of steps;
3) specification of constraints;
4) specification of the result as operations with masks of the template layout, where obviously a given number of them changes at each iteration.

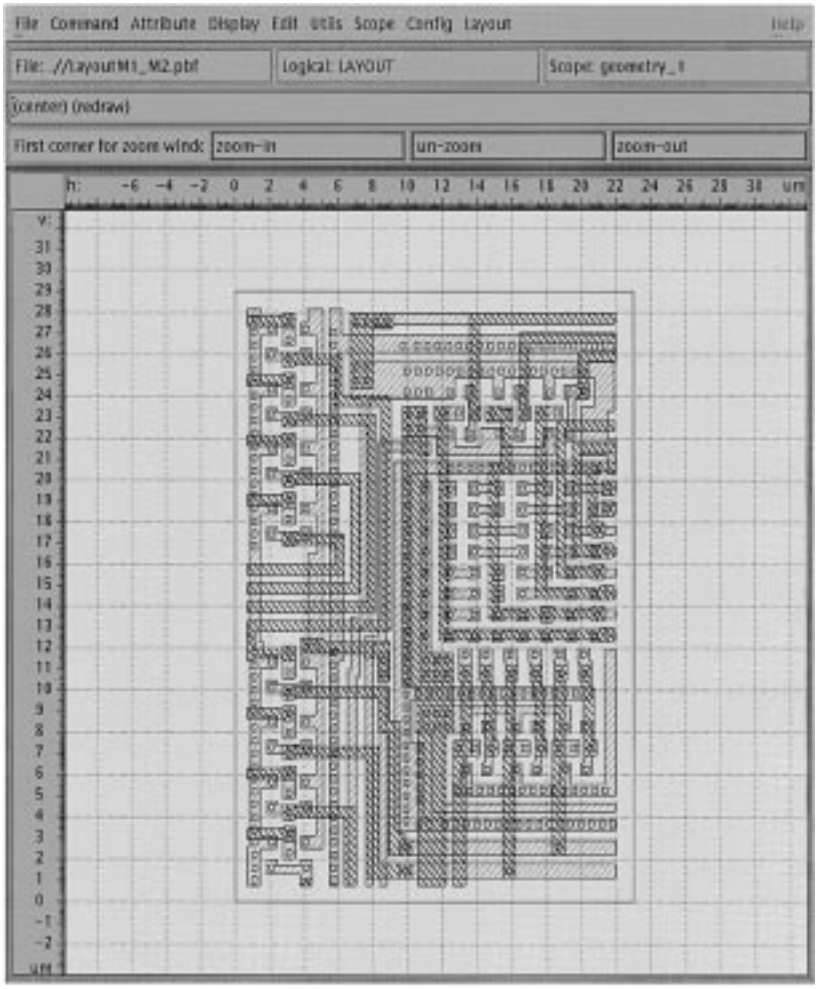


Fig. 2. Layout example (only the interconnect layers are shown).

The most important among the operations are *rotation, translation, scale, stretch-left, stretch-right, stretch-up, stretch-down,* and the usual Boolean operations. The way the constraints are used is twofold: to generate a premature exit condition (or warning message) and to force some relations between masks. These relations will have maximum priority. The last three steps are specified in an auxiliary ASCII file, as in Fig. 3, which shows the syntax required for the automatic generation of layout sets (used in the plunge trim resistor in Fig. 15) with different laser cut lengths.

```
; Generation of laser trimmed plunge
; resistor sets.
;
(step
  (y 0 9 1))

(constraints
   (exit !fullInside[SiO2 HI_POLY])
   (warning less[height[HI_POLY]-height[SiO2],
                 1.0] 'Too big cut!'))

(evaluate
   (SiO2= stretchUp[iSiO2 y 1.0])
   (HAZ= stretchUP[iHAZ y 1.0] && !SiO2)
   ($DUMMY= SiO2 || HAZ)
   (HI_POLY= iHI_POLY && !$DUMMY))
```

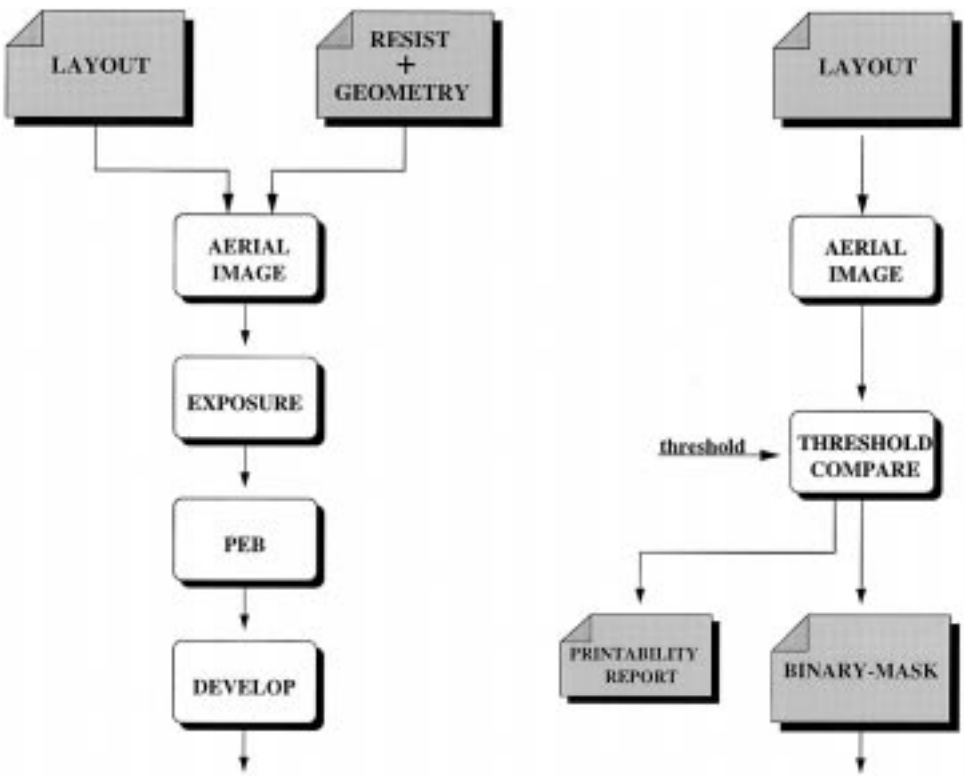
Fig. 3. Syntax required for the automatic generation of layout sets.

C. Lithographic Issues

As indicated in Fig. 1, we can precede the topography simulation with a lithography analysis. This way, we take into account that the real structures deviate from the layout due to lithographic phenomena. One typical example in interconnect lines occurs in "nested elbows," where (with decreasing linewidth) the corners get bloated and the elbows rounded. The line endings also become rounded and shrunk (see Fig. 6).

One important enhancement in lithographic techniques is the use of phase-shift masks [19]. The conventional layout editing features of PED are extended with the capabilities for phase-shift masks edition, as this feature is not available in conventional ECAD layout editors. For the background and for every polygon of any mask, we can specify values of the modulus and phase attributes of their transmittance.

A complete lithography simulation flow as in Fig. 4(a) is too complex and consumes too much time/resources. In



(a) (b)

Fig. 4. (a) Complete lithography simulation flow. (b) Simplified simulation flow.

the approach described here, only the aerial intensity image is calculated. Next, it is compared at each point with a threshold value in order to generate a binary aerial image that is used as a conventional binary mask in the further process simulation steps—see Fig. 4(b). This also allows the use of phase-shift masks without any special processing. The threshold can be entered manually or calculated automatically in the same way as in [20]. To compute the aerial intensity image on the resist, the simulator `illum2d` [21], which is tightly connected with `PED`, is used. After performing these tasks, it is possible to generate a report of printability of the input layout, where the critical nets (if existing) are pointed out. Fig. 5 depicts the aerial image of mask Metal 2 of the layout in Fig. 2. The simulated imaging system uses a lens with a numerical aperture of 0.55 and a wavelength of 365 nm (I-line), and the focus error is 1 μm. The resulting binary mask is shown in Fig. 6.

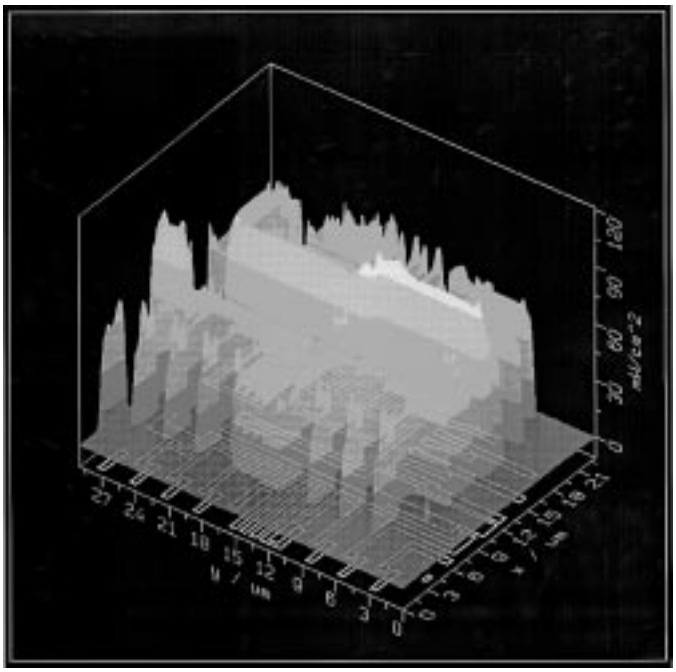


Fig. 5. Aerial image of mask Metal 2 of the layout in Fig. 2.

III. Topography Simulation

If the structures to be simulated are strongly nonplanar, an accurate topography simulation must be performed. Otherwise, simple rules can be used to derive the three-dimensional model from the layout. In our solution, one can decide which level of topography simulation is to be used. In the second case, a perfect planarization is assumed for each layer. However, if maximum accuracy is necessary, the three-dimensional topography simulator `etch3d` [22] is utilized. This program uses methods based on morphological operations derived from image processing, which are performed on a cellular material structure where the formation of unphysical surface loops is completely avoided.

A. Solid Modeling and Grid Generation

In the cellular format, materials are represented as a three-dimensional array of cubic cells. Each cell refers to a different

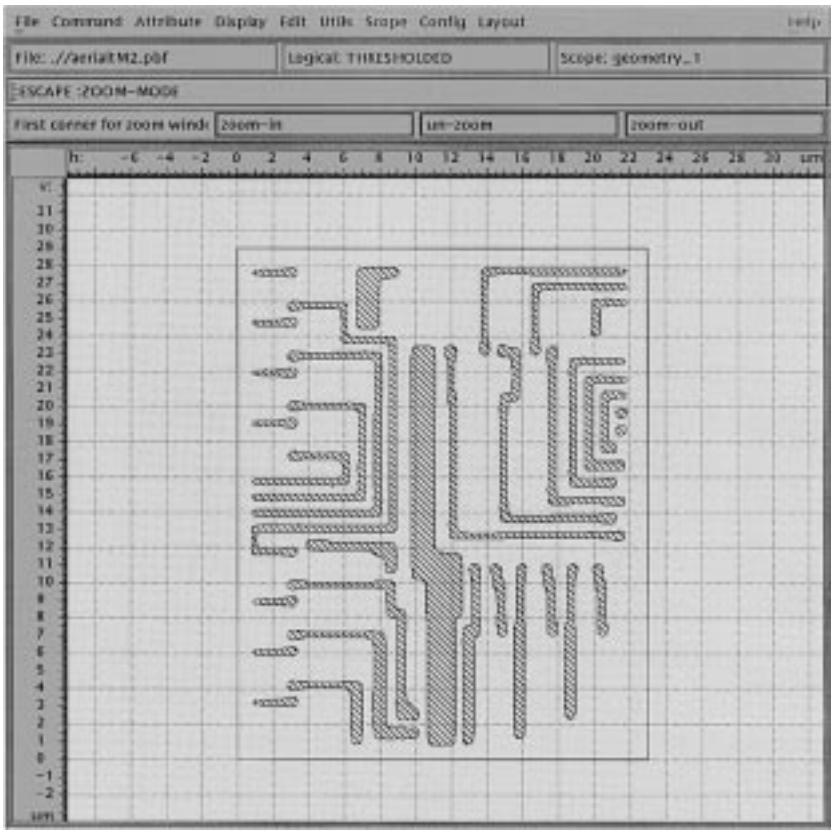


Fig. 6. Binary mask after applying threshold.

material identified by a 7-bit index. Although presenting several advantages as pointed out in [22], the use of a cellular material representation poses difficult problems in the linkage with the finite-element-based capacitance and resistance/thermal simulators. They require a quite different data format for the structure geometries and, of paramount importance, a grid.

We use the preprocessor `laygrid` [23] to generate three-dimensional (tetrahedral) grids compatible with the used finite-element simulators. It works based on a layered description, where a complete structure is created by stacking planar layers (that are associated with some thickness). Each layer is made of faces with contacts (specifying net names and external voltage/current conditions) and material references. In the stacking process, all new cutting faces are calculated, and then the preprocessor grids each layer with a modified version of Bank's mesher `trigen` [24] or (at user's choice) with Shewchuk's `triangle` [25]. By doing this, the preprocessor is quite suitable for generating structures directly from layout, but proved to be useful as well with the structures created by the topography simulator, as explained next.

One plane of the three-dimensional array of the cellular material representation can be considered as a bitmap image. If we apply an edge-detection algorithm to it, polygonal faces defining material boundaries are found and used to build one layer for the laygrid preprocessor. To generate a complete structure, the array is sampled in the vertical direction and a new layer is inserted if the difference between the actual image and the last that has been inserted is larger than an error criterion. In Fig. 7, we show the polygonal faces obtained at the boundaries between two materials in nonuniform sampled planes. As along with the number of inserted planes, the number of grid nodes increases (which means more memory and time needed to perform the consequent simulations), an efficient sampling must be performed. Simple algorithms based on an overall error over the image are not satisfactory, as they

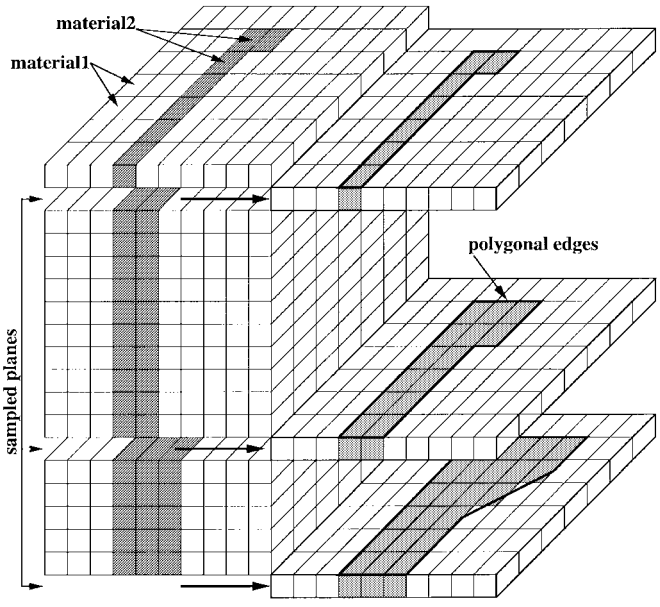


Fig. 7. Extraction of polygonal faces from cellular data.

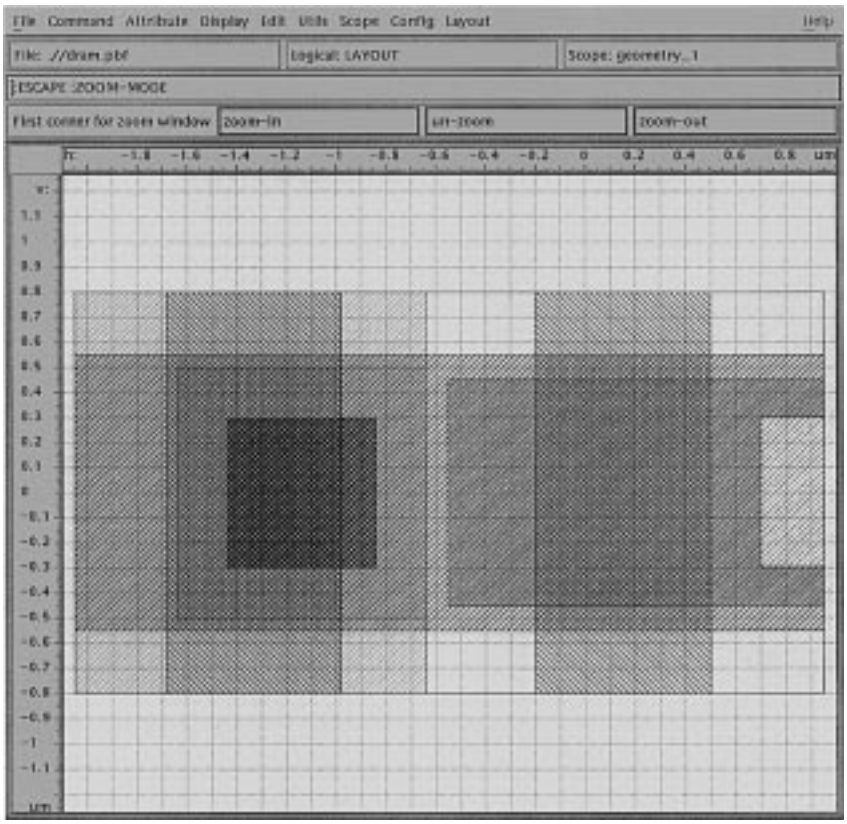


Fig. 8. Layout of DRAM cell.

tend to ignore small feature details. The following algorithm overcomes this problem.

1) Divide the plane in regions of the same material R_{Mi} and for each one calculate its area $A(R_{Mi})$, which means counting the number of adjacent cells with same index.
2) Add each R_{Mi} to the equivalent in the last written plane. Equivalent means that they have the same material and they overlap somewhere. Then calculate the area of the sum $A(Sum_i)$.
3) For all R_{Mi}, calculate

$$Error_i = \frac{A(R_{Mi})}{A(Sum_i).}$$

4) If any $Error_i$ is larger than a certain value, this plane is written; otherwise, jump to the next plane.

This way, a three-dimensional structure is created and gridded in a form compatible with the subsequent tools. The main advantages of this approach are the simplicity and robustness. As a drawback, it generates more grid points than necessary if the structures present large variations in the vertical direction. This is compensated for by easily allowing one to build structures that are partially derived from real topography simulation and partially created directly from the layout (saving grid points). This is the case in Fig. 9, where the trench capacitor is formed by real topography simulation and the poly-gate and metal lines are obtained directly from the layout of Fig. 8. The bottom part of the capacitor was created so as to avoid sharp edges at the corners, which may lead to the formation of a thinner oxide layer there. As a high electric field will emerge in these regions, a too large leakage current could occur [26]. To round the corners, an oxidation and stripping step was made before forming the actual SiO_2 dielectric film. As this is only 10-nm thin, a very large number of grid points are necessary to resolve such small dimensions (as seen in Fig. 9), making this a difficult problem and a good test of the capabilities of the tools. In Fig. 9, we also see the described adaptive sampling mechanism of Z-planes in the grid.

IV. Capacitance and Resistance/Thermal Simulation

Once the structures are gridded, we use SCAP and STAP [6], [23], finite-element-based simulators for calculating capacitances and resistances (or performing thermal analysis). Transient electrical simulation is also possible to be performed. This is of interest in cases where a very accurate estimation of delay times and cross talk between arbitrary shape lines is necessary. In these cases, lumped models based on the extracted resistances and capacitances simply cannot achieve a sufficiently good precision.

A. Capacitance Extraction

In a circuit with n nets (made physically with conductive materials), there are always $\frac{1}{2}n(n-1)$ capacitors $C_{i,j}$ across them. These may be desired capacitors by the integrated circuit designer, or parasitic ones that have unwanted influence on the circuit performance. Whatever the case, our simulator returns

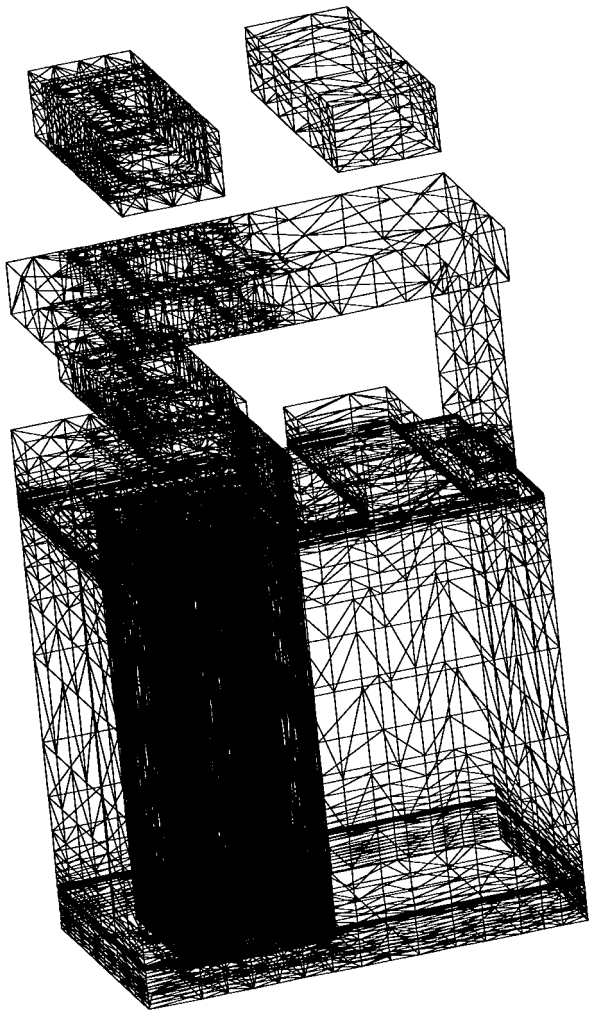


Fig. 9. Grid of a DRAM cell with a trench capacitor.

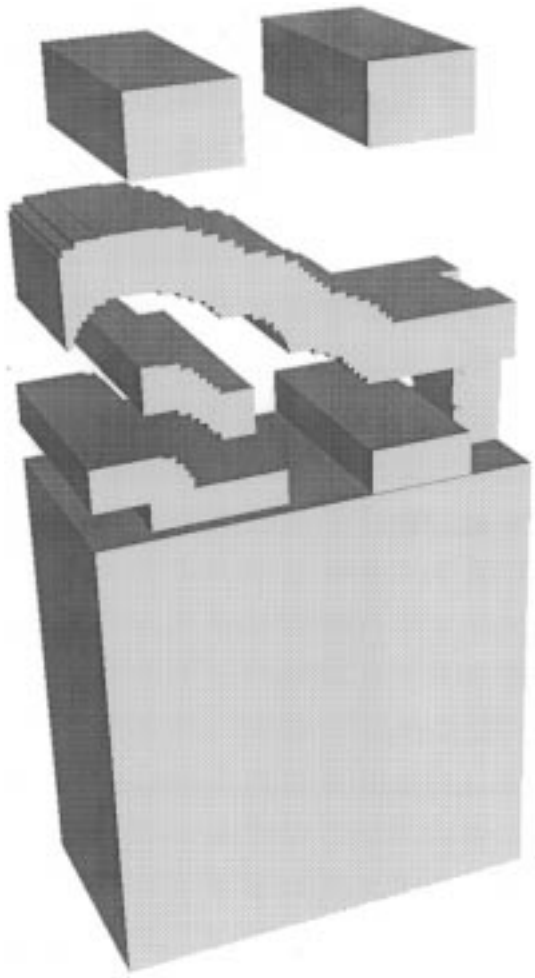


Fig. 10. DRAM cell with accurate topography simulation of interconnect lines.

a netlist with all capacitors in a SPICE like circuit description format:

- C_{1_0} 1 0 *value* [unit];
- C_{1_2} 1 2 *value* [unit];
- C_{1_3} 1 3 *value* [unit];
- C_{2_0} 2 0 *value* [unit];
- ….

The energy method is used to calculate the capacitance values, as high numerical accuracy is achieved. The energy W in a system with n conductors is

$$W = \tfrac{1}{2}\sum_{i=1}^{n}\sum_{j=i+1}^{n} C_{i,j}(\psi_i - \psi_j)^2.$$

Therefore, we must apply $\frac{1}{2}n(n-1)$ different potential conditions and solve the resulting linear system to obtain all capacitor values. The electric potential φ for each partial capacitance pair is obtained solving Laplace's equation

$$div(\epsilon\ grad\ \varphi) = 0$$

where ϵ is the permittivity tensor.

TABLE I

	Planar	Non-planar	Measured
	fF	fF	fF
C_{trench}	40.1	40.1	38.2
C_{bit_line}	1.04	1.72	1.88
$C_{word-line}$	2.22	3.35	-
$C_{bit-line,word-line}$	0.34	0.42	-
$C_{bit-line}/C_{trench}$	3.3	5.5	6.3

B. Resistance and Thermal Simulation

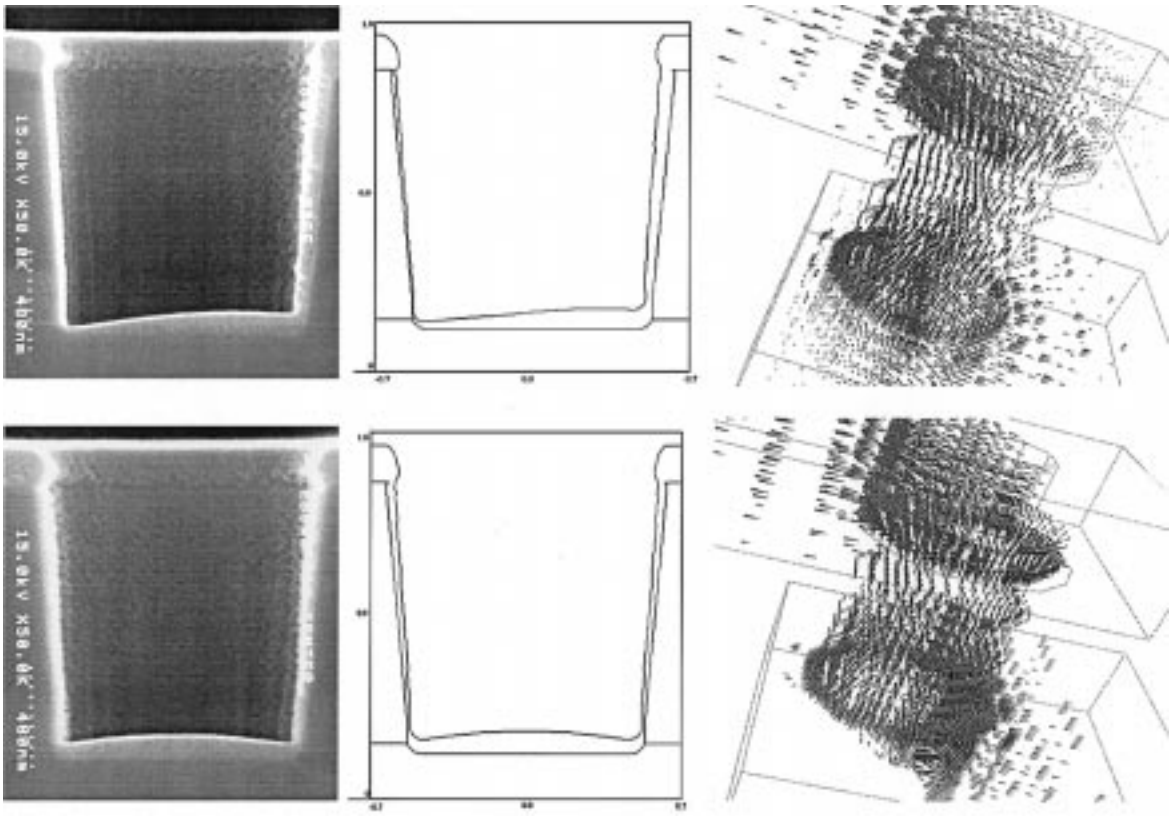
A similar equation must be solved to calculate the current density and potential distribution inside the conductors. If γ_E denotes the electrical conductivity (assumed to be zero in all nonconductor materials), we obtain

$$div(\gamma_E\ grad\ \varphi) = 0. \tag{1}$$

For the thermal problem the solution of

$$div(\gamma_T\ grad\ T) = -p$$

in all simulation domains is required. Here, γ_T represents the thermal conductivity, T is the temperature distribution, and $p = \gamma_E(grad\ \varphi)^2$ is the power loss density.



(a) (b) (c)

Fig. 11. Contact simulation. (a) SEM picture (after TiN sputtering). (b) Result from topography simulation (a cut is shown). (c) Current density in the contact.

The electrical and thermal equations are linked by a first-order approximation given by

$$\gamma_E = \gamma_0 \frac{1}{1+\alpha(T-T_0)}$$

where α is a constant temperature coefficient and γ_0 is the electric conductivity at room temperature T_0.

C. Transient Simulation

To perform the transient potential distribution, the time-varying term ∂t is included in (1), which becomes

$$div\left(\gamma_E \; grad\, \varphi + \epsilon \; grad \frac{\partial \varphi}{\partial t}\right) = 0.$$

To optimize the simulation speed, the implemented algorithm uses an adaptive time step.

V. Examples

A. DRAM Cell

The dynamic RAM (DRAM) is the flagship product of the semiconductor industry. To continue the minimization of cells' area, more and more TCAD simulations must be performed. As in a DRAM, the information is stored as charge in a capacitor, a good characterization of this and the total bit-line parasitic capacitance is fundamental in the development of new cell configurations. Using our capacitance simulator, we studied a variation of the stacked trench cell [27] (where the storage capacitor was made rectangular instead of circular).

We divided the study in two parts. Initially, only the storage capacitor was carefully simulated (see Section III), and the metal lines were considered planar as shown in Fig. 9. Then we performed a topography simulation for the complete cell (whose solid model is shown in Fig. 10). The experimental data and the results obtained for both cases are presented in Table I, which shows a significant improvement of the nonplanar model (in the $C_{bit\text{-}line}$ the error was reduced by a factor of five) over the simple model. Here, the large errors result from the nonplanarity of the bit-line interconnection wire and demonstrate the need for topography simulation. The value of $C_{bit\text{-}line}/C_{trench}$ is for the case of 128 cells sharing the same bit-line.

B. Capacitance of General Interconnect Submicrometer Lines

So as to justify the need of accurate topography in interconnect lines, we extracted the capacitances of some nets of the layout in Fig. 2 using a 0.35-μm technology. As before, we compared the results when a simple solid model is assumed with those after three-dimensional topography simulation (with lithography taken into account). We found that for the capacitances to the substrate (connected to ground), the variation is negligible, but for the interline capacitances, it changed from 1% to a maximum of 31%. This difference is significant because the interline capacitance dominates over the capacitance to ground. Although we selected the nets more or less randomly (from the longer ones), the lines with higher differences are likely to occur because they correspond to those drawn side by side that are commonly used in buses. The

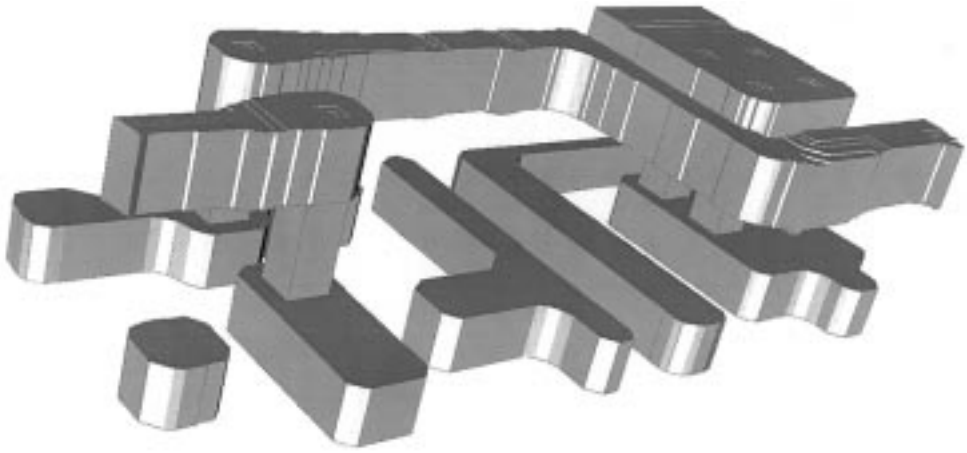


Fig. 12. Part of the three-dimensional model of the layout of Fig. 2.

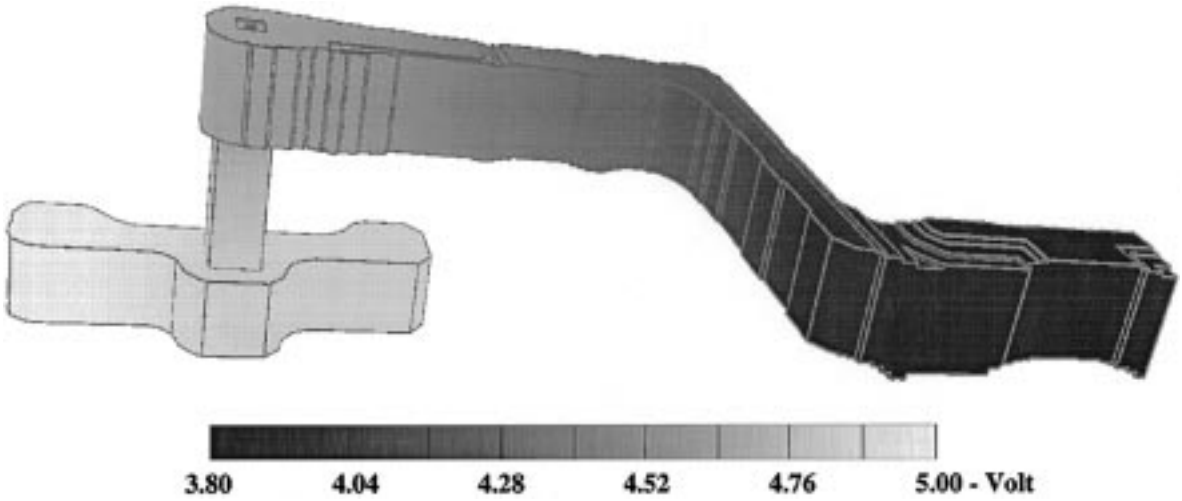


Fig. 13. The potential distribution along the wire.

maximum variation obtained is almost identical to that from measured data—30% [28].

C. Contact Resistance Analysis

Contacts and vias are often the weak points in integrated circuits. Their electrical characteristics must be studied in order to determine under what circumstances they affect circuit performance or reliability. Our tools can be used for analyzing vias and the ohmic contact between metal or metal-silicide thin films and single-crystal silicon.

We present here two contact structures, where a titanium nitride barrier layer is used to insulate metallurgically the metal from the semiconductor. In Fig. 11(a), we show scanning electron microscope (SEM) pictures after a TiN deposition into a 1.0-μm circular hole located 260 mm below the center of the sputter target disk (bottom picture) and when the deposition of TiN is made at a position 90 mm off the wafer center (top picture). The center pictures, cuts from the simulated three-dimensional structures, agree well with the SEM's. In Fig. 11(b), we show the current density in the two contacts, after being filled with aluminum. The effect of the asymmetry in the TiN layer in the current density is clearly seen. In the top case, the current flows mainly in unusual areas, namely, in the trailing edge of the contact, whereas in the other case, we have the known current crowding effect at the opposite edge. As electromigration problems are worsened by current crowding effects [29], our tools can be used to understand and minimize this unwanted phenomena. The resistance values obtained were 0.77 and 0.89 Ω for the upper and lower cases, respectively, and agree well with the experiments.

D. Resistance of Interconnect Wires

Metal wires are also subject to defects. Besides electromigration problems, shorted lines and too narrow lines (or even opens) are also causes of integrated circuit failure. These, in turn, are sometimes related with lithographic issues. We can predict these problems by performing a lithography simulation as shown in Fig. 4(b). The tools provide a report indicating possible problems in the printability of one given layout. Using the imaging system described, some possible too narrow line faults for the layout of Fig. 2 were pointed out.

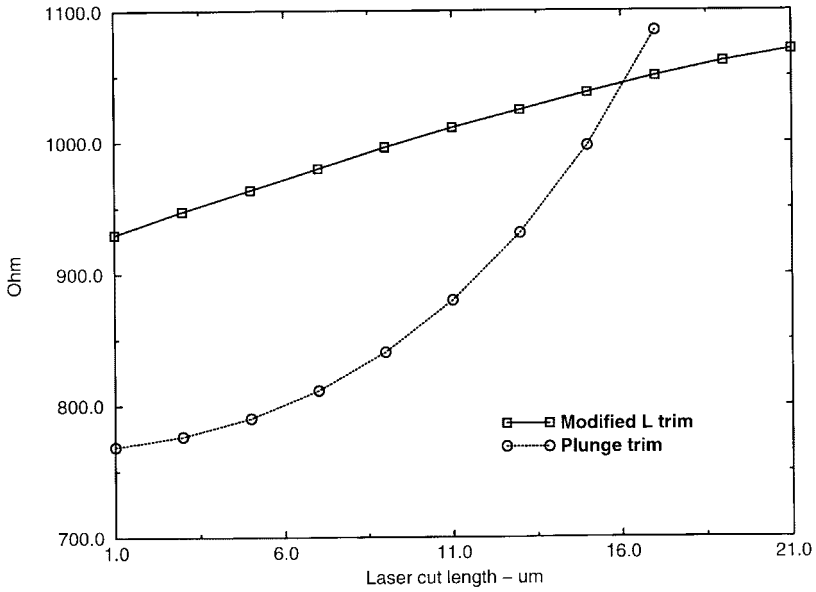


Fig. 14. Dependence of resistance value on laser cut length.

In Fig. 12, we show a part of the three-dimensional model, where an electrical simulation was done. We observed that the current density in some places is two times larger than that for structures where lithography is not taken into account. The corresponding voltage drop along some lines is also too high, as shown in Fig. 13. We concluded that the layout, with some automatically routed nets in Metal 2, must be modified.

E. Laser-Trimmed Resistors

Laser trimming of film resistors allows integrated-circuit manufacturers to very accurately control resistance values. Being an expensive process step, it is important to maximize the benefits once that option is taken [30]. Our electrical/thermal simulator allows easy characterization of different trim algorithms.

The performance of laser-trimmed resistors is related to the so-called heat-affected zone (HAZ) [30], formed during the trimming process. The HAZ corresponds to a region along the edge that, being heavily heated (but still below the vaporization temperature), after cooling suffers an alteration in its physical properties, namely, in the sheet resistance, temperature coefficient, and aging.

We model the sheet resistance of HAZ as in [30]. The use of parameterized layout generation facilitates the preparation of sets corresponding to different lengths of the laser cut. The simulated structures are then formed directly from the layout and are made of a silicon substrate, a SiO_2 layer, the high-resistivity polysilicon resistor layer, and a passivation SiO_2 layer. The bottom of the silicon substrate is kept at a constant temperature of 300 K. We compared the classical plunge trim and a modified L-trim resistor as in Fig. 15 with the same dimensions and geometry before trim. The target resistance is 1000 Ω for both resistors.

Fig. 14 shows the dependence of the resistance value as function of the cut length. As near 1000 Ω the sensitivity is much lower in the modified L-trim, its better accuracy is evident. In Fig. 15, we present the temperature distribution

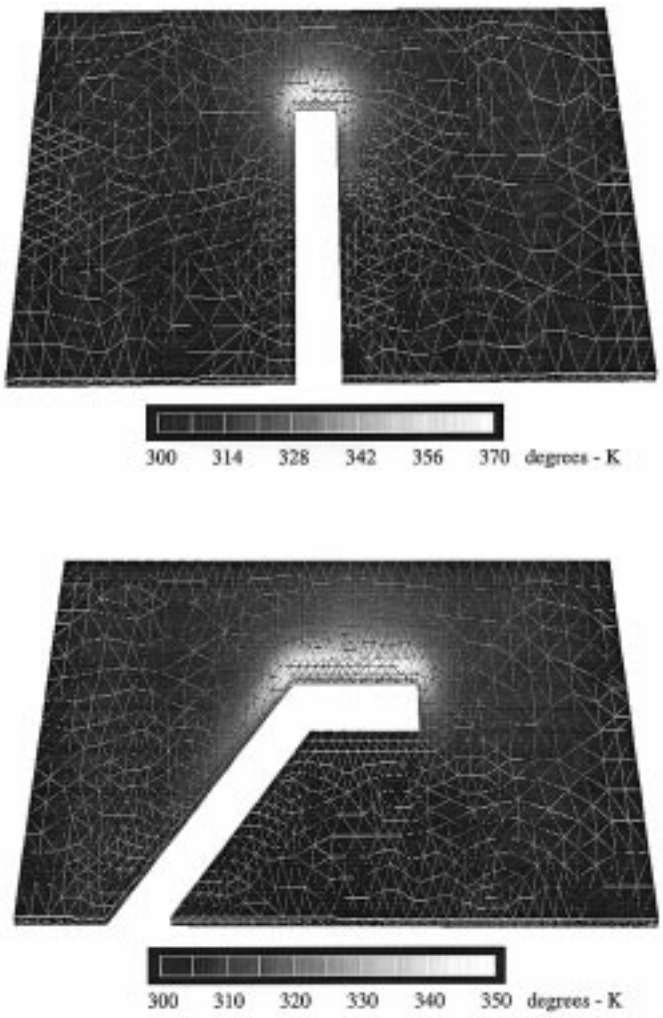


Fig. 15. Temperature distribution in two different resistor configurations trimmed to 10 000 Ω.

along the resistors. We can see the crowding effect in the HAZ (corresponding to the maximum values in the current and

temperature) and that for the same overall power dissipation, the maximum temperature is 20°C lower in the modified L-trim resistor. This predicts a much more stable aging of resistors using this trim algorithm.

VI. Conclusions

To perform accurate capacitance and resistance extraction of interconnect structures, the planar and conformal three-dimensional models are sometimes too incomplete, and a rigorous topography simulation is required. In this paper, we presented a layout-driven ECAD/TCAD integrated environment capable of performing capacitance and resistance/thermal simulations over three-dimensional structures created with accurate topography simulators and taking lithography effects into consideration. Some possible applications were also discussed.

References

[1] N. D. Arora, K. V. Raol, R. Schumann, and L. M. Richardson, "Modeling and extraction of interconnect capacitances for multilayer VLSI circuits," *IEEE Trans. Computer-Aided Design*, vol. 15, pp. 58–67, Jan. 1996.

[2] U. Choudhury and A. Sangiovanni-Vincenteli, "Automatic generation of analytical models for interconnect capacitances," *IEEE Trans. Electron Devices*, vol. 14, pp. 470–480, Apr. 1995.

[3] A. H. Zemanian, R. P. Tewarson, C. P. Ju, and J. F. Jen, "Three-dimensional capacitance computations for VLSI/ULSI interconnections," *IEEE Trans. Computer-Aided Design*, vol. 8, pp. 1319–1326, Dec. 1989.

[4] A. Seidl, M. Svoboda, J. Oberndorfer, and W. Rosner, "CAPCAL-A 3D capacitance solver for support of CAD systems," *IEEE Trans. Computer-Aided Design*, vol. 7, pp. 549–556, May 1988.

[5] Q. Ning, P. M. Dewilde, and F. L. Neerhoff, "Capacitance coefficients for VLSI multilevel metallization lines," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 644–649, Mar. 1987.

[6] M. Mukai, T. Tatsumi, N. Nakauchi, T. Kobayashi, K. Koyama, Y. Komatsu, R. Bauer, G. Rieger, and S. Selberherr, "The simulation system for three-dimensional capacitance and current density calculation with a user friendly GUI," *Tech. Rep. IEICE*, vol. 95, pp. 63–68, 1995.

[7] A. J. van Genderen and N. P. van der Meijs, "Using articulation nodes to improve the efficiency of finite-element based resistance extraction,' in *Proc. 33rd Design Automation Conf. (DAC'96)*, June 1996, pp. 758–763.

[8] R. Bauer, M. Stiftinger, and S. Selberherr, "Capacitance calculation of VLSI multilevel wiring structures," in *Proc. VPAD*, 1993, pp. 142–143.

[9] M. Bächtold, J. G. Korvink, and H. Baltes, "Enhanced multipole acceleration techniques for the solution of large poisson computations," *IEEE Trans. Computer-Aided Design*, vol. 15, pp. 1541–1554, Dec. 1996.

[10] Z. Wang, Y. Yuan, and Q. Wu, "A parallel multipole accelerated 3-D capacitance simulator based on an improved model," *IEEE Trans. Computer-Aided Design*, vol. 15, pp. 1441–1450, Dec. 1996.

[11] Y. L. Le Coz, R. B. Iverson, H. J. Greub, P. M. Campbell, and J. F. McDonald, "Application of a floating-random-walk algorithm for extracting capacitances in a realistic HBT fast-RISC RAM cell," in *Proc. 11th Int. VLSI Multilevel Interconnection Conf. (VMIC)*, June 1994, pp. 542–544.

[12] R. H. Uebbing and M. Fukuma, "Process-based three-dimensional capacitance simulation-TRICEPS," *IEEE Trans. Computer-Aided Design*, vol. CAD-5, pp. 215–220, Jan. 1986.

[13] J. P. Elliot, G. A. Allan, and A. J. Walton, "The automatic generation of conformal 3D data for interconnect capacitance simulation," in *Proc. VLSI Multi-Level Interconnect Conf.*, June 1995, pp. 664–666.

[14] "RAPHAEL reference manual," Technology Modeling Associates, Sunnyvale, CA.

[15] "TEMPEST manual," Silvaco International, Santa Clara, CA.

[16] "SOLIDIS manual," ISE AG, Zurich, Switzerland.

[17] S. Halama *et al.*, "VISTA—User interface, task level, and tool integration," *IEEE Trans. Computer-Aided Design*, vol. 14, pp. 1208–1222, Oct. 1995.

[18] R. Martins and S. Selberherr, "Layout data in TCAD frameworks," in *Proc. Eur. Simulation Conf.*, June 1996, pp. 1122–1126.

[19] Y. Liu, A. K. Pfau, and A. Zakhor, "Systematic design of phase shift masks with extended depth of focus and/or shifted focus plane," *IEEE Trans. Semiconduct. Manufact.*, vol. 6, pp. 1–21, Feb. 1993.

[20] C. Sengupta, J. R. Cavallaro, W. L. Wilson, Jr., and F. K. Tittel, "Automated evaluation of critical features in VLSI layouts based on photolithographic simulations," *IEEE Trans. Semiconduct. Manufact.*, vol. 10, pp. 482–494, Nov. 1997.

[21] H. Kirchauer and S. Selberherr, "Three-dimensional photolithography simulation," *IEEE Trans. Computer-Aided Design*, vol. 16, June 1997.

[22] E. Strasser and S. Selberherr, "Algorithms and models for cellular based topography simulation," *IEEE Trans. Computer-Aided Design*, vol. 14, pp. 1104–1114, Sept. 1995.

[23] R. Sabelka, K. Koyama, and S. Selberherr, "STAP—A finite element simulator for three-dimensional thermal analysis of interconnect structures," in *Proc. Simulation in Industry—9th Eur. Simulation Symp.*, Oct. 1997, pp. 621–625.

[24] R. E. Bank, "PLTMG: A software pakage for solving elliptic partial diffrential equations," in *Frontiers in Applied Mathematics*, vol. 7. Philadelphia, PA: SIAM, 1990.

[25] J. R. Shewchuk, "Triangle: Engineering a 2D quality mesh generator and Delaunay triangulator," in *Proc. 1st Workshop Applied Computational Geometry*, May 1996, pp. 124–133.

[26] S. Wolf, *Silicon Processing for the VLSI Era*. Sunset Beach, CA: Lattice Press, vol. 2, 1990.

[27] S. Fujii *et al.*, "A 45-ns 16-Mbit DRAM with triple-well structure," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1170–1175, Oct. 1989.

[28] D. H. Cho *et al.*, "Interconnect capacitance, crosstalk, and signal delay for 0.35 μm CMOS technology," in *Tech. Dig. Int. Electron Devices Meeting*, 1996.

[29] D. Gardner, J. Meindl, and K. Saraswat, "Interconnection and electromigration scaling theory," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 633–643, Mar. 1987.

[30] J. Ramírez-Angulo, R. Geiger, and E. Sánchez-Sinencio, "Characterization, evaluation, and comparison of laser-trimmed film resistors," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 1177–1189, Dec. 1987.

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