A CMOS IC for Portable EEG Acquisition Systems

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***Abstract*—We present a monolithic low-power, low-noise analog front-end electroencephalogram acquisition system. It draws only 500 μA from a standard 9-V battery, making it suitable for use in portable systems. Although fabricated in a standard CMOS technology, by using current feedback techniques it achieves a common mode rejection ratio of 100 dB while the total input noise referred to input is kept below 1.5 μV (rms).**

***Index Terms*— Analog integrated circuits, CMOS, CMRR, instrumentation amplifiers, noise, VLSI.**

I. Introduction

THE USE of very large-scale integration (VLSI) techniques in biomedical instrumentation opened the doors toward the miniaturization and portability of such systems. Among other benefits this portability gives more freedom of movements to the patient (of particular importance in long duration exams) and allows the use of very small leads between the electrodes and the input amplifiers [1]. This last point is of great importance on systems that are usually used in noisy environments, while the signals to acquire have very low levels (down to few microvolts). But portability requires very low power consumption to guarantee long life to the battery, which in turn creates constraints in circuits performance that are difficult to overcome.

In this paper a monolithic implementation of an analog front-end for a portable EEG acquisition system is presented. Besides low-power, the key design points are high common mode rejection ratio (CMRR) and very low noise. Minimum component count is also important to reduce system weight and volume.

The system includes 16 instrumentation amplifiers (IA), one 16:1 analog multiplexer, one programmable gain amplifier, autocalibration circuitry for nulling mismatches among the 16 channels (including a test signal oscillator), a microprocessor compatible digital interface, and an internal current/voltage reference source as shown in the block diagram of Fig. 1. It was implemented in the low-cost MIETEC 2.4 μm double-poly/double-metal CMOS technology, providing opportunity for a complete system integration if an analog-to-digital converter (ADC) and telemetry circuitry are added.

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II. Instrumentation Amplifiers (IA's)

In an acquisition system the overall performance strongly depends on the quality of its input IA's. They are the most critical elements in the integrated circuit described here and are therefore, the components to which more attention was given.

CMOS is unquestionably the best technology for micropower circuits [2]. However, among other problems associated with it, the CMRR behavior is worse than the bipolar and JFET counterparts. As EEG signals exhibit low frequencies (0.3–150 Hz) [3], the flicker noise becomes another potential problem. Since we are not interested in circuits using sampling techniques [4], only a careful full-custom design can overcome such difficulties.

A. Current Feedback Instrumentation Amplifiers

Conventional resistive feedback differential amplifiers (where the classical three operational amplifier structure is included) are not suitable when low power, low cost, and high CMRR are simultaneously required. They need operational amplifiers with low output impedance to drive the feedback resistors, which implies high currents and large power drain. In addition, precisely matched resistors are needed to achieve high CMRR. This matching usually requires laser trimmed resistors, an expensive technique not available in a standard CMOS technology. One way to overcome these problems is the use of current feedback amplifiers [5]–[9] whose basic functional block diagram is presented in Fig. 2. Analyzing the input branch of this figure, we conclude that a high input impedance is guaranteed by two unity gain buffers. Thus, the current in resistor R_g is

$$i_g = \frac{1}{R_s} \cdot (v_1 - v_2) \tag{1}$$

whereas the output voltage equals

$$v_{\text{out}} = R_s \cdot i_s + v_{\text{ref}}. \tag{2}$$

The input and output circuits behave as a transconductance amplifier and a transresistance amplifier, respectively. If the current in the input branch is mirrored into the output (and $i_1 = i_g = i_2 = i_s$) we obtain

$$v_{\text{out}} = \frac{R_s}{R_g} \cdot (v_1 - v_2) + v_{\text{ref}} \tag{3}$$

the usual relation for an instrumentation amplifier. But it is important to note that, contrary to the classical configuration with three operational amplifiers, there is no global feedback (from the output to the input) and that there is only one high

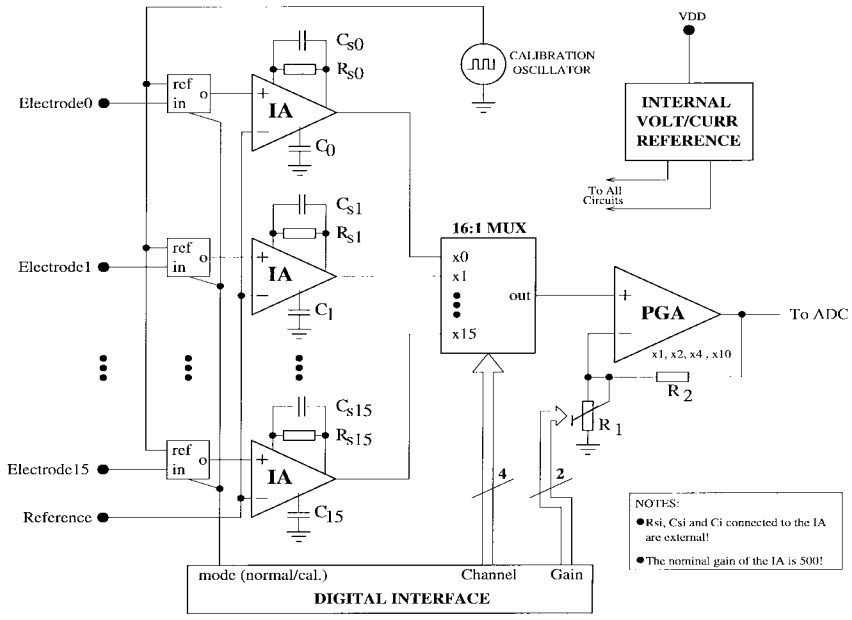


Fig. 1. IC block diagram.

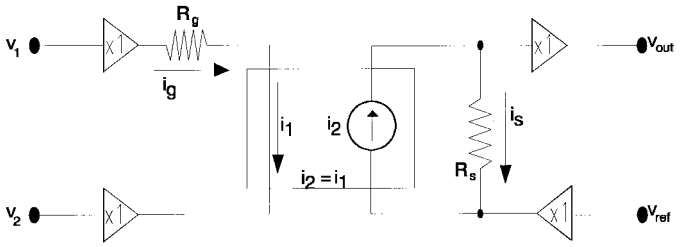


Fig. 2. Block diagram of an IA with current feedback.

impedance node, which simplifies the frequency compensation. Another advantage is that the CMRR (and the gain as well) do not depend on any matching of resistor values. The resistor count is also reduced, saving chip area.

B. Implementation Issues

There are different possibilities to design a current feedback IA. Most of the reported ones are in bipolar technology [5]–[7] and [8] uses CMOS. We implemented a CMOS variation of [6], as with this configuration only a reduced number of stacked transistors is necessary (improving dc behavior at low voltage power supplies) and only two transistors at input are needed (optimal for noise reasons). Also, as PMOS transistors exhibit low flicker noise for the same area, we chose them to the input as shown in Fig. 3.

The circuit with no signal applied is fully balanced, so all currents are equal and $v_{\text{out}} = 0$. When a differential signal is applied, the output currents of the transconductance amplifier GM become unbalanced in order to maintain the drain currents of M1 and M2 equal. In this situation, if both transistors are well matched their gate-source voltages are approximately equal and

$$i_{Rg} = \frac{v_1 - v_2}{R_g}.$$

We can say that M1 and M2 linearized by GM replace the input buffers of Fig. 2. The transistors M7 and M8 linearized by the voltage amplifier Av working in a complementary (but similar) way, convert an input current into a voltage according to

$$i_{Rs} = \frac{(v_{\text{out}} - v_{\text{ref}})}{R_s}.$$

Since the output current of the input circuit is mirrored by M6–M9 and M5–M10 the output/input relation becomes exactly (3).

With the aim of reducing noise to the minimum, the IA also incorporates circuitry to make it a bandpass filter (0.3–150 Hz). For the low-pass filter, a capacitor C_s is connected in parallel with R_s, which causes a pole at

$$f_H = \frac{1}{2\pi \cdot R_s \cdot C_s}.$$

The high-pass filter action is more difficult to implement. The use of a passive *RC* filter is not a good solution for such a low cut-off frequency (0.3 Hz), so it was implemented using another feedback loop around the output circuit, as shown in Fig. 4. $\text{GM}_{\text{filter}}$ acts as a resistor, but offers two advantages over a real one: First, as it is possible to make its transconductance low, a high equivalent resistor can be

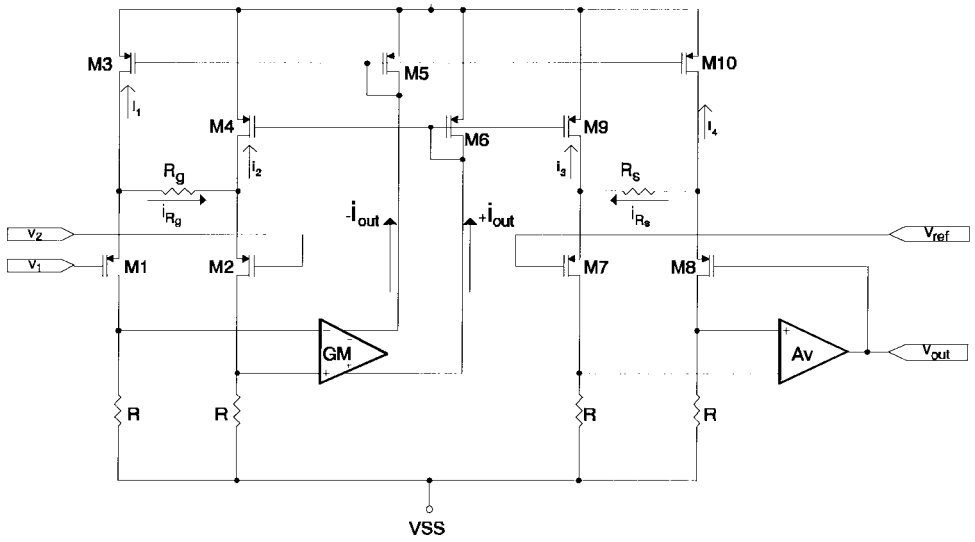


Fig. 3. Simplified IA circuit.

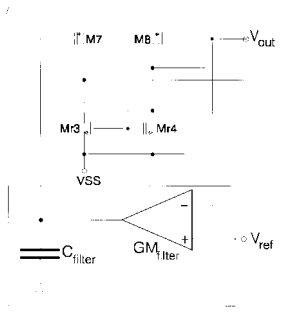


Fig. 4. Feedback loop realizing the hi-pass filter function.

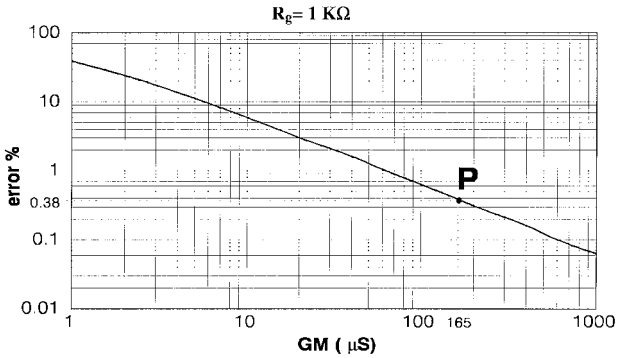


Fig. 5. Transconductance error (ideal gain is $1/R_g$).

obtained (>1 MΩ). Second, there is no resistive loading of the output. The zero is at frequency

$$f_L = GM_{\text{filter}}/(2\pi \cdot C_{\text{filter}}).$$

To improve the CMRR and reduce power consumption, the input transistors were made to work almost in moderate inversion [2]. For a good matching of these devices both W and L are considerably larger than the minimum feature size of the technology used. Furthermore, the layout was done carefully—the input transistors have common centroid structures and all interconnections were made symmetric.

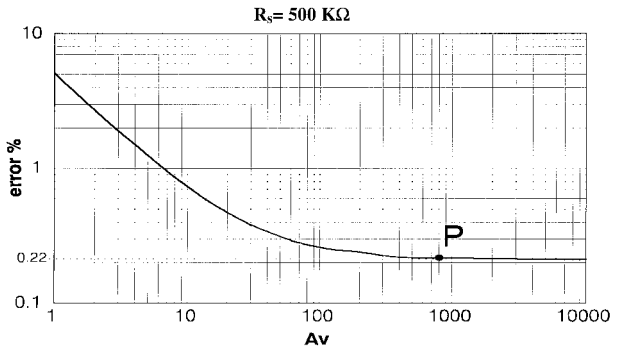


Fig. 6. Transresistance error (ideal gain is R_r).

Load transistors Mr1–Mr4 are usually designed according to the estimation that its transconductance should be three times lower than one of the input transistors in order to these dominate the noise and offset performance. While this is correct for thermal noise, such transconductance ratio is insufficient when considering flicker noise and pMOS transistors are used at input (note the load transistors are nMOS). For flicker noise, the parameter Y_F—*noise excess factor* [10]—that normalizes the total equivalent input noise density to the equivalent input noise density of only one of the input transistors is

$$Y_F = \left.\frac{v_{n_t}^2}{v_{n_{\text{M1}}}^2}\right|_{\text{FLICKER}} = 2\left[1 + \frac{Kf_N}{Kf_P} \cdot \left(\frac{g_{m_{\text{Mr1}}}}{g_{m_{\text{M1}}}}\right)^2 \cdot \frac{(W \cdot L)_{\text{M1}}}{(W \cdot L)_{\text{Mr1}}}\right]$$

where K_f [11] is the flicker noise coefficient. Then to have a low Y_F we must have:

$$\frac{g_{m_{\text{M1}}}}{g_{m_{\text{Mr1}}}} > 3\sqrt{\frac{Kf_N}{Kf_P} \cdot \frac{(W \cdot L)_{\text{M1}}}{(W \cdot L)_{\text{Mr1}}}}. \tag{4}$$

The condition (4), however, is difficult to be verified if we do not want to waste a lot of area in Mr1. Our option was to make $Y_F = 4$ (the input and load transistors generate

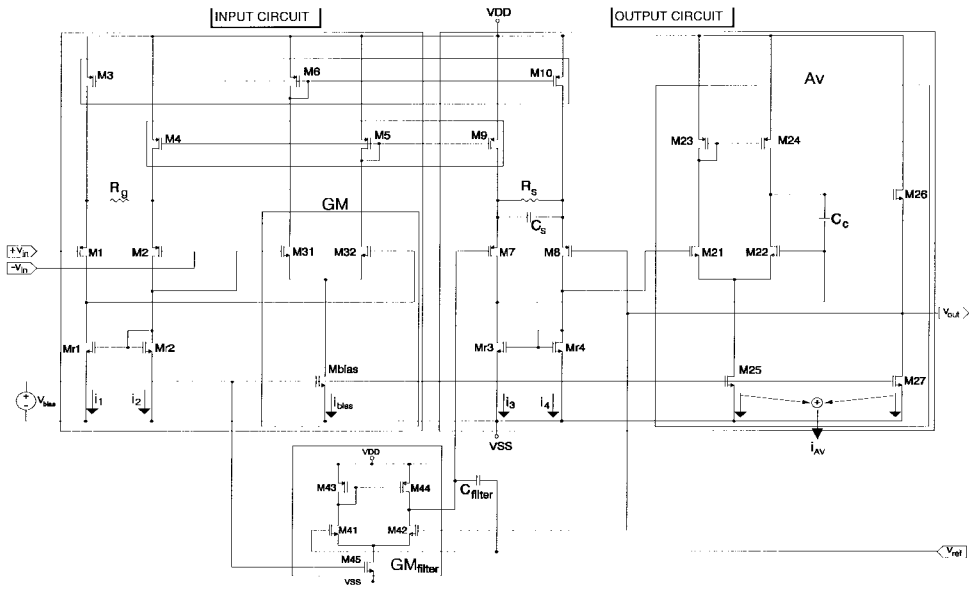


Fig. 7. Instrumentation amplifier (complete schematic).

the same noise). To obtain an integrated noise in the referred bandwidth less than 1.2 μV (rms), we end up with relatively large transistors: $(W/L)M1 = (600/25)$ and $(W/L)Mr1 = (24/200)$—all dimensions are in micrometers.

One reason why current feedback IA are frequently implemented in bipolar technology is the low transconductance gain of these devices. It is important to guarantee sufficient loop gain in the input and output circuits to make a good linearization of M1, M2 and M7, M8. For the input circuit the relative error in the gain (the ideal transconductance gain is $1/Rg$) as function of the transconductance of the block GM is shown in Fig. 5 (simulation).

For the output circuit we present the relative error as function of the voltage gain in ampere-volts (A·V) (with the ideal transresistance gain being equal to R_s) in Fig. 6. In this, as well as in Fig. 5, the point P represents the chosen value, which corresponds to a total error of 0.6%.

As we have to deal with two separate amplifiers the stability problems are somewhat relaxed. In the input circuit no special circuitry is necessary. At the output circuit a compensation capacitor C_c must be added to assure stability, because the loop gain is relatively high. This is done inside the block Av of Fig. 3. The complete circuit of the instrumentation amplifier is shown in Fig. 7.

III. Other Components of the IC

A. Programmable Gain Amplifier

The IA has a fixed gain of 500. Then we have an amplifier with a programmable gain of 1, 2, 4, or 10. This amplifier is also used as a buffer with low output impedance. As the signal level at its input is already high, there are no problems related to noise and precision as in the AI. We decided to use a simple configuration in which the most important design criteria was the low power consumption. Therefore, we designed a classical two-stage amplifier with a Miller compensation scheme and a class AB output stage. The AB class output stage allows us to source/sink high currents while the biasing current is low. It is used in a noninverting configuration and the gain is modified by switching the resistor R1 (see Fig. 1).

B. Autocalibration Signal Oscillator

There are always some gain mismatches among the 16 channels. This effect is easily corrected by software if a common signal is injected in all channels and used as reference to determine all gains relative to one given channel. In EEG systems the usual test signal is a square-wave with 10 Hz and amplitude of 50 μV.

We designed a relaxation oscillator with output levels not dependent on the power supply [12]. To make it frequency stable, the integration is performed by a capacitor over a current independent of the power supply value.

C. Voltage/Current Internal References

Since the voltage of a battery changes widely from a full-charge condition to the empty level, we integrated a stabilized current and voltage sources. We use a bootstrap type [12] with a safe start circuit.

IV. Measurements

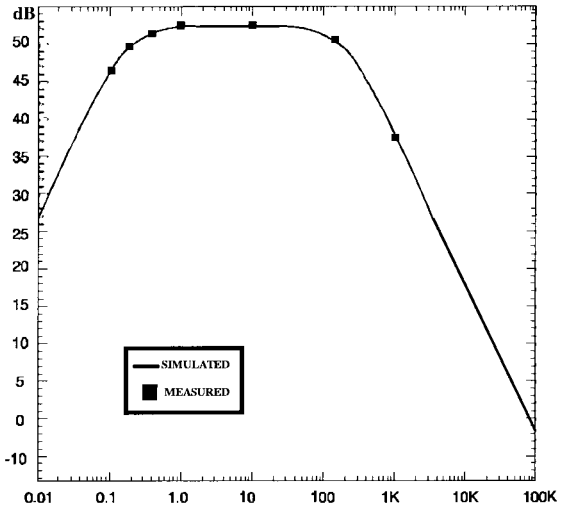
In Fig. 8 we show the frequency response and noise results regarding the intrumentation amplifiers. The noise is excellent and the typical CMRR is 99 dB, very close to the target value. Other important parameters of the IA's and the auxiliary circuits are presented in Table I. The worst result is the relatively low PSRR (40 dB), but as this chip is intended to be operated with batteries this problem is alleviated. The die photo is displayed in Fig. 9.

V. Conclusions

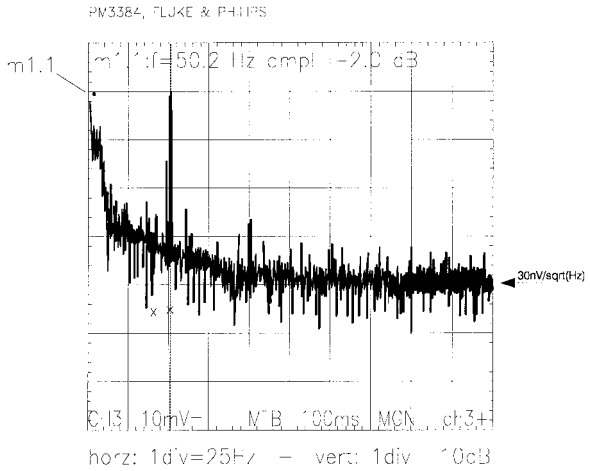
We have presented a monolithic analog front-end in a standard CMOS technology drawing 520 μA from a standard

TABLE I
MEASURED RESULTS

PARAMETER	value	Note
Active area	24 mm^2	
Power supply	±4.5 V	
Total current	520 μA	typical
Maximal error in gain	0.9 %	Any gain
Total noise (inp. Ref.) Referred)	1.4 μV (RMS)	0.3 < BW< 150 Hz
CMRR	99 dB	typical (50 Hz)
Offset (input)	0.29 mV	typical (hi-filter disabled)
Offset (output)	5.7 mV	typical (hi-filter enabled)
PSRR	40 dB	typical (low-freq)
Common Mode Range	-3.8<CMR<1.5 V	
f_{osc} (oscillator)	9.8 Hz	typical
v_{out} (oscillator)	56 μV	typical
Common Mode Range (output ampl.)	-2<CMR<2.5 V	
Slew-Rate (output ampl.)	0.5 V/μS	
Max. clock Freq. (MUX)	50 KHz	



(a)



(b)

Fig. 8. Instrumentation amplifier. (a) Frequency response. (b) Noise.

9-V battery. To obtain high CMRR and low noise we designed an instrumentation amplifier based in current feedback techniques with specifications suitable for EEG acquisition systems, namely a CMRR of 100 dB and a total input equivalent noise of only 1.4 μV. The IA design strategy to obtain a good noise behavior is also described and a formula that relates the transconductance of the input and load transistors with the flicker noise is derived.

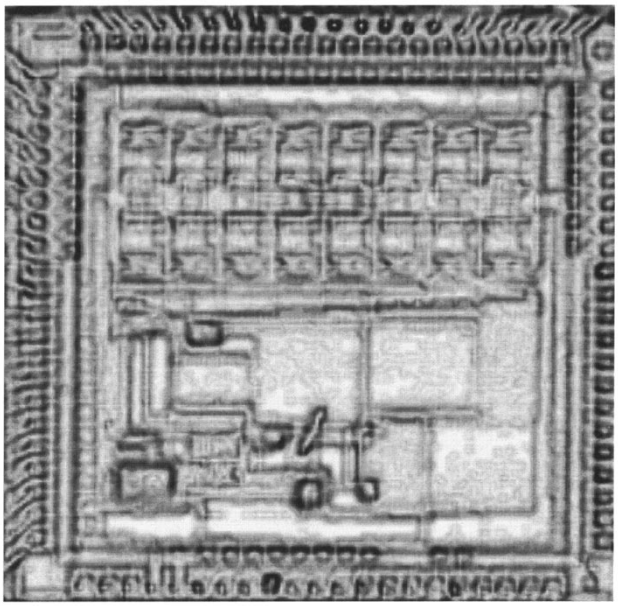


Fig. 9. Die photo. The 16 IA's are at the top.

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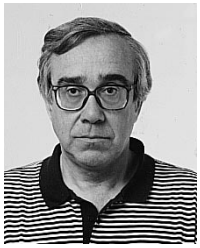

Francisco A. Vaz (S'86–A'86) was born in Oporto, Portugal, in 1945. He received the electrical engineering degree from the University of Oporto, Portugal, in 1968, and the Ph.D. degree in electrical engineering from the University of Aveiro, Portugal, in 1987. His Ph.D. dissertation was on automatic EEG processing.

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