

Simulation of Semiconductor Devices and Circuits at High Frequencies

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Due to the rapid progress in semiconductor technology, device sizes could be continually decreased during the last decades. This reduction allows for a higher package density which in turn increases the demands on modern simulation tools. This article covers some of the recent advances on the fields of device, circuit, and interconnect simulation which are fundamental requirements for accurate simulation of state-of-the-art circuits.

1. Introduction

With shrinking device dimensions device and circuit simulations with distributed devices need to be carried out by state-of-the-art tools, accounting for physical effects on a microscopic level. Several questions during device fabrication, such as device optimization and process control, can today be addressed by device simulation. For circuits operated in the GHz regime the influence of the interconnect structure becomes very important, and accurate simulation of the resulting parasitics is a must.

2. Device Simulation

To enable predictive simulation of semiconductor devices proper models describing carrier transport are required. The classic drift-diffusion transport model [1] is by now the most popular model used for device simulation. However, with down-scaling of the feature size, non-local effects become more pronounced and must be accounted for by using energy-transport or hydrodynamic models [2].

2.1 Mainstream Silicon CMOS Technology

As the driving force of today's semiconductor industry, mainstream silicon CMOS technology has attracted large attention during the last decades. The bulk of papers in the TCAD field were devoted to this subject and the behavior of the devices for not too small gate lengths is pretty well understood nowadays. For deep submicron devices with $L_g < 0.25 \mu\text{m}$, however, several second-order effects increase in importance and can no longer be neglected in an accurate simulation. Among these effects are quantum mechanical effects (quantization in the channel and tunneling through the oxide) and hot-carrier effects (non-local behavior and impact ionization) which further complicate the simulation.

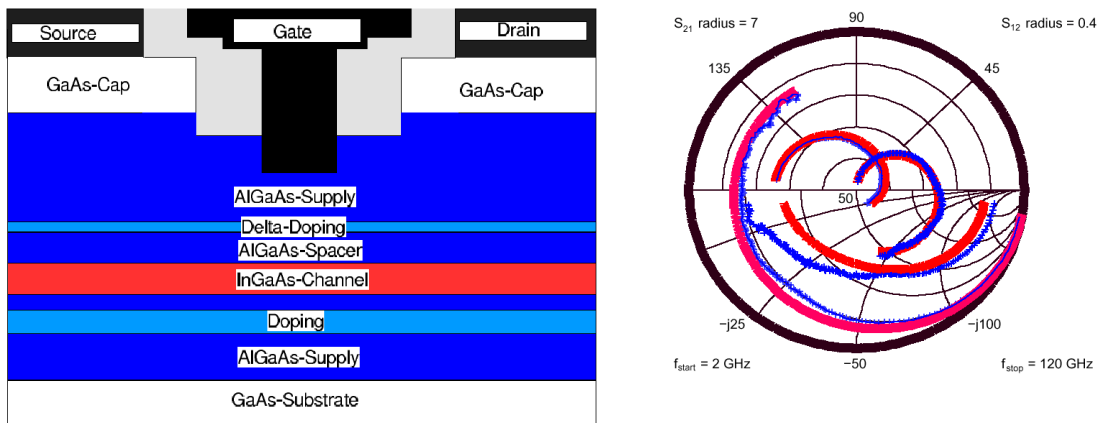


Fig. 1: Geometry of a HEMT and simulated (red / light gray) and measured (blue / dark gray) S-parameters ($L_g = 140$ nm).

2.2 High-Frequency Devices

Especially for high-frequency applications, SiGe and III-V heterostructure bipolar transistors (HBTs) and GaAs based high-electron mobility transistors (HEMTs) are being considered. The simulation of these devices is a challenging task with many issues still not satisfactorily solved. An important issue remains the proper modeling of heterostructure interfaces which can only be adequately dealt with when the quantum mechanical nature of the carriers is considered. A typical pseudomorphic InGaAs/AlGaAs HEMT on GaAs substrate with $L_g = 140$ nm is shown in Fig. 1 together with a comparison of the simulated and measured S-parameters at $T_L = 373$ K. These devices gain increasing importance for low noise applications like 77 GHz automotive collision avoidance radar. The parasitic elements were extracted from the measurements, and no fitting on device-level was employed. To obtain such an excellent agreement, many effects like energy relaxation, impact ionization, gate currents and self-heating must be modeled carefully.

3. Circuit Simulation

Circuit simulation has been traditionally performed using compact models of the individual devices. The most prominent program based on compact models is definitely SPICE which is being widely used. However, development of a compact model is a very complex task and requires permanent refinement to keep pace with modern technology developments. Even standard devices like MOS transistors are often only poorly described using these compact models. One of the most elaborate models is the BSIM3v3 [3] model which has been under continuous development throughout the last decade. While calibrating the model to measured data we found that the model failed for a device with $L_g = 0.13$ μm , even though accurate results have been obtained for $L_g = 0.25$ μm . Simulation results obtained by the compact model and a realistic device simulation are shown in Fig. 2 for the $L_g = 0.13$ μm device. As can be seen, the sub-threshold region is only poorly reproduced by the compact model but poses no problems to the device simulation. This region is very critical for low-power applications, and an accurate description is therefore mandatory.

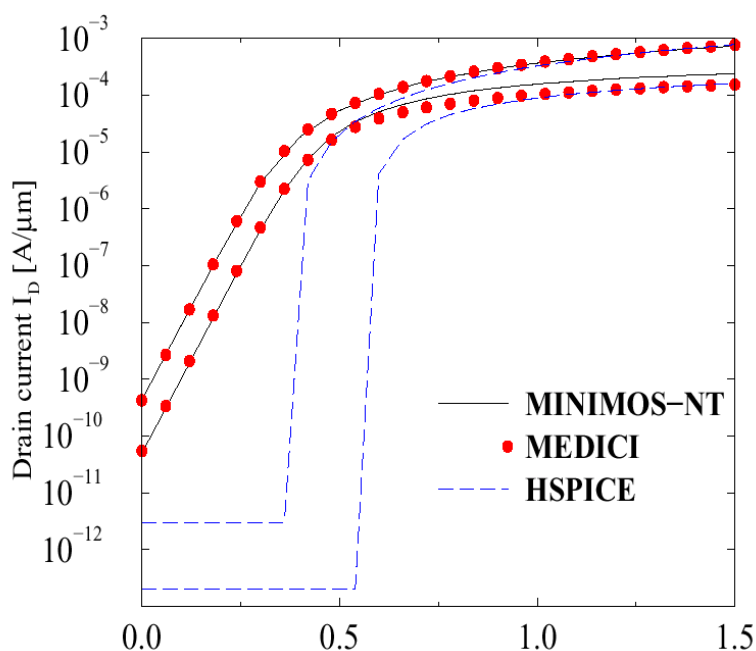


Fig. 2: Comparative simulation of a 0.13 μm NMOS I_d - V_g characteristics at $V_{DS} = 0.1$ V and $V_{DS} = 1.5$ V.

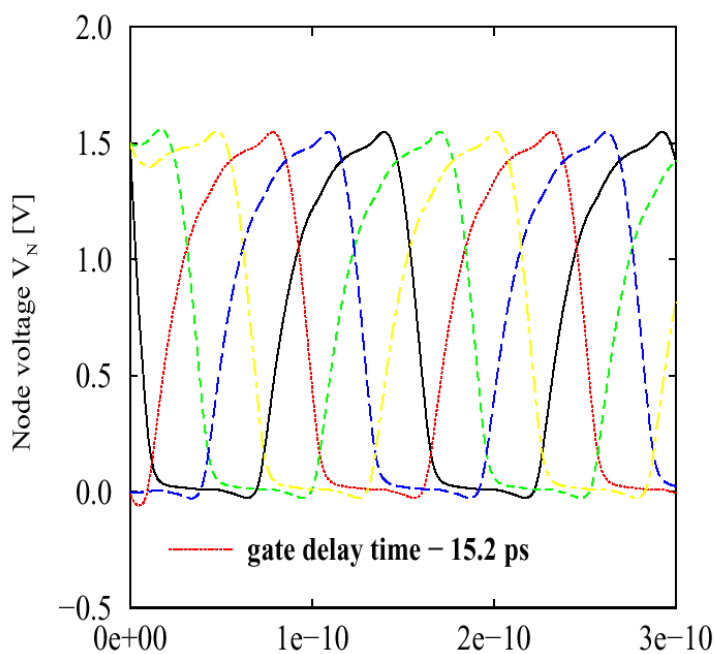


Fig. 3: The simulated node voltages of a five stage ring oscillator created with 0.13 μm technology

Mixed-mode device/circuit simulation provides a solution for this problem for up to medium-sized circuits. A typical example is the simulation of ring-oscillators which are commonly fabricated on test-wafers to investigate the high-frequency performance of the devices. Simulated node voltages of such a ring-oscillators are shown in Fig. 3 for the circuit of Fig. 4. The device simulator has been calibrated for a 0.25 μm technology

and used for a predictive simulation of $0.13\ \mu\text{m}$, a feature not offered by compact models. The simulated inverter delay time of $15.2\ \text{ps}$ is well within the scattering range of the measured data.

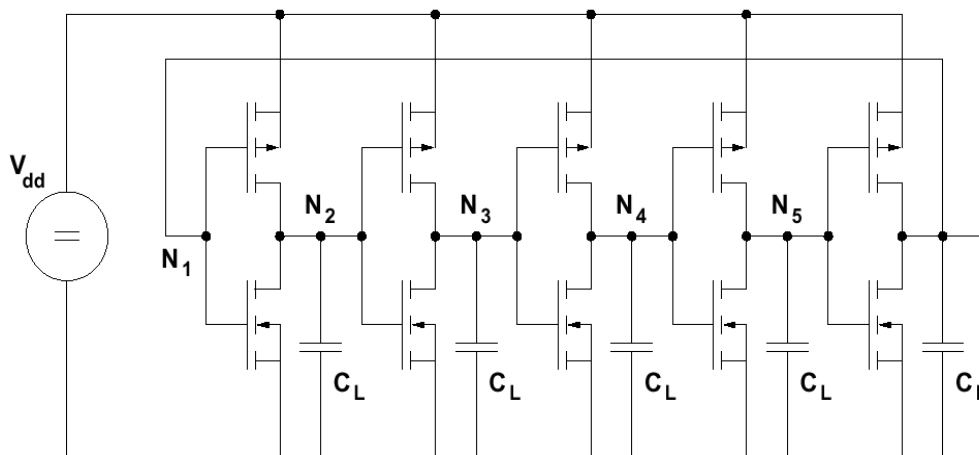


Fig. 4: Schematics of a five stage ring oscillator.

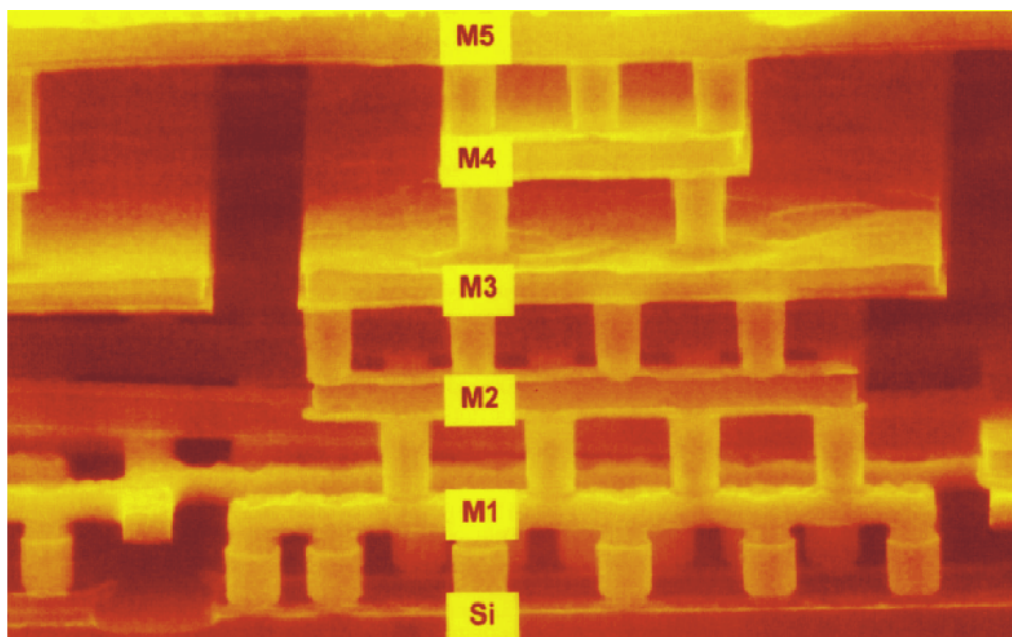


Fig. 5: Typical interconnect structure

4. Interconnect Simulation

Down-scaling of integrated circuits to the deep sub-micron regime increases the influence of interconnects on circuit behavior [4]. As devices are getting faster and line widths get smaller parasitic effects of the interconnects become the limiting factor for

further improvements in circuit speed. With clock frequencies in the GHz regime, integrated circuits will behave more and more like microwave circuits [5]. During the design phase care must be taken on various parasitic effects, like attenuation caused by resistive voltage drops, self-heating due to losses, delay times, crosstalk (caused by capacitive or inductive coupling or by the substrate), reflections incurred by discontinuities, skin-effect and eddy currents (e.g. in on-chip spiral inductors). A typical interconnect structure is shown in Fig. 5 which utilizes five metal layers. Extraction of the parasitic elements by means of simple analytical models yields rather unsatisfactory results, and a numerical simulation should be used instead. Highly satisfactory results for the generally very complex structures have been obtained using the finite element method. Simulated isopotential surfaces together with the extracted capacitances are shown in Fig. 6. A fully-coupled three-dimensional interconnect/device simulation would require too large amounts of computer memory and CPU time to be feasible from an engineering point of view. Thus, the parasitic elements are extracted and used for a mixed-mode device/circuit simulation.

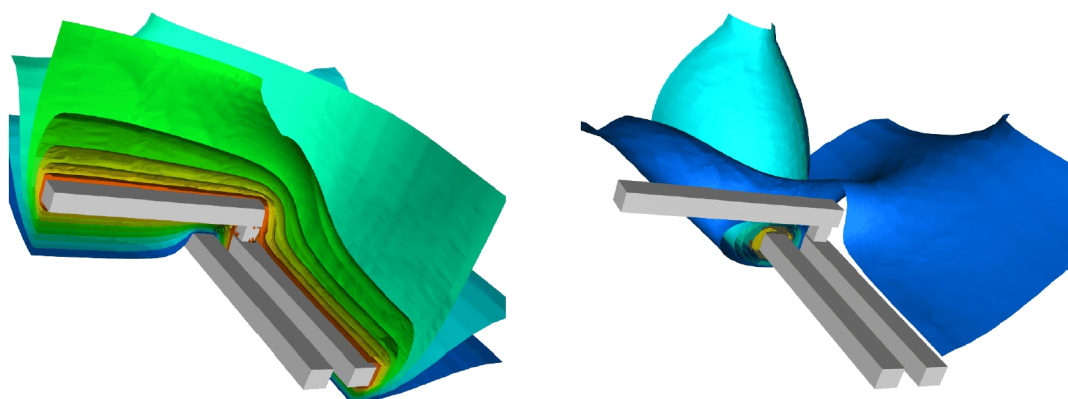


Fig. 6: Simulated isopotential surfaces of a typical interconnect structure ($C_{1,2} = 0.52$ fF, $C_{1,GND} = 1.04$ fF, $C_{2,GND} = 1.15$ fF).

Acknowledgements

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References

- [1] S. Selberherr, "Analysis and Simulation of Semiconductor Devices", Springer, Wien – New York, 1984.
- [2] W. Hänsch, "The Drift Diffusion Equation and its Application in MOSFET Modeling", Springer, Wien – New York, 1991.
- [3] Y. Cheng, M.-C. Jeng, Z. Liu, J. Huang, M. Chan, K. Chen, P.K. Ko, and C. Hu, "A Physical and Scalable I-V Model in BSIM3v3 for Analog/Digital Circuit Simulation", *IEEE Trans. Electron Devices*, vol. 44, no. 2, pp. 277 – 287, 1997.

- [4] A.K. Goel, "High-Speed VLSI Interconnections", *John Wiley & Sons*, New York, 1994.
- [5] N. P. van der Meijs and T. Smedes, "Accurate interconnect modeling: Towards multi-million transistor chips as microwave circuits", in *Proc. Intl. Conf. Computer Aided Design*, San Jose, CA, USA, Nov. 1996, pp. 244 – 251, IEEE.