Simulation of Gallium-Arsenide Based High Electron Mobility Transistors

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Abstract– **We present results for hydrodynamic simulations of pseudomorphic AlGaAs/InGaAs/GaAs High Electron Mobility Transistors (HEMTs) obtained by the two-dimensional device simulator MINIMOS-NT. The concise analysis of industrially relevant HEMT power devices of two different foundries for gate-lengths between l_g = 140 nm and l_g = 300 nm is carried out. Several aspects, including thermal and breakdown effects, the insulator-semiconductor interface, and the Schottky contact are considered.**

Keywords– **Electrothermal effects, Simulation software, MODFETs, Electric breakdown, Schottky barriers.**

I. Introduction

HIGH electron mobility transistors (HEMTs) have entered industrial large volume production for the RF market, and they replace the MESFETs in an increasing number of applications. For this reason III/V device simulation tools face a strong need to deliver predictable device information so far only known from the silicon based industry. The two-dimensional device simulator MINIMOS-NT [1] is enhanced to deal with effects especially relevant for III/V RF power devices. The HEMT devices presented in this work are used for power applications in the X-band, in the Ka-band, e.g. for local multi-point distribution services (LMDS), and for automotive collision avoidance radars in the W-band at 77 GHz.

II. Simulations

For the III/V binary semiconductors GaAs, AlAs, InAs, InP, and GaP and their ternary compounds we developed composition and lattice temperature dependent models that allow simulation of varying material composition, e.g. in the multilayer cap structures of power HEMTs. Thermionic emission and field-emission interface models are included to describe the AlGaAs/GaAs and the AlGaAs/InGaAs heterojunctions. Carrier temperature dependent relaxation times are implemented to describe high-field effects [2]. The models are verified for several HEMT and HBT technologies. We investigate pseudomorphic $Al_{0.2}Ga_{0.8}As$/ $In_xGa_{1-x}As$/GaAs HEMTs with x = 0.2-0.3. Measurements are performed for devices which are manufactured in two different foundries, further called Foundry A and Foundry B.

III. RF Power Devices

Fig. 1 shows the simulated and measured output characteristics of a pseudomorphic AlGaAs/InGaAs/GaAs HEMT with l_g = 210 nm gate-length and 4×40 μm gate-width for a substrate temperature of T_L = 300 K. Drain to source bias V_{DS} extends to 8 V and the measurements are taken using a 2 W/mm power compliance to protect the device.

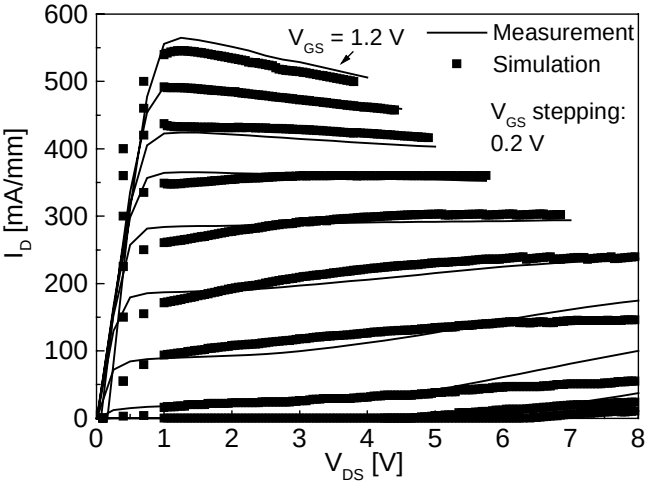

Fig. 1. Simulated and measured output characteristics including global self-heating of a HEMT of 4×40 μm gate-width and l_g = 210 nm [Foundry A].

When solving the heat flux equation self-consistently with the energy transport equations the following observation is used. The thermal boundary conditions for two-dimensional electrothermal simulations are evaluated by three-dimensional thermal chip simulations [3] which deliver thermal resistors for several thermal situations of the device such as single chip, on-wafer, or mounted on heat sinks. When using two-dimensional simulations the lattice temperatures $T_{L,2D}$ obtained solving the heat flux equation generally exceed the "real" three-dimensional temperatures $T_{L,3D}$ by up to 100%. This observation is especially critical since in power HEMTs a typical temperature rise $\Delta T_{L,3D}$, amounts to $\Delta T_{L,3D}$ = 150 K, as was shown by [3]. A 100% overestimation of $T_{L,3D}$ drives calculated $T_{L,2D}$ to $T_{L,2D}$ > 600 K, a range, for which the models become invalid.

Thus, a concept of global self-heating is used [4]. This allows, as shown in Fig. 1, to simulate the effects of self-heating which are visible especially for high gate to source voltage V_{GS} and increasing V_{DS}. We notice the negative output conductance visible in the measurement and in the simulation and observe a significant reduction of the (saturation) current.

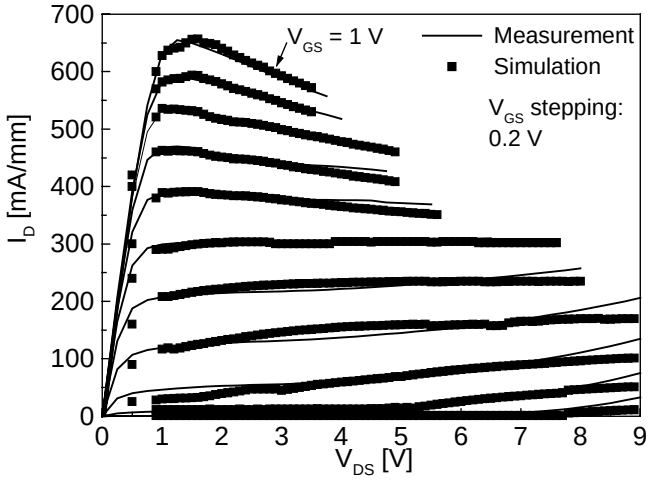

Fig. 2. Simulated and measured output characteristics of a power HEMT of 8×100 µm gate-width and l_g = 300 nm [Foundry B].

For RF power amplifiers above 10 GHz device and circuit optimization seek for a delicate compromise of RF-power and RF-gain. The resulting optimum DC-bias typically amounts to $V_{DS} \geq 5$ V. The corresponding high electric fields are compensated by double gate recess structures. Fig. 2 shows the simulated and measured output curves for an 8×100 µm pseudomorphic HEMT device of Foundry B up to V_{DS} = 9 V. Gate-length is l_g = 300 nm and a symmetric double recess is used to suppress impact ionization phenomena. To justify the simulation at a V_{DS} bias of 5 V and above an impact ionization model is included into the hydrodynamic simulation [5]. The coefficients needed are found to be in the order of magnitude of published data for bulk GaAs, AlGaAs, and InGaAs. To our finding they cannot be generalized independently of the technology, so they are calibrated for the particular technology.

To confirm the onset of impact ionization for the particular device bias dependent S-parameter measurements at high V_{DS} voltage are taken. The S-parameters are analyzed by evolutionary algorithms to fit an extended small signal equivalent circuit model with additional elements accounting for impact ionization [6]. The onset of impact ionization is found to start at $V_{DS} \geq 7$ V for the small signal situation. This corresponds to a calculated impact ionization rate in the channel of $G_{II} = 10^{29}$ cm^{-3} s^{-1}. The deviations of the simulation results with respect to the measurements especially at low V_{GS} voltages are explained by the influence of traps. Traps lead to a softer onset of the breakdown behavior which is at present not satisfactorily modeled in the impact ionization model. The impact on the gate current will be discussed below.

In Fig. 1 and Fig. 2 we show device output characteristics of devices with a double gate recess to reduce the electric field in the channel and in the barrier layer. When performing a geometrical recess optimization for such devices the strong condition of the Fermi-level pinning at the SiN-$Al_xGa_{1-x}As$ interface has to be included in the simulation. A critical issue is to maintain this condition at high V_{DS} bias in the simulation. To achieve this two means are used: First, distributed traps for the Shockley-Read-Hall (SRH) recombination model and a midgap trap energy are assumed at the interface. The sheet concentration found necessary is $n_s > 10^{12}$ cm^{-2}, which corresponds to a degenerate volume concentration of $n_s > 10^{19}$ cm^{-3}. Therefore, locally distributed interface charges along the interface are assumed. This assures the surface depletion caused by the Fermi-level pinning also at high V_{DS} bias for the complete interface. Furthermore, the obtained description is confirmed by the analysis of the gate-capacitances C_{gs} and C_{gd} from simulated (see below) and measured S-parameters. With this model, a geometrical recess optimization is performed, which is experimentally confirmed by increased breakdown voltage.

For the purpose of computational efficiency in HEMT simulations minority carriers are normally neglected. Accounting for the low p-type doping for the $Al_{0.2}Ga_{0.8}As$ of some 10^{14} cm^{-3} holes improves the description of the pinch-off current and is, as [7] stated, necessary for the description of the gate-current. Proper modeling of the gate current as a function of bias, especially V_{DS}, is a key issue for determining realistic breakdown voltages, both on- and off-state. The off-state breakdown voltages BV_{GD} (gate-drain) and BV_{GS} (gate-source) are experimentally determined for a gate current I_G = 1 mA/mm in a simple reverse diode measurement with the third terminal at floating potential. The on-state breakdown voltages BV_{DS} are measured as given by [8].

To simulate the gate current I_G the boundary conditions are used as described in [7]. The hydrodynamic Schottky contact model after [9] is implemented in MINIMOS-NT. It is necessary to describe the bias dependence of the gate current I_G correctly. The correction of the barrier height as well as the tunneling probability have to be included. The Schottky barrier heights are determined from available experimental data.

Fig. 3 shows the comparison of the simulated and measured gate current I_G as a function of V_{DS} bias for $V_{GS} = V_{th}$+ 0.2 V. The gate currents are found to show the expected dependence on V_{DS} and, in comparison to simplified assumptions, the right magnitude. Given the uncertainties of the gate current measurements and the assumptions of the model Fig. 3 demonstrates good agreement. Following the simulated gate current in Fig. 3 to I_G = 1 mA/mm an on-state breakdown voltage BV_{DS} can be obtained from simulation which amounts

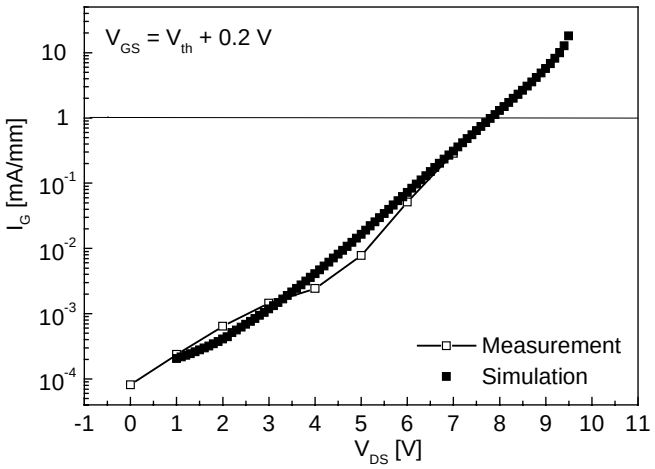

Fig. 3. Simulation of the gate current as a function of V_{DS} bias and comparison to measurements for a power HEMT with a symmetrical double recess.

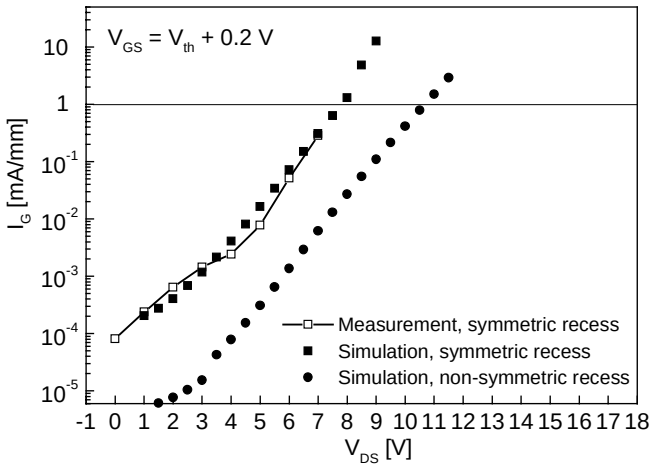

Fig. 4. Simulation of the gate current as a function of V_{DS} bias and comparison to measurements for a power HEMT with a symmetric and a non-symmetric double recess.

to approximately BV_{DS} = 8 V. Comparing this to direct measurements of BV_{DS} at the simulated device according to [8], where BV_{DS} = 8.5 V is obtained, a good agreement with breakdown experiments is demonstrated.

In order to prove the usefulness of the simulated breakdown voltages BV_{DS} as a function of device parameters Fig. 4 shows the comparison of the gate currents for two power devices. Device 1 is a power HEMT with a symmetric double recess, also used in Fig. 3, Device 2 is a similar device, where the drain side recess is extended by 0.3 µm. All other device parameters are kept constant. Fig. 4 shows the expected reduction of the simulated gate current I_G for the non-symmetric device, which is due to the relaxed electric fields at comparable V_{DS} bias. From this simulation we obtain a BV_{DS} = 11 V at I_G = 1mA/mm for the non-symmetric device. The measured on-state breakdown voltage BV_{DS} is found to be BV_{DS} =12 V at I_G = 1mA/mm.

A comparison of the measured off-state breakdown voltages reveals BV_{GD} = 10 V for the symmetric power device and BV_{GD} = 14 V for the non-symmetric device. This shows that for the devices optimized both on-state and off-state breakdown voltages scale in the same way. It is further found that the increase of the breakdown voltages scales with the decrease of the maximum electric field simulated in the AlGaAs barrier. Thus, from a different perspective the influence of the description of the SiN-AlGaAs interface is confirmed, which justifies the recess optimization mentioned above.

It can be concluded that the physical changes of the device are correctly incorporated in the model. An advantage of these simulations is that they describe the device for typical operational conditions and additional aspects, e.g. thermal aspects, can be included. Hence, these simulations can be used for device optimization within the assumptions of the model.

IV. SMALL SIGNAL SIMULATIONS

The small signal RF-behavior of the HEMT devices is simulated by small signal analysis at 5 GHz using MINIMOS-NT. Y- and S-parameters are obtained. Fig. 5 shows the comparison of simulated and measured S-parameters of a HEMT between 0.5 GHz and 50 GHz with a gate-length of l_g = 140 nm for a substrate temperature of T_L = 373 K [Foundry A]. Bias V_{DS} = 1.5 V and V_{GS} for maximum g_m are chosen. We find that the good agreement of the RF-quantities with the measurements is strongly correlated to the accuracy of the DC-simulations at the particular bias.

For the temperature dependence of the small signal elements a reduction of the transconductance g_m is observed. The DC equivalent g_m can be seen in Fig. 6 as a function of V_{GS} bias for two different substrate temperatures.
A rise of the semiconductor contributions of the source and drain resistors R_S and R_D in the caps due to the reduction of the low field mobility is further observed.

Furthermore, the change in the band gap results in reduced carrier confinement in the channel: This, next to the decrease of the saturation velocity, is one reason for the g_m-reduction. The capacitances C_{gs}, C_{gd} and C_{ds} are found to be nearly independent of thermal effects, except that the intrinsic transistor experiences a bias shift. These different bias conditions are caused by the temperature dependence of the parasitic R_S, R_D and R_G, which are part of the simulation.

In Fig. 1 and Fig. 2, both in simulation and measurement, a negative output conductance is observed due to the high heat dissipation at both high V_{GS} and V_{DS} bias. When determining the RF-output conductance g_{ds} from small signal S-parameter measurements, g_{ds} decreases as a function of rising T_L, but always remains positive. In the small signal simulations obtained by MINIMOS-NT in agreement with the RF small signal measurements a decrease of g_{ds} is found. Nevertheless,

the RF-g_{ds} never becomes negative. This again proves the readiness of the physics-based RF simulation for advanced applications.

V. CONCLUSIONS

Results for two-dimensional simulation of pseudomorphic AlGaAs/InGaAs/GaAs power High Electron Mobility Transistors are presented. The concise simulation of industrially relevant HEMT power devices of two different foundries for gate-lengths between l_g = 140 nm and l_g = 300 nm is carried out. Thermal aspects are considered as well breakdown effects, which are found to occur at high V_{DS} voltages. The importance of the insulator-semiconductor interface is stressed for geometrical device optimization with respect to breakdown, and an advanced Schottky contact model is successfully used to simulate bias dependent gate currents. The results demonstrate the possibility to make reliable predictions for III/V devices by two-dimensional device simulation tools.

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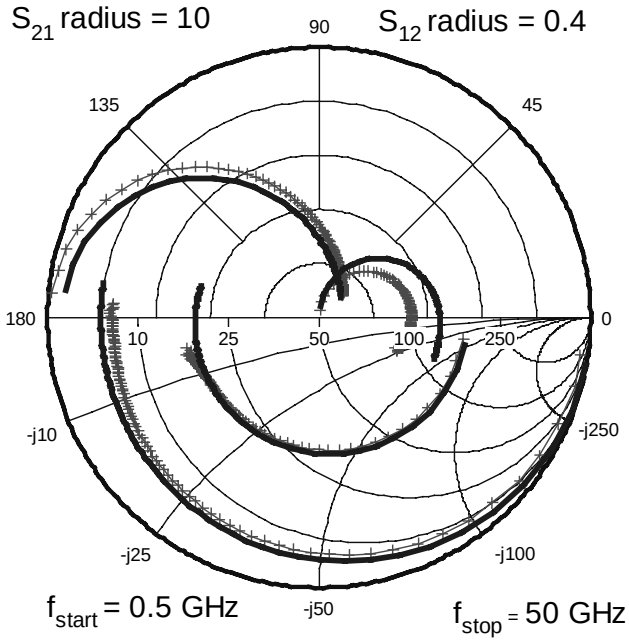

Fig. 5. Simulated (-) and measured (+) S-parameters at T_L = 373 K of a device with l_g = 140 nm [Foundry A].

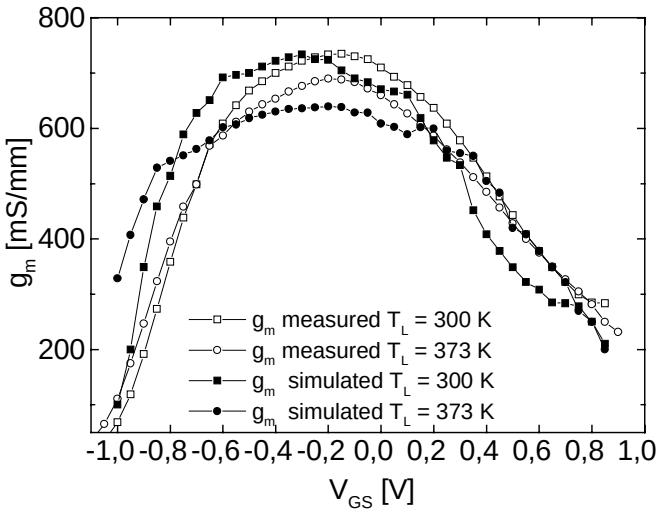

Fig. 6. Simulated and measured DC transconductance as a function of V_{GS} bias, parameter substrate temperature for the HEMT of Fig. 5.

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