Simulation of Polysilicon Emitter Bipolar Transistors

Vassil Palankovski
Institute for Microelectronics
TU Vienna
Gusshausstr. 27-29
A-1040 Vienna, Austria
palankovski@iue.tuwien.ac.at

Tibor Grasser
Institute for Microelectronics
TU Vienna
Gusshausstr. 27-29
A-1040 Vienna, Austria
grasser@iue.tuwien.ac.at

Martin Knaipp
Austria Mikro Systeme
International AG
Schloß Premstätten
A-8141 Unterpremstätten
m_knaipp@amsint.com

Siegfried Selberherr
Institute for Microelectronics
TU Vienna
Gusshausstr. 27-29
A-1040 Vienna, Austria
selberherr@iue.tuwien.ac.at

Abstract

We present results of two-dimensional simulations of polysilicon emitter Bipolar Junction Transistors (BJTs). For that purpose proper polysilicon contact models have been implemented in our two-dimensional simulator MINIMOS-NT. By accounting for self-heating effects a good agreement between simulated and measured forward and output device characteristics is achieved.

1. Introduction

Polysilicon emitter silicon based BJTs are attractive semiconductor devices with their high performance-to-cost ratio and are used for, e.g., power applications in modern mobile telecommunication systems. Accurate simulations save expensive technological efforts to obtain improvements of the device performance.

2. Device Fabrication

The device under investigation is a Double Base Silicon Bipolar Junction Transistor epitaxially grown by a Chemical Vapour Deposition process. An n-well (Arsenic), similar to the implanted one used in the standard CMOS technology, is grown during the epitaxial process. The buried layer (Antimony) is connected to a sinker (Phosphorus) to conduct the electron current from the buried layer to the collector contact.

The base consists of an intrinsic base (below the emitter window, Boron doped) and the extrinsic base (highly Boron doped under the base contact).

The emitter-base junction is formed by a diffusion process of a polysilicon layer which is placed on the p-doped base under the emitter window. After implantation of Arsenic, a diffusion process pushes the Arsenic into the p-doped base, thus forming the emitter-base junction.

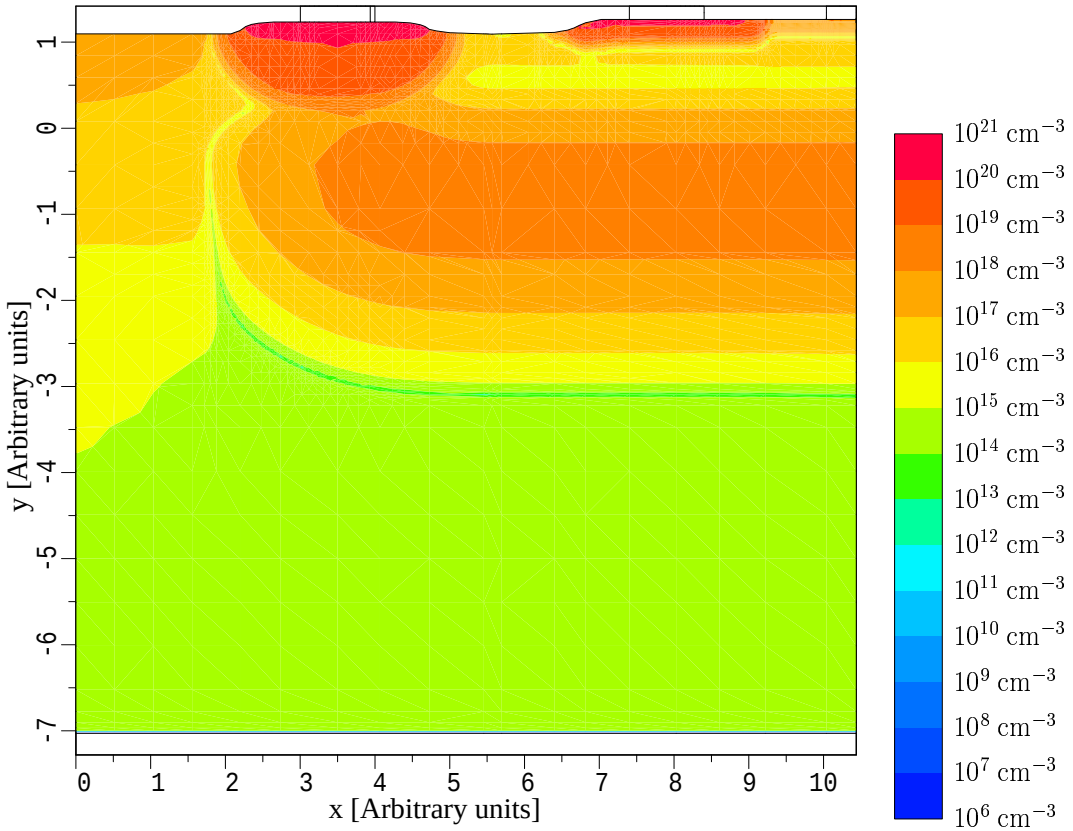

Figure 1. Device structure and net doping profile (absolute value)

3. Process Simulation

In order obtain results of practical use appropriate process simulation followed by device simulation and device optimization need to be performed. The process simulation is straightforward and identical results can be obtained using e.g. TSUPREM4 [1] or DIOS [2]. The device structure and net doping profile are shown in Fig. 1. The simulation domain covers only half of the real device, because of the symmetric device structure.

4. Device Modeling

The two-dimensional device simulator MINIMOS-NT [3] deals with different complex materials and structures. The physical models used are well calibrated [4], especially for silicon-based devices. Various important physical effects, such as band gap narrowing [6] (see Fig. 2), surface recombination, and self heating, are taken into account. In addition, we have implemented the polysilicon contact model after [5].

Thus, the dielectric flux D through the oxide reads

$$D = -\frac{\varepsilon_0 \cdot \varepsilon_{\mathrm{r}}}{\Delta} \cdot V_{ox} \qquad (1)$$

where ε_{r} is the relative permittivity of the oxide, Δ is the oxide thickness, and V_{ox} is the voltage drop over the oxide.

The electron and hole current densities across the contact interface J_n and J_p, respectively, read

$$J_n = \sigma \cdot V_{ox} \qquad (2)$$

$$J_p = q \cdot p \cdot S_p \qquad (3)$$

where σ is the oxide conductivity, p is the concentration of holes in the semiconduc-

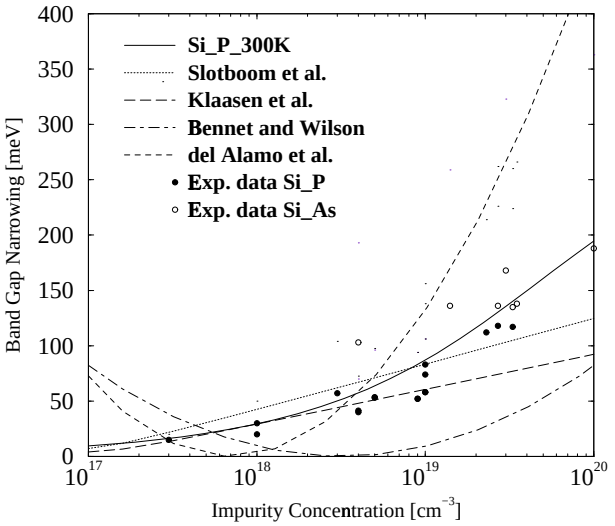

Figure 2. Band gap narrowing depending on the dopant species

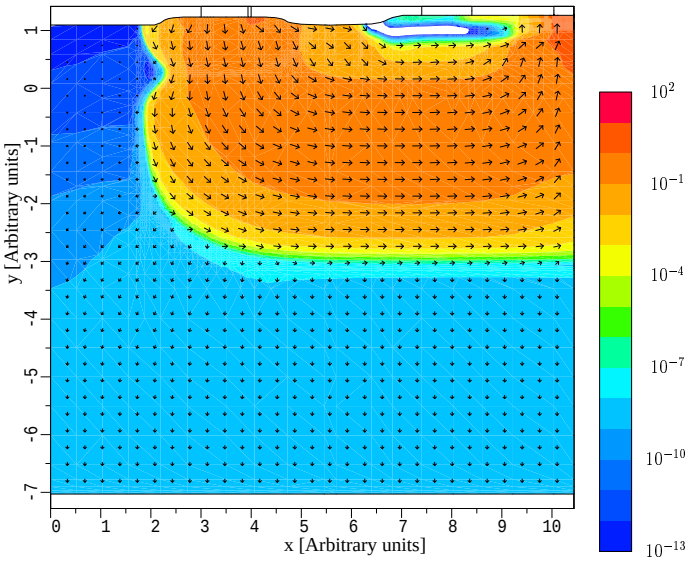

Figure 3. Electron current density at V_{BE} = 1.5 V

tor, and S_p is the surface recombination velocity for the holes. The voltage drop over the oxide V_{ox} depends on the Fermi level in the metal (which is specified by the contact voltage φ_{m}), the potential in the semiconductor φ_{s}, and the built-in potential ψ_{bi}.

$$V_{ox} = \varphi_{\mathrm{s}} - \varphi_{\mathrm{m}} - \psi_{\mathrm{bi}}. \qquad (4)$$

In the case of simulation of the output characteristics one meets severe problems to achieve realistic results, especially in the case of power devices. Therefore, self-heating effects were accounted for by solving the lattice heat flow equation self-consistently with the energy transport equations.

5. Simulation Results and Comparison with Measurements

The result for the electron current density at V_{BE} = 1.5 V is shown in Fig. 3. Note, the comparatively high electron current portion of the base current which occurs at this bias. Comparisons between the measured and simulated forward Gummel plot (Fig. 4) and current gain (Fig. 5) show good agreement.

In Fig. 6 we show the simulated output device characteristics compared to measurements for base current of 2, 4, 6, and 8 mA. We achieved also good agreement by including self-heating effects. The higher lattice temperatures which occur in the device significantly change the material properties of the device and, therefore, its electrical characteristics.

6. Conclusion

We present the device simulation results for polysilicon BJT compared to experimental data. The achieved very good agreement is a prerequisite for device optimization and fine tuning of fabrication process dependent parameters.

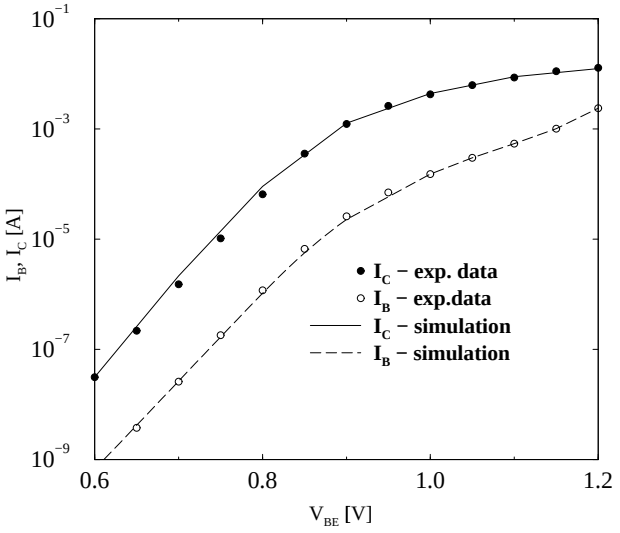

Figure 4. Measured and simulated forward Gummel plot at V_{BC} = 0 V at 300 K.

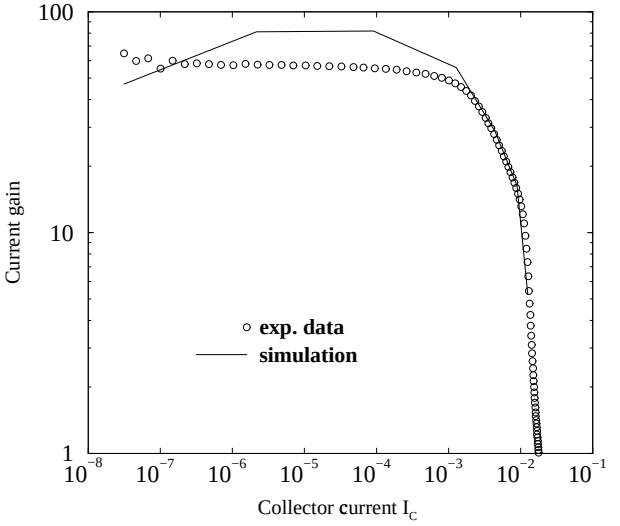

Figure 5. Current gain vs. collector current.

7. References

[1] Technology Modeling Associates, Inc., Palo Alto, CA, *TMA TSUPREM-4, Two-Dimensional Process Simulation Program, Version 6.2*, June 1995.

[2] ISE TCAD Manuals vol. 5, release 4, ISE Integrated Systems Engineering, 1997.

[3] T. Binder, K. Dragosits, T. Grasser, R. Klima, M. Knaipp, H. Kosina, R. Mlekus, V. Palankovski, M. Rottinger, G. Schrom, S. Selberherr, and M. Stockinger, *MINIMOS-NT User's Guide*. Institut für Mikroelektronik, 1998.

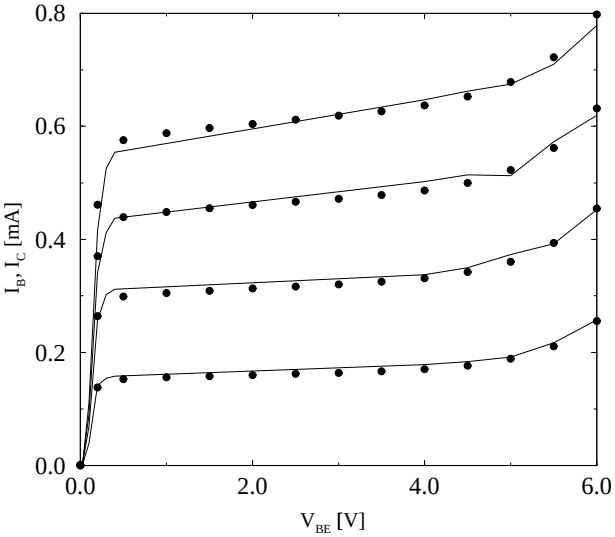

Figure 6. Measured (symbols) and simulated (lines) output characteristics.

[4] T. Grasser, K. Tsuneno, H. Masuda, and S. Selberherr, "Mobility Parameter Tuning for Device Simulation," in *28th European Solid-State Device Research Conference* (A. Touboul, Y. Danto, J.-P. Klein, and H. Grünbacher, eds.), (Bordeaux, France), pp. 336–339, Editions Frontieres, 1998.

[5] Z.Yu, B.Ricco, and R.Dutton, "A Comprehensive Analytical and Numerical Model of Polysilicon Emitter Contacts in Bipolar Transistors," *IEEE Trans.Electron Devices*, vol.ED-31, no. 6, pp. 773-784, 1984.

[6] V. Palankovski, G. Kaiblinger-Grujin, H. Kosina, and S. Selberherr, "A Dopant-Dependent Band Gap Narrowing Model Application for Bipolar Device Simulation," in K. D. Meyer and S. Biesemans, eds., *Simulation of Semiconductor Processes and Devices*, pp. 105–108, Wien, New York: Springer, 1998.

8. Acknowledgment

This work is supported by Infineon Technologies AG, Munich, Germany and by "Christian Doppler Forschungsgesellschaft", Vienna, Austria. The authors would like to thank to R. Minixhofer for supplying the measurement data.